EXHIBIT 15 Dickinson

Concerns:

Many play-back programs today don't even have a zoom option. To this extent, mode "b" may not be needed.

Mode c could be implemented today with 16bit/pel RGB (555) in s/w and the only improvement we provide is 24bit/pel capability and h/w color conversion (some level of acceleration). So mode "c" may not be needed as a special h/w.

If this is the case, maybe we do not need to do anything in h/w for Cinepak !

One idea: should we run 24bit/pel MS windows stored in 4:2:2 (Y0 U01 Y1 U01) format? This will allow us to run 24bit/pel MS Windows and use 16bit/pel memory space with no loss of quality. The windows driver could compress the data and the h/w could decompress it.

4.4 Nordic-1M Motion Video Architecture

Sasha Eglit, Rakesh Bindlish, Vlad Bril and Dave Keene are important contributors to the Motion Video Architecture definition.

4.4.0 The Problems to Solve & Generic Solutions

Nordic-1M is supposed to support CDROM play-back and live-video under Microsoft's Video for Windows. With all of today's VGA Compatible Graphics Controllers, the play-back picture pixel depth has to be the same as the surrownding MS Windows pixel depth. In other words, we have to run MS Windows in a 24bit/pel mode in order to display 24bit/pel in the play-back window.
The only way we can run today live video is from a Video Port (= Feature Connector). In this case we'll use an overlay or a color key to define the live video window.
Due to CDROM player, s/w interface complexity, CPU bus and Video Memory limitations, only small clips at 15fps or less can be playd-back today. So today we need a lot of Video Memory to run small clips in slow motion at low rezolution. Nordic-1M will try to use less Video Memory, increase the clips size, their resolution and speed.

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Nordic-1M is supposed to support:

- accellerated play-back for all popular CDROM compression standards, especially Cinepak and Indeo
- live video from a PCMCIA card in a system with a standard PCMCIA host adapter, for a "Multumedia-Ready Notebook Computer"
- live video from a Feature Connector, preferably VESA Advanced Feature Connector compatible, for a Multumedia Notebook Computer with direct NTSC input (full mother-

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board solution).

What will Nordic-1M bring to the Video plate:

A. Nordic-1M will break the dependency between the pixel depth of MS Windows and the pixel depth of the live-video / play-back window. By doing so, Nordic-1M will be able to run 24bit/pel LV/PB while running MS Windows in 8bit/pel or 4bit/pel (even planar) This will lead to high quality live-video and play-back, while minimizing Video Memory requirements.

B Nordic-1M will further reduce Video Memory requirements as well as Video Memory Bandwidth requirements by storing data in compressed form: 4:2:2 YUV (16bit/pel), 4:1:1 YUV (12bit/pel) or Sashapak YUV (2.6bit/pel)

C. Nordic-1M will define one architecture and work-frame to run both play-back and live-video in a unitary way for both s/w and h/w.

D. Nordic-1M will support up to two active LV/PB windows at the same time.

E. By providing h/w YUV->RGB conversion and 1:2 zoom Nordic-1M will accellerate playback for most standards, but mostly for standards that allow us access to their decompressor like Cinepack (for whose decompressor we have a licence).

Nordic-1M will not provide Cinepak specific accelleration (custom BLT).

On the Live Video from Feature Connector (or Video Port)

Due to pin-out limitations, the VAFC implementation has to be limitted to 8 pins of data requiring external muxing of 16bit data to Nordic. Further, the VAFC solution will be restricted to 5428 type support: overlay and color key (no memory video port). The only additions to the 5428 support will be the internal YUV-> RGB converter able to accept sequential 4:2:2 YUV (16bit/pel in avarage: Y0,U,Y1,V) and display it as a 24bit/pel RGB in the overlay/color-key window. We may also support horizontal 1:2 zoom with avaraging. Nordic-1M will be back-wards compatible to 5428 and it will support also 16bit 5-5-5 RGB Sierra and 5-6-5 RGB XGA pixel formats. As in 5428, live video from the Feature Connector can be executed only from mode 5F (640x480 256 colors).

In the following we will refer mostly to the other two modes of operation: play-back and live video from a PCMCIA card, which we'll call compressed live video, because due to PCMCIA bus bandwidth limitations, we assume that video data received by Nordic is compressed with Sashapak (see Sashapak details further in this spec). Please note that due to its huge advantages, it makes sense to use Sashapak as a mother-board solution too. The main reason we continue to support the Feature Connector based live video is the availability of drivers for 5428 which will give Nordic an early start in the live video arena

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Video Memory Band-width Constraints

Please note that, even with a 32bit wide Video Memory, there are severe memory band-width limitations when running 16bit/pel and 24bit/pel graphics modes.

Assumming that Nordic-1M does 8 CRT fetches in a row and 1 CPU cycle, for a CRT or TFT panel, here are the minimum frequency requirements for memory clock frequency at different rezolutions and pixel depths:

24bit/pel:
R+7P+R=12m+14m=26m with 1 CPU cycle per CRT FIFO fill fetches data for 32B/3B=10pixels
R+7P = 6m+14m = 20m with no CPU cycle during non-display time
min mclk freq = 65MHz / 50MHz @ 640x480 -> Nordic-1M upper limit at 5V CVDD
= 104MHz / 80MHz @ 800x600 -> too high
= 169MHz / 133MHz @ 1024x768 60Hz -> too high

16bit/pel:
R+7P+R=12m+14m=26m / R+7P = 20m fetches data for 32B/2B=16pixels
min mclk freq = 40.6MHz / 36MHz @ 640x480 -> OK even at 3V
= 65MHz / 50MHz @ 800x600 -> Nordic-1M upper limit at 5V CVDD
= 105MHz / 83MHz @ 1024x768 60Hz -> too high

12bit/pel
R+7P+R=12m+14m=26m / R+7P=20m fetches data for 32B/1.5B=21pixels
min mclk freq = 30.9MHz / 23MHz @ 640x480 -> OK even at 3V
= 49.5MHz / 38MHz @ 800x600 -> OK even at 3V
= 80.4MHz / 64MHz @ 1024x768 60Hz -> too high

8bit/pel:
R+7P+R=12m+14m=26m fetches data for 32B/1B=32pixels
min mclk freq = 20.3MHz @ 640x480 -> OK even at 3V
= 40.6MHz @ 800x600 -> OK even at 3V
= 52.8MHz @ 1024x768 60Hz -> OK at 5V

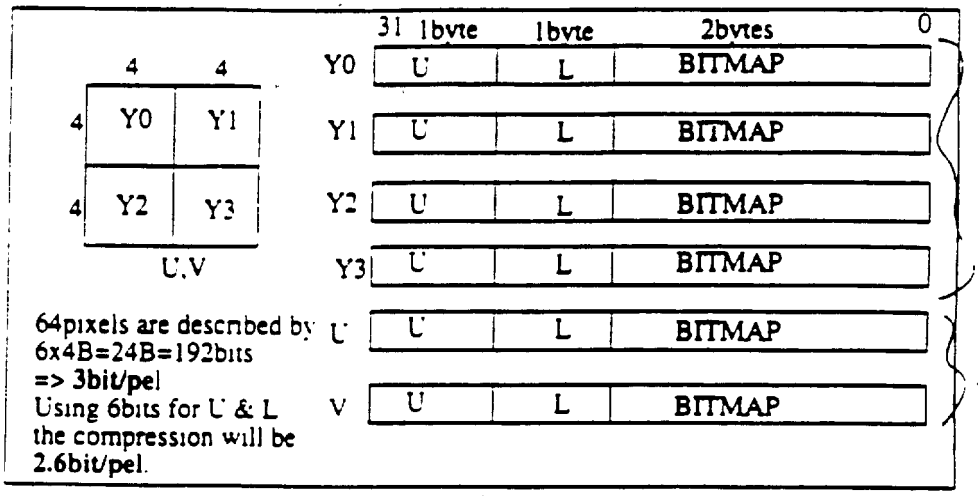
We may conclude that Nordic-1M will be able to run 24bit/pel only at 640x480 rezolution. 16bit/pel up to 800x600. 12bit/pel up to 800x600 and 8bit/pel up to 1024x768 rezolution These results apply only to CRT or TFT and single scan STN panels.
Please note that for dual scan STN panels the memory requirements increase significantly.

These severe memory bandwidth limitations lead us to attempt to minimize video memory traffic. If we store **Cinepak data in 4:2:2, with an avarage of 16bit/pel**, independent of Cinepak window size. **Nordic-1M will not be able to run Cinepak above 800x600.** Any attempt to execute vertical zoom with interpolation, even with two points interpolation will further aggravate this memory band-width bottleneck. The next step should be 100MHz SDRAM-s with a large CRT FIFO (32x32) or 64bit wide memory data bus. These considerations apply to any playback compression standard that stores data in video-memory as 16bit/pel in avarage. The key to a successful compression standard would be one that does decompresssion on the CRT memory read and stores data in memory as 8bit/pel or less, in avarage.

As we store live video at 2.6bit/pel and fetch it as if it was 8bit/pel with Sashapak, Nordic-1M should be able to run live video even at 1024x768.

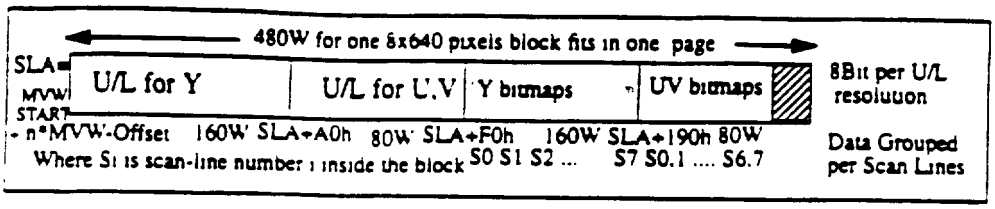
If we defined a new CDROM play-back standard based on Sashapak, then we could run even 1024x768 with 24bit/pel accuracy and keep it memory as an 8bit/pel. **Keith and Ken are actually working on it, with Sasha's help.**

Sashapak is a highly assymetric, lossy "Block Truncation" compression algorithm optimized for visually equivalent image processing.
Data is proccessed as Y,U,V one byte each. U and V are sub-sampled, characterizing one 8 by 8 pixel array, while Y is characterizing a 4x4 pixel aray. Actually one of two values is assigned to each pixel inside the 4x4 (for Y) and 8x8 (for U and V).
At compression time, the compression chip determines a threshold and two values U&L for each group of sixteen (4x4) pixels. This way all pixels above threshold will be assigned the value U, all pixels below threshold will be assigned the value L.



At decompression, the bitmap will control a mux between the U and L values. This way the decompression is straightforward
The main drawback of this approach is that a BITMAP contains Y data from 4 scan lines and U,V data from 8 scan lines. When data is read from memory to be displayed only data from one scan line is used. Similarly the U/L values apply to several scan-lines and the same value will be read in each scan line. The same data will be read again and again in each scan line raising the actual memory bandwidth requirements to an equivalent of 16bit/pel map.
In order to overcome this problem and reduce memory bandwidth requirements, Sasha proposed a **scan line oriented, segregated mode of data organization**. This would require the Sashapak compression chip to write compressed data in a specific way puting the strain on the compresion chip address generator. The basic principles of the new organizations are.
1 Data is organised in the MV Window in chunks of 32 sequential pixels.
a)For **8bit U/L resolution**, as one Y covers 4 pixels, 8 U/L sequential values are needed, 16bits each -> **8x16/32=4W** (8x12/32=3W for 6bit res. U/L) (where W is a 32bit word).
b)U and V U/L data is packed together in the same word (16bits for U U/L and 16 bits for V U/L -> total 32bits=1W) and as one pair of U and V applies to 8pixels, 4 such values are needed for 32 sequential pixels -> **4x32=4W**. (4x12x2/32=3W for 6bit res. U/L)
c) The mask data is also scan-line oriented: all 32bits of Y mask of sequential 32pixels are placed in one 32bit word and due to sub-sampling on U and V, all 32bits of U and V mask of sequential 32pixels are placed in one 32bit word. So in 2W data for 32 sequential pixels on one scan line is packed. -> **2W** (the same for 6bit resoluuon for U/L)

d) For 640x480 window size, even at 8bit U/L resolution, data for 8 scan-lines fits in one DRAM page (symetric DRAM-s assumed): 320WY+80WU+80WV=480W < 512W page



f) The key to memory bandwidth opumization is the fact the the compression chip will organize data sequentially over 32 pixels instead of 8. This will be done for the mask bits which will be organized sequentially by scan line and for the U/L data. This way a 32bit word of Mask data contains only information for the current scan line and no extra memory fetches are required. The main reason we segregate U/L for Y and U/V is the fact that we want to use 6bit U/L. In this case it is easier to identify the proper U/L info chained within 32bit words if the words are sequential and we have a fix relationship between their address and the 6bit U/L quantities.

g) If we calculate now the amount of data we need to fetch to display 32 sequential pixels:
- for 8bit per U/L: 4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B
  --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
- for 6bit per U/L: 3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B
  --> 32B/32pixels = 8bit/pixel

This is a very good data fetch ratio, much better than the 16bit/pel we'd get without the opumization.

g) When reading data from the Motion Video Window the controller will generate the following sequence of addresses, all of them in the same DRAM page (8bit per U/L):
- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset, +1, +2, +3
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h, +1, +2, +3
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h
- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset+4, +5, +6, +7
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h+4, +5, +6, +7
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h+1
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h+1
- now the MVW FIFO is full.
- chunks of ten 32bit words will be proccessed for every 32pixels displayed
- the MVW FIFO gets empty after the first 10 words being read for decompression and display.

Please note that all data for every 8 scanlines starting from the top of the MVW is in the

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same DRAM page.
Because we have to fetch the MVW Data before we start displaying it, and because at that time the CRT FIFO does not empty as fast as it is needed (unless MS Windows is running at the same pixel depth as the MV Window), it is necessary to have a separate FIFO for the MVW or at least half the FIFO (at least 10W for 8bit per U/L and at least 8W for 6bits per U/L).
h) When we run 6bit per U/L, because the Video Memory band-width requirements are as if we were running 8bit/pel, we could do vertical zoom with avaraging. But there should not be a need for zoom with Live Video because there is enough CPU and memory band-width to run 640x480 windows even when MS Windows is run as 1024x768 4 or 8bit/pel.

Conclusion: With Sashapak we can get data organized in memory such that the memory bandwidth is as for 10bit/pel (8bit U/L) or 8bit/pel (6bit U/L) pixel depth. The actual memory area will be close to 3bit/pel or 2.6bit/pel depending on the resolution of U/L values - 8 or 6bits per value.
Please note that the memory area will be slightly larger due to the fact that we use only 480 words in a page of 512.

4.4.2 YUV to RGB Conversion Algorithm

The ideal YUV to RGB transformation is
R=Y+1.37V
B=Y+1.73U
G=Y-0.699V-0.336U

After defining an objective way of measuring color error, Sasha came up with the following Conversion algorithm
R=Y+1.375V=Y+1 3/8 V
B=Y+1.75U=Y+1 3/4U
G=Y-0.375U-0.75V= Y-(3/8U+3/4V)

This algorithm can be implemented with 8 9bit adders and it should support excess 128 or two's complement U,V formats (U,V may be negative while Y is always positive).
This algorithm will be used with Live Video
For Cinepak, the YUV->RGB converter will be reconfigured to the Cinepak YUV->RGB conversion rule:
R=V+Y
B=U+Y
G=Y-V/2-U/4

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4.4.2 Motion Video Architecture Functional Blocks

Instead of treating play-back and live-video as two separate modules, we'll isolate several generic functions to be used by both:

- Display Window Generauon Block:
  allows s/w to define one or two play-back or live video **window**(s)
  The MV Window is defined in memory cycles relauve to the start of line in horizontal and frame in vertical direcuon. Horizontally the unit of measure is different outside relative to the inside of the window: the horizontal window start coordinate is expressed in memory cycles for the surrounding pixel depth (MS Windows pixel depth, normally 4 or 8 bit/pel), while the width of the MVW is expressed in memory cycles for the MVW pixel depth (8bit RGB, 16bitRGB, 422YUV spacial, 422 YUV linear, 411YUV linear, Sashapak)

  - **XS** = MVW Horizontal Start Coordinate (in surrounding pel depth memory cycles)
    The horizontal position is programmed with 8 pixel resoluuon (0,8,16.... pixels starung from the left side of the screen)
    XS register CR34[7:0] -> 8 bits
    (up to 1K pels in increments of 8 pels)
    To get an early warning, we will require XS to be programmed 8 pixels less than the actual position: 0 is zero, 1 is 16pels, 2 is 24 pels....
  - **XW** = MVW Horizontal Width (MVW pel depth memory cycles)
    XW register CR35 [7:0] -> 8 bits
    (up to 1K pels in increments of 8 pels)
    To get an early warning, we will require XW to be programmed 8 pixels less than the actual width: 0 is zero, 1 is 16pels, 2 is 24 pels.... width.

  - **YS** = Vertical MVW Start (in true scan-lines not affected by scan-line doubling or panel vertical expansion)
    10 bits in CR36[1:0] (msb-s) and CR37[7:0] (lsb-s)
  - **YE** = Vertical MVW End
    (all bits are programmed, in true scan lines)
    10 bits in CR36[3.2] (msb-s) and CR38[7:0] (lsb-s).
  - **SAdOf**= Surrounding Address Offset (a number to be added every line to the surrounding CRT Address Counter value to allow it to jump over the MVW without counting through it. This allows calculaung the surounding restart address.) This number depends on the surrounding mode resolution. Assuming a maximum line of 1024 pels, in increments of 4 pels per address (8bits/pel), 256 addresses is enough -> 8bits.
    8bits in CR39[7:0]
  - **WMAdS** = MVW Memory Address Start in increments of 16KB = 4KW (a phisical address 00000:3FFFF for 1MB or 00000:7FFFF for 2MB Video Memory).
    7bits in CR3A[6:0]

  - **WMAdOf = MVW Memory Address Offset** (A number to be added to the current MVW Start Address to get the next MVW start Address). Having this s/w model allows panning through a large image for the MVW. The actual image stored in memory may be as large as 1K pixels

at 16bit per pixel (2 per word) -> 9bits.
9bits -> in CR36[4] (msb) and CR3B[7:0] (lsb).

Because the CRT Address Counter counts surrounding memory cycles, during the MVW display it would count a wrong number corresponding to the MVW pixel depth. To avoid this wrong count, the CRT Address Counter is stopped while MVW is displayed and loaded with the value corresponding to the end of MVW and restart of the surrounding display. As this address value changes every line, an offset is specified and will ba programmed by the MS Windows driver depending on the MVW size and pixel format. The horizontal size of the window is controlled by a different counter counting to XW. During the MVW display the adddress will be generated by the same CRT Address Counter which will be loaded with a MVW Memory Address Start (WMAdS).

- **XW8P = MVW Horizontal Width in 8 pixel units.** Defines the size of the window in 8 pixel units. It is used to terminate the window horizontally. It may require to program the value minus one or two. To be Defined Later. Register CR3D[6:0] will contain this value.

Every scan-line

MVW Scan-Line Start Address = Previous Scan-Line MVW Start Address + WMAdOf

Scan-line doubling for "zoom" should be taken into account when designing the MVW Architecture: on the address generation block.

- **Off-screen MV Memory Addressing and Access Control.** This includes data type tag generation based on MV memory Address and the circuitry placing the tags in the CRT-FIFO. This block has provisions for scan line replication by repeating the MV address generated on the previous scan line of the MV window (only).

As Cinepak needs 4:1:1 rectangular format the MV Memory Address Counter needs to count in a non sequential way:

Y0Sn Y1Sn Y2S(n+1) Y3S(n+1) U V

implies an address counter that can skip over two numbers, or maybe **a second address counter that starts counting from 2 instead of zero.**

- **One tag bit is generated based on CRT Address and is 1 if the data in the CRT FIFO is from the MVW, other-wise is 0.** This tag bit, called the **steering bit** will be delayed through the enure data path and end up controlling the final video data mux just before the DAC.

Other tag bits called "data-type" tag bits encode the type of 32bit word in a given data format and are used by MVW Decoder/Serialiser to steer CRT-FIFO data at CRT-FIFO read.

For instance, in 4:1:1 linear data format, data is stored in memory and in the CRT-FIFO as Y0Y1Y2Y3 U03V03Y4Y5 Y6Y7 U47V47, 3 groups of 32bits. Two "data-type tag bits will mark the three types of 32bit words so that steering logic knows where to place the three words in the data serialiser.

Simularly Sashapak will need 3 "data-type" tag bits to encode 8 32bit words (for 6bit per U/L) or 4 "data-type" tag bits to encode 10 32 bit words (for 8 bits per U/L).

16bit RGB 5:6:5 and 5:5:5 and 8bit RGB 3:3:2 can either use the **standard VGA data**

path. which in 5428 was extended to 16bit wide (used for 16bit/pel 1kx768 interlaced) or the new data path. **if a phisically new data path will be actually created**.

- **MV Data Path .** This is area wise the largest piece. It consists of a new 16bit wide data-path with the same delay as the VGA data path. that takes MV data from the MV prefetch cache and the CRT FIFO. treats it appropriately depending on the MV data format encoded in the MV tags and converts it to 24 bit YUV first and 24bit RGB second. Horizontal zoom with avaraging (or maybe 5 levels of interpolation) is in this block too

- **Larger (26 or 24 stages) CRT-FIFO. Variable CRT-FIFO threshold and its control.** Because the MS Windows pixel depth and MVW pixel depth don't match. it is necessary to reserve CRT-FIFO space to fill in enough high pixel depth data before the MVW display starts. In Sashapak this means 10 or 8W (for 8 or 6bits per U/L respecuvely).
This funcuon can be implemented as a dinamic threshold size modificauon of the CRT-FIFO. If the CRT-FIFO has 24 stages instead of 16 but only 16 stages are used before the MVW but it is switched to 24 when MVW fetches start. there will be 8 more stages to fill at that time ensuring more prefetched data in the CRT-FIFO at the beginning of each MVW scan-line.
In normal operation the threshold is 8 (or 6).
Here is the sequence of events that follow the detection of MVW start:

1. **Drop CRT-FIFO threshold to 1 to get immediat service & make 10 (or 8) more stages available in the CRT-FIFO.**
2. **Start fetching MVW data till CRT-FIFO is full.** (BLT in progress will increase latency)
3. **Increase threshold to 10.**
4. **Proceed as such till end MVW.**
5. **Load the CRT Address Counter with its last contents + SAdOf**

(where SAdOf = Surrounding Address Offset)

7. **Continue fetching based on the new address** (start with random cycle). **CRT-FIFO threshold remains the same - at least 10 or 8. CRT-FIFO size is still 26 or 24.**
8. **At the end of line. upon flushing the CRT-FIFO before prefetch, decrease CRT-FIFO size back to 16 keeping the threshold the same.**
9. **Go back to #1 for the next scan-line.**

This sequence is applied if MVW pixel depth is higher than surrounding pixel depth. If MVW pixel depth is lower than surrounding pixel depth, then the action described at #1 above takes place at the end of MVW, instead of the beginning. ***In other words, FIFO depth extension takes place when a switch from low to high pixel depth occurs.*** **If MVW pixel depth is the same as the surrounding, only the address is switched. In this case the CRT FIFO depth and the threshold remain the same.**

- Steering logic decode the tags comming out of the special addition to the CRT-FIFO and the pre-fetch buffer and controls the decompression, formating and serializauon. (they tell the formatter what data is Y, U or V).

- What about the video serializer load and the CRT FIFO read signal? What hapens to them when in MVW? They are one signal today.
WHEN the data path switched to display MVW data, what hapens with the VGA Video Data Path is don't care as we do not display that data, except for the h/w cursor anf the h/w icon that do not go through the standard VGA serializer. So we'll probably stop the VGA data path untill the point h/w cursor and h/w icon are combined into it, to save power, as we will stop the MVW data path when not in use, for the same reason.
So, the Video Serializer Load may be stopped while MVW data is displayed, **but the CRT FIFO read will be going on, with a frequency and shape depending on the data format loaded in the CRT FIFO for display.**
In RGB 3:3:2 8bit/pel direct color mode CRT-FIFO read will be generated every 4 vclks.
In standard RGB 5:5:5 or 5:6:5 16bit/pel modes CRT-FIFO read will be generated every two vclks.
In YUV 4:2:2 24bit/pel (Y0 U Y1 V on one scan line) the CRT-FIFO read will be generated also every two vclks.
IN Sashapak 10 (for 8bit per U/L) or 8 (for 6bit per U/L) CRT-FIFO read pulses will be generated every 32 vclks.
- The MVW Address Counter, loaded at the beginning of each MVW scan-line with a start address calculated based on the Start MVW Address and the MVW Address Offset, will count at format dependent rate for as long as the CRT-FIFO is not full. Because the CRT-FIFO will be emptied faster in the MVW (in general the pixel depth will be higher in the MVW) there will be requests for more memory cycles when displaying in the MVW.

- If either h/w cursor or h/w icon are on, they should be displayed even if the direct data path is used. In this case both video data pathes will clock and the steer tag will point to the VGA data path when either h/w cursor or h/w icon or both are displayed, even on top of a MV window. Please note that neither the h/w cursor, nor the h/w icon data go through the CRT FIFO or the VGA Data path except for the final pixel address block and the RAMDAC RAM, though they have a special path in the RAM. So we could stop most of VGA data path (including the internal palette) but not all of it even if we are in 16bit/pel mode (the new one that goes through a separate 16bit data path).

- If we are in a 16bit/pel mode with no h/w cursor or h/w icon, or in a 640x480 MVW mode filling the screen, we can stop the VGA data path to save power.

- The off-screen MVW memory will be a programable start memory array normally placed towards the end of the memory, but before h/w cursor, h/w icon and the half frame buffer, even the color one. The start of the MVW memory will be programable in increments of 4KW (16KB) as a physical address -> 7bits to program.

CR3B[6:0] is the MVW Memory Array Start Address.

2MB configuration will support enough memory to support:

- one 640x480 3bit/pel window or up to two 320x240 3bit/pel (Sashapak) -> 32KW
- one 640x480 16bit/pel window or two 320x240 16bit/pel windows

(153.6KW=614.4kB out of 256KW or 512KW available depending on the memory configuration)

- all of the above at the same time up to a total of two windows though.

1MB configuration will support:

- one 640x480 3bit/pel Sashapak window or two 320x240 Sashapak windows or
- two 320x240 16bit/pel windows.

Please note that about 24KW are needed for 800x600 DS Color STN HFB, the h/w cursors and h/w icons while about 18KW are needed for 640x480 DS Color STN HFB and that

- 640x480 4bit/pel requires 38.4KW
- 800x600 4bit/pel requires 60KW
- 1024x768 4bit/pel requires 98.3KW
- 640x480 8bit/pel requires 76.8KW
- 800x600 8bit/pel requires 120KW
- 1024x768 8bit/pel requires 196.608KW

Video Motion Formats supported are:

- 8bit RGB 3:3:2 going through the palette (RGB 3:3.2)
- 16bit RGB (5:5:5 Sierra and 5:6.5 XGA) not going through the palette -> this is a 16bit/pel that does not require double dotclock !!
- 4.1:1 array converted to 4.2.2 Y0 Y1 Y2 Y3 U V -> Y0UY1V Y2UY3V for Cinepak (with Y2Y3 for the next scan line)
- 4.2.2 linear Y0UY1V from TV Decoder
- Sashapak format (we'll support only 6bit/pel)
  - for 8bit per U/L.

    4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B

    --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
  - for 6bit per U/L

    3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B

    --> 32B/32pixels = 8bit/pixel

CR3C[3:0] will encode the pixel format for the first motion video window data:

0h = 0000 = 8bit RGB 3.3.2 going through the palette
1h = 0001 = 16bit RGB Sierra (5:5.5)
2h = 0010 = 16bit RGB XGA (5:6.5)
3h = 0011 = 4:2:2 YUV Y0UY1V
4h = 0100 = 4:1:1 YUV linear Y0Y1Y2Y3UV
5h = 0101 = 4:1:1 YUV array Y0Y1Y2Y3UV but Y2Y3 are in next scan line
6h = 0101 = Sashapak 6bits for U/L
7h = 0110 = Sashapak 8bits for U/L
8h:Fh = 0111:1111 = reserved

CR3C[4] = Enable Motion Video Window
CR3C[5] = Enable Live Video in Full Screen
CR3C[7] = MVW horizontal zoom (doubling)
CR3C[6] = MVW vertical zoom (doubling)

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Note We will not support 4:1:1 linear from TV decoder, for design simplicity.

Memory data formats:
- 8bit and 16bit RGB, as in 5428.
- 4:1:1 Cinepak converted to 4.2:2 by writing a 4:2:2 Code-Book
first scan line -> Y0UY1V -> One 32bit Word

---

second scan line in memory -> Y2UY3V -> One 32bit Word
- 4.2:2 linear will be mapped in memory as follows:

first scan line Y0UY1V
first scan line Y2UY3V

---

consecutive data in the same scan line.

The tags that accompany the motion video data through the CRT-FIFO mark both the data format and the type of data inside the format (U/L for Y or U,V or mask for Y or U,V in Sashapak. Y0, Y1,U or V in 4.2:2)

Double Buffering for MVW Video Memory Data

In order to get a high quality Live Video full frames should be displayed at all times. This assumes that writing the video buffer and displaying it are in sync, which is normally not the case
To solve this problem and provide a simple interface between MVA h/w and the driver, Nordic will support a double buffer approach.

Addressing with Sashapack:
Sashapack stores data for eight scan-lines in one memory page (works only with synchronous DRAM-s) But due to U,V sub-sampling diferent data types are not read from memory uniformly.
On Y U/L the first four scan-lines read at offset 0 in the page, but the second four scan-lines read at offset 50H in the page.
On U,V U/L we read the same data for each scan-line. So we repeat reading the same data at all times, for eight scan-lines Page addresses to read are A0:EF. If the scan-line is shorter it will end sooner.
On Y Map the data should be sequential, scan-line oriented: first pixels 0 to 639 on the first scan line, than pixels 0 to 639 on the second scan line and so on till the 8-th scan line. If the lines have less than 640 pixels, Sasha wants them cropped for the first 4 scan lines, and then starting again from the half for the next four scan-lines. This is in sync with Y U/L where the last four scan-lines start from mid.
On U,V Map, because of the vertical subsampling, the same data is read for two scan lines, so there are four scan-lines worth of data but each scan-line is read for two consecutive scan-lines. Even if the scan-line is shorter, there will be a gap every-scan-line: there are fix page addresses for each scan-line up to 640 pixels wide.

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Memory data formats:
- 8bit and 16bit RGB, as in 5428.
- 4:1:1 Cinepak converted to 4:2:2 by writing a 4:2:2 Code-Book
first scan line -> Y0UY1V -> One 32bit Word

second scan line in memory -> Y2UY3V -> One 32bit Word
- 4:2:2 linear will be mapped in memory as follows:
first scan line Y0UY1V
first scan line Y2UY3V

consecutive data in the same scan line.

The tags that accompany the motion video data through the CRT-FIFO mark both the data format and the type of data inside the format (U/L for Y or U,V or mask for Y or U,V in Sashapak, Y0, Y1,U or V in 4:2:2).

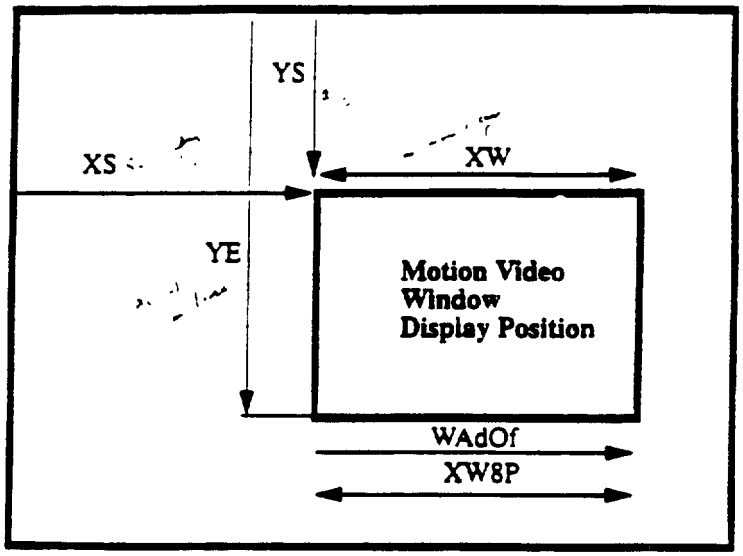
Double Buffering for MVW Video Memory Data

In order to get a high quality Live Video full frames should be displayed at all times. This assumes that writing the video buffer and displaying it are in sync, which is normally not the case
To solve this problem and provide a simple interface between MVA h/w and the driver, Nordic will support a double buffer approach.

Addressing with Sashapack:
Sashapack stores data for eight scan-lines in one memory page (works only with synchronous DRAM-s) But due to U,V sub-sampling diferent data types are not read from memory uniformly.
On Y U/L the first four scan-lines read at offset 0 in the page, but the second four scan-lines read at offset 50H in the page
On U,V U/L we read the same data for each scan-line. So we repeat reading the same data at all times, for eight scan-lines. Page addresses to read are A0:EF. If the scan-line is shorter it will end sooner.
On Y Map the data should be sequential, scan-line oriented: first pixels 0 to 639 on the first scan line, than pixels 0 to 639 on the second scan line and so on till the 8-th scan line. If the lines have less than 640 pixels, Sasha wants them cropped for the first 4 scan lines, and then starting again from the half for the next four scan-lines. This is in sync with Y U/L where the last four scan-lines start from mid.
On U,V Map, because of the vertical subsampling, the same data is read for two scan lines, so there are four scan-lines worth of data but each scan-line is read for two consecutive scan-lines. Even if the scan-line is shorter, there will be a gap every-scan-line: there are fix page addresses for each scan-line up to 640 pixels wide.

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Full Screen in a given graphics mode



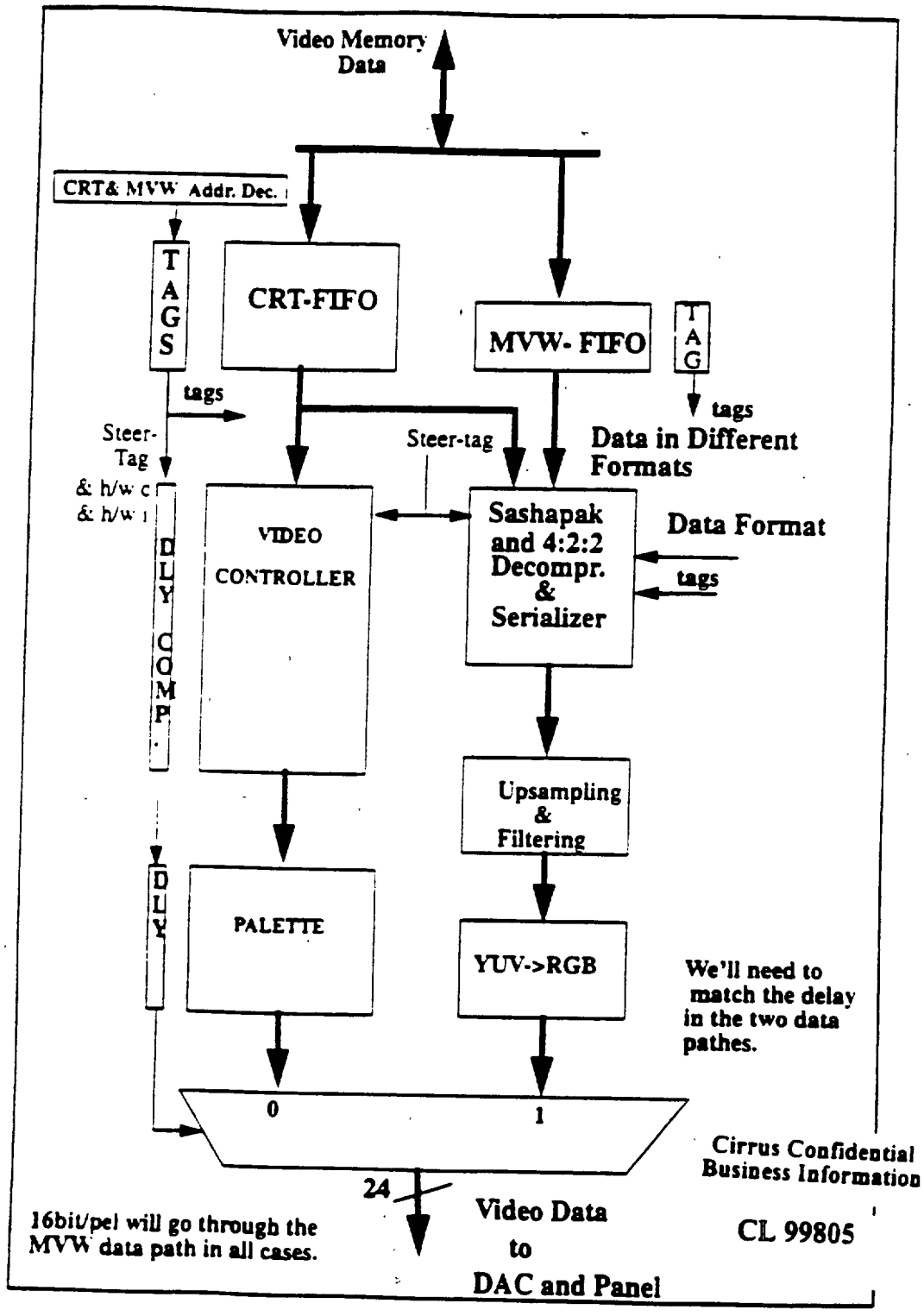
Where:

- **XS** = MVW Horizontal Start Coordinate (in surrounding pel depth memory cycles)
- **XW** = MVW Horizontal Width (MVW pel depth memory cycles)
- **YS** = Vertical MVW Start (in true scan-lines not affected by scan-line doubling or panel vertical expansion)
- **YE** = Vertical MVW End (all bits are programmed, in true scan lines)
- **WAdOf** = MVW Address Offset (a number to be added every line to the CRT Address Counter to allow it to jump over the MVW without counting through it.
- **XW8P** = MVW horizontal width expressed in 8 pixel units

Please note that MVW horizontal width is defined twice in different units:
XW defines it on the memory side in memory cycles
XW8P defines it on the CRT side in 8 pixel units.

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Video Memory Data
CRT& MVW Addr. Dec.
TAGS
CRT-FIFO
MVW- FIFO
TAG
tags
tags
Steer-Tag
& h/w c
& h/w
Steer-tag
Data in Different Formats
DLY COMP.
VIDEO CONTROLLER
Sashapak and 4:2:2 Decompr. & Serializer
Data Format
tags
Upsampling & Filtering
DLY
PALETTE
YUV->RGB
We'll need to match the delay in the two data pathes.
0
1
24
Video Data to DAC and Panel
16bit/pel will go through the MVW data path in all cases.
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5.0 Registers for Motion Video Architecture

5.1 CR34 - MVW XS Register

Bit	Definition
[7:0]	**MVW Horizontal Start Coordinate XS** (in surrounding pel depth memory cycles) The horizontal position is programmed with 8 pixel resolution (0,8,16,... pixels starting from the left side of the screen) (up to 1K pels in increments of 8 pels). To get an early warning, we will require **XS** to be programmed 8 pixels less than the actual position: 0 = zero, 1 = 16 pels, 2 = 24 pels, etc.

5.2 CR35 - MVW Horizontal Width XW Register

Bit	Definition
[7:0]	MVW Horizontal Width XW (MVW pel depth memory cycles) (up to 1K pels in increments of 8 pels). To get an early warning, we will require XW to be programmed 8 pixels less than the actual width: 0 = zero, 1 = 16 pels, 2 = 24 pels, etc. width.

5.3 CR36 - Vertical MVW High Position Register

Bit	Definition
[7]	Reserved
[6]	Cinepak type YUV to RGB conversion. If this bit = 0, YUV to RGB conversion is done according to the standard algorithm If this bit = 1, the YUV to RGB conversion is done based on Cinepak algorithm.
[5]	Excess 128 for YUV to RGB conversion. U and V are integer values expressed as two-th complement or excess 128. If this bit = 0, the YUV to RGB converter assumes that U and V are expressed in 2-th complement format (as in Philips SAA715B and SAA9051 TV Decoders). If this bit = 1, the YUV to RGB converter assumes that U and V are expressed in excess 128 format.
[4]	**MVW Memory Address Offset** (WMAdOf MSB)
[3:2]	**Vertical MVW End MSBs** (see CR37)
[1:0]	**Vertical MVW Start MSBs** (see CR38)

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5.4 CR37 - Vertical MVW Start Register

Bit	Definition
[7:0]	**Vertical MVW Start YS**: (in true scan-lines not affected by scan-line doubling or panel vertical expansion) 10 bits in CR36[1:0] (msbs) and CR37[7:0] (lsbs).

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5.5 CR38 - Vertical MVW End YE Register

Bit	Definition
[7:0]	**Vertical MVW End YE:** (all bits are programmed, in true scan lines) 10 bits in CR36[3:2] (msb-s) and CR38[7:0] (lsb-s).

5.6 CR39 - Surrounding Address Offset Register

Bit	Definition
[7:0]	**Surrounding Address Offset:** SAdOf (a number to be added every line to the surrounding CRT Address Counter value to allow it to jump over the MVW without counting through it. This allows calculating the surounding restart address.) This number depends on the surrounding mode resolution. Assuming a maximum line of 1024 pels, in increments of 4 pels per address (8-bits/pel), 256 addresses is enough for eight bits

5.7 CR3A - MVW Memory Address Start Register

Bit	Definition
[6 0]	**MVW Memory Address Start**: WMAdS in increments of 16KB = 4KW (a phisical address 00000.3FFFF for 1MB or 00000:7FFFF for 2MB Video Memory). Note that on the CPU side, this Start Address should be aligned at 16KB.

5.8 CR3B - MVW Memory Address Offset Register

Bit	Definition
[7 0]	**MVW Memory Address Offset** WMAdOf (A number to be added to the current MVW Start Address to get the next MVW start Address). Having this s/w model allows panning through a large image for the MVW. The actual image stored in memory may be as large as 2K pixels at 16 bits per pixel (two per word) -> 10bits. 10bits -> in CR36[5:4] (msb) and CR3B[7:0] (lsb).

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5.9 CR3C - MVW Pixel Format Register

Bit	Definition
[7]	**MVW horizontal zoom** (doubling)
[6]	**MVW vertical zoom** (doubling)
[5]	**Enable Live Video in Full Screen**
[4]	**Enable Motion Video Window**
[3:0]	Encode format for the first Motion Video Window as well as full screen graphics going through the MVA data path at 1x dot-clock frequency: 0h = 0000 = 8 bit RGB 3:3:2 direct (not through the palette), going through MVA 1h = 0001 = 16 bit RGB Sierra (5:5:5) (at 1x dot-clock frequency) 2h = 0010 = 16 bit RGB XGA (5:6:5) (at 1x dot-clock frequency) 3h = 0011 = 4:2:2 YUV Y0UY1V 4h = 0100 = Reserved for 4:1:1 YUV linear Y0Y1Y2Y3UV 5h = 0101 = Reserved for 4:1:1 YUV array Y0Y1Y2Y3UV but Y2Y3 are in next scan line 6h = 0110 = Sashapak 6 bits for U/L 7h = 0111 = Sashapak 8 bits for U/L 8h= 1000 = 24bit RGB through MVA (at 1x dot-clock frequency) 9h= 1001 = 8 bit RGB through the palette For improved quality of 8 bit/pel. A program can even update the palette during 8bit live video to get more colors. ah= 1100 = 8 bit direct color grey shaded (R=G=B=8bit grey shade) To be used for immage processing in the printing industry related applications. This mode Nordic can run at 1024x768 as any other 8bit/pel. Bh:Fh = 1001:1111 = reserved for future formats When a Motion Video Window is created data alwqays goes through the MVA data path. In this case anly the VGA Data Path can be used for the surounding data If no Motion Video Window, the MVA data path can be used to display full screen in any of the above formats. Especially for high pixel depth modes (24, 16bpp) it is recommended to use the MVA data path which runs at 1X dot-clock frequency and has a larger FIFO than the VGA Data Path. A full screen motion video window can be also defined that can be anywhere in memory and can run video or any application in the above formats.

5.10 CR3D - Motion Video Window Horizontal Size Register

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Bit	Definition
[7]	**MVA Data Bus Signature Generation Selection bit.** **0 = selects VGA Data Path for signatire generation** **1 = selects MVA Data Path for signature generation**
[6.0]	Motion Video Wondow width in 8 pixel units This register is used to specify the horizontal width of the MVW in 8 dot-clock

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units.
The MVW has to be a multiple of 8 pixels. The value programmed in this register is used to terminate the MVW on each scan line.

Preliminary Information

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6.0 Registers for Panel Horizontal Timing Control

This set of four registers are used to generate horizontal panel timing with 640x480 or 800x600 panels and to center horizontally a 640dots or 720dots picture on an 800x600 panel.

6.1 CR40 - No Center Panel HDE Start Register

Bit	Definition
[7:0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. This register is used to program Panel Line Clock Start and Panel Display Enable Start with both 640x400 and 800x600 panels any time no horizontal centering is needed. Used automatically by h/w if CR41 and CR42 are not used.

6.2 CR41 - Panel HDE Start Register to Center 720 dots

Bit	Definition
[7:0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 720 dot mode (text or graphics - RIX mode only) is centered on an 800x600 panel. If horizontal expansion is on, CR40 is used. Used automatically by h/w if : 800x600 panel & No 800x600 graphics mode & 8 dot character clock & no horizontal expansion

6.3 CR42 - Panel HDE Start Register to Center 640 dots

Bit	Definition
[7 0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 640 dot mode (text or graphics) is centered on an 800x600 panel. If horizontal expansion is on, CR40 is used. Used automatically by h/w if : 800x600 panel & No 800x600 graphics mode & (9 dot character clock + horizontal display enable >= 50H) & no expansion no horizontal expansion

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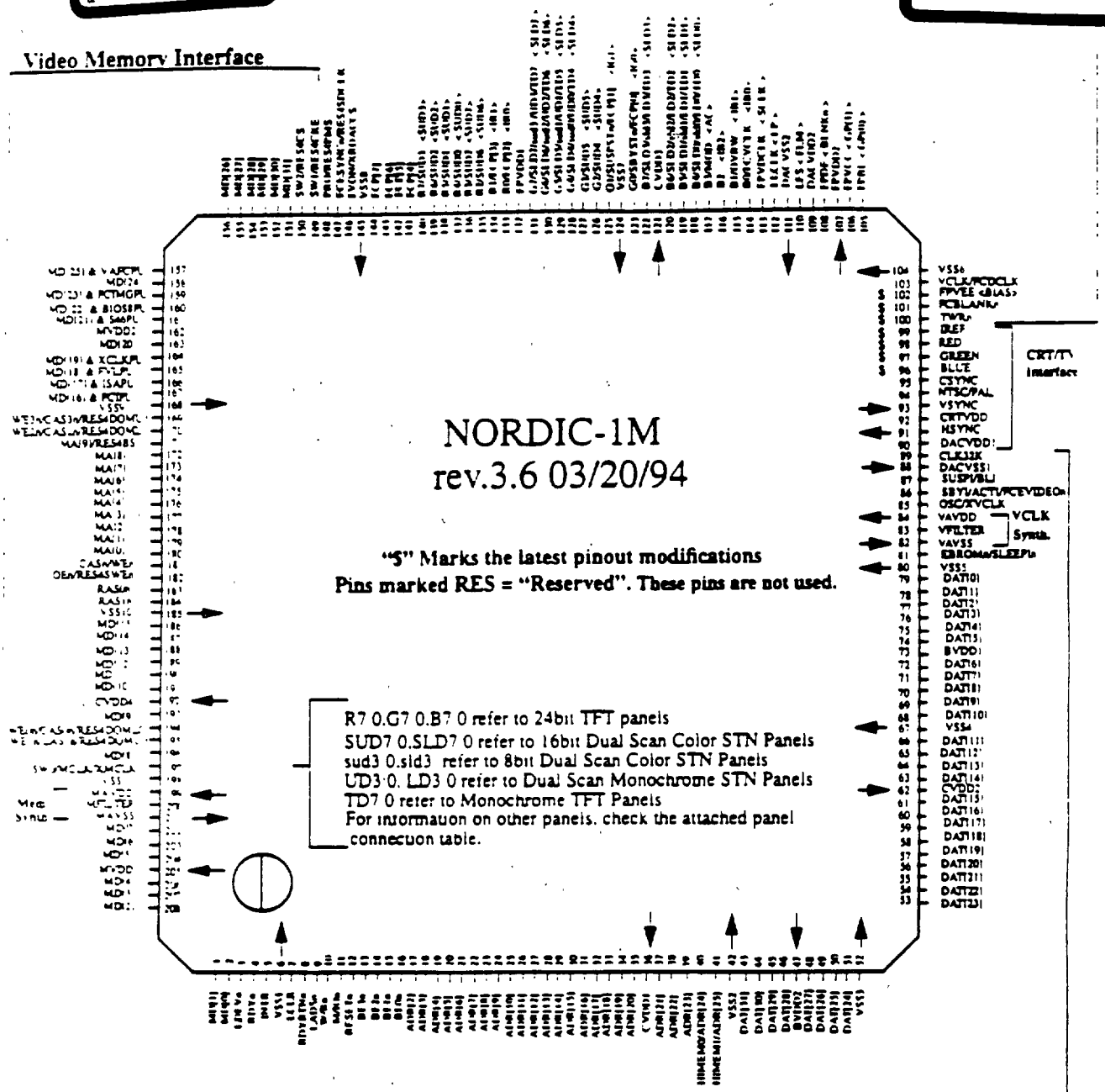
CL 99811

EXHIBIT
17
Dickinson

EXHIBIT
EX-465C

Panel & FC interface

Video Memory Interface



cpu interface

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DELTA LIST OVER PREVIOUS PINOUT RELEASED ON :

08/26/93:

- no POUT on SW2/POUT
- XVCLK moved from SW1/VCLK/XVCLK to OSC/XVCLK. This way SW1/VCLK/XVCLK became SW1/VCLK.

09/06/93

- All panel pins whose names were not starting with the color panel name were changed such that the names start now with the color panel pin (R7, G7, B7 and so on). So it was only a pin name change

09/12/93 rev. 1.0 and 1.1

1 Took-out Whisper Support Pins: WWRn, WRdn, WAD[3:0], FPCn.

2 Reduced the number of CPU Address Pins ADR[24:27] went-away. Use HIMEM to place the chip outside 16MB of memory for linear addressing.

3 Killed CRTVDD and placed CRT Interface on Host Bus VDD

4 Introduced VAFC pins in a unique pinout configuration in both VESA VL and PCI.
Added VAFCPU a pull-up to enable VAFC (VESA Advanced Feature Connector).
ADR[27:24] become VAFC pins, and R[7:4], G[7:6], CLK32K, SUSPI/BLI, SBYI/ACTI get a configuration for VAFC -> total 14 pins
SW0/VCLK will be used as VAFC DCLK, losing SW0 pin as panel type when VAFCPU is used.
In PCI bus no ADR pin will be shared with VAFC
ASW0PU will be added on MD pins to replace SW0 pin when VAFC is enabled by VAFCPU. SW0PU will read-back in the same register bit as SW0, so the BIOS will not feel any modification in the reporting scheme
The chip will draw more power in suspend with VAFC

5 Moved SW2, SW1/MCLK/XMCLK, the two RESERVED pins and TRWn on MVDD to prepare for SDRAM pin compatible option in the next Nordic that supports SDRAMs. It looks that we need only 3 more memory pins to support SDRAM-s so TRWn will not be used. It was moved so it is on the right VDD bus if needed

6 Moved CVDD3, VSS3, VCLK Synth, H/VSYNC, EROMn, SW0 per Thomas Hung's request to fit the floor plan.

09/21/93

1 Added AUXS1 on D/Cn as an option to be used with CS4231S as CS.
2 Added AUXS2 on EROMn/VADRn as an option to be used for Sound Synthesizer Chip Select.
3 Rearanged 5428 FC pins due to a previous error : R5 and R4 should not be used with FC.
- FCP[1:0] are shared with G7 and G6.
- SW2 and the two pins reserved for SDRAM were moved in between Video Memory pins and Panel pins and one of them is used as FCESYNCn.
- OVRWis shared with CLK32K. FCBLANKn is shared with SUSPI and FCEVIDEn is on SBYI.
4 Renamed the External Clock PU XCLKPU instead of XMCPU.

10/11/93 rev 1.3

1 Moved some external pull-ups.
2 Added alternate pin functions on panel pins as well as actual schematic name for engineering

10/27/93

1 Added TV-OUT (called also NTSC-OUT) pins on the panel pins

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10/28/93 rev 1.5 Modifications

1. Added TVG on EBROMn/AUXS2 and took out VADR as an option on this pin.
2. Put back FCESYNCn on RES4SDCLK as an option (deleted by mistake).

11/11/93 rev.2.0 Modifications

1. Reset became RESETn, active L to correspond with the defined reset signal for VESA VL and PCI.
2. TFT Panels Data Pins R7:R0, G7:G0, B7:B0 changed and all pins got rotated to get them ordered from right to left. Due to this change now Ri=TVRi, Gi=TVGi and Bi=TVBi.

01/06/94 rev 3.0 Modifications

1 Update Panel Data Pins based on Robin's Table
2 Move MOD pin on a Panel Data Pin used in 18bit TFT
3 Move OVRW on a 24bit Panel Data Pin
4 Removed pin configuration for TV-OUT support with digital encoders. All pins marked TV... were removed As a result, some pins like LLCLK, LFS, FPDE, FPVDCLK have one function now
5 Removed WavePort pins, including AUDVDD total 7 pins freed
AUX2 and TVG muxed on EBROMn are no longer needed either
6 Added one more CPU address pin: instead of HIMEM, Nordic has now HIMEM0 and HIMEM1, corresponding to CPU Address 24 and 25 or any other external decode of the high order CPU address bits. In the process of adding this pin, most CPU Interface pins on the right side were moved to the right by one pin
7 Added CRTVDD supplying HSYNC, VSYNC, CSYNC, NTSC/PAL CRT and TV Interfaces output buffers
8 EBROMn is shared with TVON, the power-on signal for AD720. So, in ISA bus with on chip BIOS support AD720 power on cannot be directly controlled by Nordic
9 Added pins for Analog TV Encoder support - AD720 and MC13[illegible]
   a CSYNC = Composite Sync signal
   b NTSC/PAL = 1 -> NTSC, 0-> PAL (for AD720, but it is TV Encoder Dependent)
   c EBROMn/TVON (see #8)
10 ASW0PU "Alternate Switch 0 Pull-Up" pull-up on pin 155 MD[26] was removed, as SW0 is now not multiplexed
11 De-multiplexed some of the pins previously multiplexed
   a Pin 168 TWRn/RES4PMS is now RES4PMS, a pin reserved for synchronous DRAM support
   b SUSPI/BLI/FCBLANKn is now SUSPI/BLI, not affected by the Feature Connector Enable Configuration
   c As a consequence of b, pin 97 is FCBLANKn (not muxed with anything). Please note that FCEVIDEOn is still muxed with SBYI/ACTI as before, as Standby Input and Keyboard Activity are less important functions in a system.
   d SW0 is no longer muxed on VCLK/FCDCLK. So VLK/FCDCLK is a pin but it moved to pin 103 in the PVDD area, to be consistent with FC power supply
12 SW1 muxed on MCLK/XMCLK (pin197) became SW0 This is just a name change to have the switches placed in a more consistent manner

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13 SW1 is now muxed with a reserved pin: RES4CKE. pin 148. which before was totally reserved. The idea here is to go for pu/pd with SDRAM-s for SW2 and SW1. while keeping SW0 on MCLK even with SDRAM-s.

14 Pin 147 is Reserved. It is actually one of the WavePort pins. but placed in-between Memory and Panel VDD busses (on MVDD) for maximum flexibility. To acheive this. the pins on its right were moved to the right by one FPVEE <BIAS> moved down to pin 98 (it was 105).

15 TRWn is now by itself on pin 96. on FPVDD

16 The names of all flat panel data pins reflect the panel type table attached to this document

01/13/94 rev. 3.1 Modifications

1. On EBROMn/TVON -> EBROMn/SLEEPIn with SLEEPIn an input which if L puts Nordic to sleep (as 3C3[0] and 46E8(3).
2. TVON is now on RES. but TVON/RES is pin 146 and FCESYNCn/RES4SDCLK is pin 147

01/22/94 rev. 3.2 Modifications

1. Pin 148. RES4PMS which was a pin reserved for synchronous DRAM-s. got a function: it is now a programable output PRO and it is on FPVDD instead of MVDD. The intention is to optionally use this pin to control a switch between 5V and 3.3V. in which case a H level of 5V is desirable. My primary choice for this function is actually NTSC/PAL pin which is on CRTVDD. but if the TV-OUT option is used in a system and a switch between 5 and 3.3V is provided. PRO may be used

02/05/94 rev. 3.3 Modifications

1. Updated panel interface table with correct Nordic pin numbers. The pins shifted a bit in the last rev but the panel interface table was not updated.

02/28/94 rev. 3.4 Modifications

1 TVON pin can be configured as XRDACCS "External RAMDAC Chip Select". H if access to 3C6.3c9 but not for 3C7 IORd. otherwise L. This way Nordic can support External RAMDAC through the feature connector and generate a chip select for it. so that with minimal external logic a RAMDAC IORD and IOWR can be generated. In previous versions. EBROMn could be used as External RAMDAC Chip Select only in ISA. because in any other bus configuration EBROMn became SLEEPIn input. SR25[6] configures TVON pin as XRDACCS. At POST this bit is TVON but it is reset to L. so in both TV-OUT systems and External RAMDAC systems. this bit will have no effect untill we need it to (in both cases the pin is active H). CL 99787

2 TWRn pin name was wrong (was TRWn).

03/06/94 rev. 3.5 Modifications

1. PCINBPU (PCI NO_Burst Pull-Up) was replaced by PCIMGPU (PCI Memory_Grant Pull-Up) on MD[23]. GRE[4] enables PCI Burst and the default is disabled. A pull-up on PCIMGPU extends Mem_Gnt value from 250nsec to 500nsec. giving more time to Nordic to execute a Burst Cycle without retry. If PCIMGPU pull-up is hooked to MD[23]. PCIPU is no longer needed. as both select PCI bus. This saves the need for two external pull-ups in PCI: only one external pull-up is needed to select PCI bus with reduced (MD16) or extended (MD23) Min-Gnt Value.

03/20/94 rev. 3.6 Modifications

1. For RAMDAC Layout related reasons. IREF. RED.GREEN and BLUE moved down three pins. FPVEE. FCBLANKn and TWRn moved up to fill the gap. No funcuonal change.

Panel Interface Data Formats (compatible with 62xx family except 18/24 bit TFT)

TFT 24/ 18/ 12/ 9 bit Name	Pin	DB44#	STN Color 16bit/8bit	Monochrome dual STN / single TFT
R7/R5/R3/R2	140	(13)	SUD3 / ---	---
R6/R4/R2/R1	139	(14)	SUD2 / ---	---
R5/R3/R1/R0	138	(15)	SUD1 / ---	---
R4/R2/R0	137	(16)	SUD0 / ---	---
R3/R1	136	(9)	SUD7 / ---	---
R2/R0	135	(10)	SUD6 / ---	---
R1	134		---	---
R0	133		---	---
G7/G5/G3/G2	131	(8)	SLD7 / sud3	UD3 / TD7
G6/G4/G2/G1	130	(7)	SLD6 / sud2	UD2 / TD6
G5/G3/G1/G0	129	(6)	SLD5 / sud1	UD1 / TD5
G4/G2/G0	128	(5)	SLD4 / sud0	UD0 / TD4
G3/G1	127	(11)	SUD5 / ---	---
G2/G0	126	(12)	SUD4 / ---	---
G1	125		---	---
G0	123		---	---
B7/B5/B3/B2	122	(4)	SLD3 / sld3	LD3 / TD3
B6/B4/B2/B1	120	(3)	SLD2 / sld2	LD2 / TD2
B5/B3/B1/B0	119	(2)	SLD1 / sld1	LD1 / TD1
B4/B2/B0	118	(1)	SLD0 / sld0	LD0 / TD0
B3/B1	117		MOD	MOD
B2/B0	116		---	---
B1	115	(23)	---	---
B0	114		---	---
FPVDCLK	113	(18)	SCLK / XCLKL	SCLK
LLCLK	112	(35)	LP	LP
LFS	110	(22)	FLM	FLM
FPDE	108	(26)	--- / XCLKU	--- / DE

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CL 99788

CIRRUS LOGIC®

CL-GD7542 (Nordic)
LCD VGA Controller



NORDIC

PRELIMINARY DATA BOOK

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CL 28423

CL-GD7542 (Nordic) Version History

Revision 1.0.1 – May 19, 1994

Revision 1.0.2 – June 20, 1994

Revision 1.1 – August 26, 1994

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CL-GD7542

Preliminary Data Book

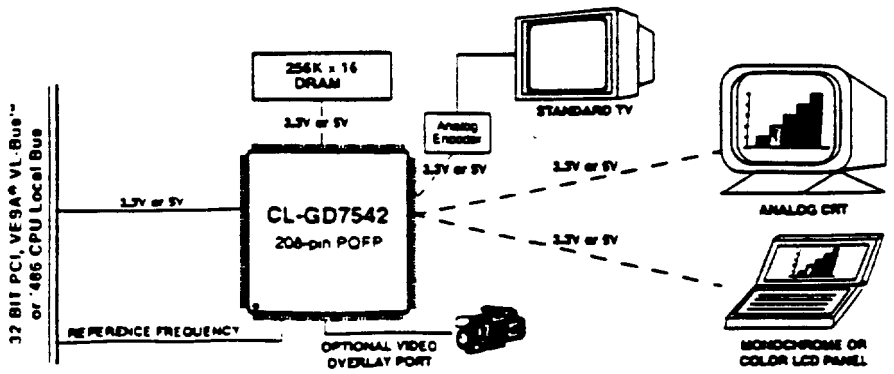
CIRRUS LOGIC®

GUI-Accelerated SVGA LCD Controller with MVA™ Multimedia for Portable Computers

FEATURES

- **Single-chip Super VGA LCD controller**
  - Based upon industry-leading CL-GD542X desktop VGA
  - BIOS and drivers optimized from CL-GD542X code
  - IBM® VGA hardware-compatible
- **GUI acceleration**
  - BitBLT (bit block transfer) engine
  - Color expansion for 8- or 16-bit pixels
  - True packed-pixel addressing for 4-, 8-, and 16-bpp
  - Programmable linear memory addressing
  - 32 x 32 or 64 x 64 hardware cursor
- **Multimedia acceleration and enhancement**
  - MotionVideo™ Architecture (MVA™)
    - True-color, full-motion video playback
    - Multi-format frame buffer
    - Integrated YCrCb: RGB color space converter
    - 2x horizontal/vertical hardware zoom
  - 8-bit feature connector port or video overlay
  - Interface to analog encoders for NTSC/PAL-out
- **64 x 64 pixel size hardware pop-up icons**
  - Displays up to four independently controlled, 4-color icons
- **32-bit direct-connect CPU host bus interfaces**
  - '486 CPU local bus (up to 50 MHz @ 5V)
  - VESA® VL-Bus™
  - PCI system bus with burst support
    - Big-endian byte-order hardware support for PowerPC
- **Scalable 1- and 2-Mbyte display memory**
  - 32-bit-wide interface to display memory
  - Two or four 256K x 16 DRAMs, or four 512K x 8 DRAMs
- **Integrated programmable frequency synthesizer**
  - VCLK up to 85 MHz @ 5V, 65 MHz @3.3V
  - MCLK up to 50 MHz @ 5V, 45 MHz @ 3.3V
- **Integrated 24-bit true-color RAMDAC™**
  - 640 x 480 non-interlaced, 16M colors
  - 800 x 600 non-interlaced, 64K colors
  - 1024 x 768 non-interlaced, 256 colors
  - 1280 x 1024 interlaced, 256 colors
- **640 x 480 and 800 x 600 LCDs**
  - Dual-scan color and monochrome STN LCDs
  - Color-active matrix LCDs (9-, 12-, 18-, and 24-bit interfaces)
  - Active addressing LCDs
  - Dithering algorithm automatically adds up to 6 bits-per-primary color without decreasing spatial resolution
  - Enhanced frame-rate modulation algorithm improves display quality with fast-response STN LCDs (~100 ms)
  - SimulSCAN™ (simultaneous CRT and LCD)
- **Power-management capabilities**
  - 3.3V, 5.0V, and mixed-voltage operation
  - Hardware suspend input pin or software suspend option
    - Self-refresh DRAMs or DRAM refresh via 32-kHz clock
  - Internal timers for Standby mode and backlight control
  - LCD power sequencing
  - VESA® DPMS (Display Power Management Signaling)
  - DDC-1 (Display Data Channel) support
- **EIAJ Standard 208-pin plastic quad flat package**

Functional Block Diagram



CIRRUS LOGIC®

CL-GD7542

Super VGA LCD Controller

OVERVIEW

The CL-GD7542 GUI-accelerated SVGA LCD controller with MotionVideo™ provides the performance and integration required for the next generation of mid-range to premium portable computers. Features of the CL-GD7542 include BitBLT GUI acceleration, 800 x 600 LCD support, true-color capability, and mixed-voltage operation for low power consumption. A complete graphics subsystem can be built using only three active components: the CL-GD7542 and two DRAMs.

System manufacturers can further differentiate their portable products by taking advantage of the video multimedia enhancement and acceleration capabilities of the MotionVideo architecture, live-video overlay, and, with an external analog encoder, video output support offered for the following standards:

- NTSC (National Television System Committee)
- PAL (Phase-Alternation Line)

ADVANTAGES

Unique Features	*Benefits*
High Performance —	
■ BitBLT engine, color expansion, hardware cursor, linear addressing, and 32-bit memory interface	❒ Accelerates GUIs such as Microsoft® Windows™; provides high resolution and color-depth capabilities.
■ 32-bit local bus interfaces, operating up to 33 MHz, includes support for PCI with burst mode	❒ Increases system throughput; PCI interface allows use in X86, PowerPC™, or other platforms.
■ Hardware 'pop-up' icons	❒ Provides hot-key display for on-screen symbols such as battery fuel gauge, contrast/brightness controls, etc.
Multimedia —	
■ MVA (MotionVideo™ Architecture)	❒ Enhances video playback capabilities to support up to 30 fps with 24-bpp color quality.
■ Multi-format frame buffer and YCrCb-to-RGB color space conversion	❒ Displays separate graphics and video windows at independent color depths.
■ 2x hardware zoom for playback	❒ Enlarges video clips with little or no frame rate reduction.
■ 8-bit VAFC port	❒ Allows live 'TV in a window' capability.
■ Interface to NTSC/PAL analog encoders	❒ Integrated design can be developed to display computer-generated data on a TV or record to a VCR.
Enhanced LCD Support —	
■ 800 x 600 LCD support (both TFT and dual-scan STN) with comprehensive resolution-compensation support	❒ Supports latest LCD technology and enables full use of the display area whether in graphics or text mode.
■ Enhanced frame-rate modulation	❒ Improves display quality; reduces crosstalk, ghosting, and cursor 'submarining'.
■ Intelligent dithering algorithm expands the number of input bits per R, G, and B on TFT or STN LCDs	❒ Displays high- and true-color modes with smooth shading (no contouring) on all supported LCD types.
Power Management —	
■ 3.3V, 5.0V, or mixed-voltage support	❒ Minimizes operating power consumption; provides manufacturing flexibility
■ Hardware-initiated Standby and Suspend modes and VESA® DPMS support for CRTs	❒ Reduces power consumption; supports Energy Star monitors for 'green PC' compliance.
Design Flexibility —	
■ VGA controller with integrated RAMDAC, dual-frequency clock synthesizer in a 208-pin PQFP	❒ Minimizes chip count and board space required for the display subsystem.
■ Big-endian byte ordering in display memory with PCI host interface	❒ Supports X86 designs with little-endian data, supports PowerPC™ designs with big-endian data.
Software —	
■ Drivers supplied for 3D-graphics libraries and emerging APIs (advanced programming interface) for games	❒ Supports emerging standards for Windows-based 3D applications

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Software Support

Operating System and Application Software Drivers

Software Drivers[a]	Resolution Supported	Number of Colors
Microsoft®/Intel® DCI v1.4	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	256 colors 16 and 256 colors 65,536 colors 16.8 million colors
Microsoft® Windows™ v3.1	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	256 colors 16 and 256 colors 65,536 colors 16.8 million colors
Microsoft® Windows NT™ v3.1 (currently for 'X86; future for PowerPC™)	640 x 480, 800 x 600, 1024 x 768	16 and 256 colors
OS/2™ v2.0, v2.1	640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	16 and 256 colors 65,536 colors 16.8 million colors
AutoCAD® v11, v12	640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	16 and 256 colors 65,536 colors 16.8 million colors
Autoshade® v2.0 3D Studio® v1, v2	640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	256 colors 65,536 colors 16.8 million colors

[a] Driver support for additional applications is provided by independent software vendors, either with specific drivers or through VESA mode support. In many instances, existing drivers for the CL-GD542X can be used with the CL-GD7542. For more information concerning driver support, contact the software manufacturer.

BIOS

Feature	Benefit
■ Available as 48-Kbyte BIOS to provide optimum performance with VGA and VESA® extended mode support, or as a 32-Kbyte subset with a 16-Kbyte-relocatable module or loaded as TSRs (terminate and stay resident)	❒ Provides system design options for the best combination of performance and functionality.
■ Fully IBM® VGA-compatible BIOS	❒ Ensures compatibility with the existing base of PC applications
■ VESA® VBE (video BIOS extensions) 1.2 and PM (power management) support	❒ Compatible with industry standard for extended mode support beyond VGA and power-management control.

Software Utilities

Utility	Function
CLPane	LCD parameter optimization utility for OEM development use
OEMSI	BIOS-customization utility for OEM development use
PCLRegs	VGA controller register viewer/editor for OEM development use
Switcher	Video configuration TSR (terminate and stay resident)
CLMode	Video mode and video display configuration utility suitable for end-use distribution (includes foreign language translations)
WinMode	Windows™ application for graphic mode and display type configuration (includes foreign language translations, selectable from within the utility)
AutoResolution Switching	Windows™ application for automatically switching display resolutions (for example, from a 1024 x 768 CRT to lower-resolutions 640 x 480 or 800 x 600 LCDs) without relaunching Windows™

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1. Pin Definitions and Block Diagrams

1.1 Pin Definitions

1.1.1 Pin-Out Diagram

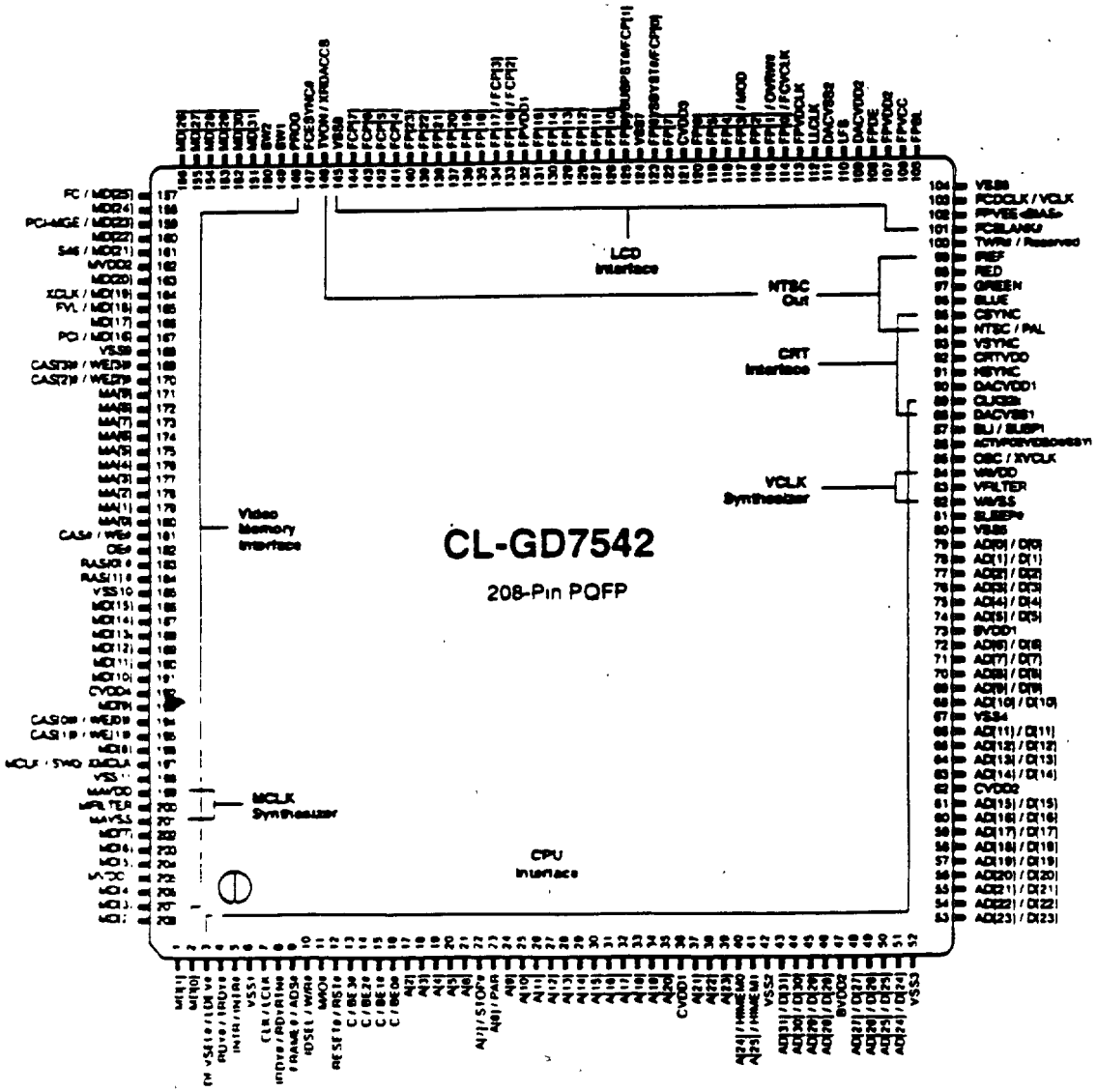


Figure 1–1. Pin-Out Diagram

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1.1.2 Pin Table

Table 1–1. Pins, by Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	MD[1]	37	A [21]	73	BVDD1
2	MD[0]	38	A [22]	74	D [5]
3	DEVSEL# / LDEV#	39	A [23]	75	D [4]
4	TRDY# / RDY#	40	HIMEM0	76	D [3]
5	INTR / INTR#	41	HIMEM1	77	D [2]
6	VSS1	42	VSS2	78	D [1]
7	CLK / LCLK	43	D [31]	79	D [0]
8	IRDY# / RDYRTN#	44	D [30]	80	VSS5
9	FRAME# / ADS#	45	D [29]	81	SLEEP# / EBROM#
10	IDSEL# / W/R#	46	D [28]	82	VAVSS
11	M/IO#	47	BVDD2	83	VFILTER
12	RESET#	48	D [27]	84	VAVDD
13	C / BE3#	49	D [26]	85	OSC
14	C / BE2#	50	D [25]	86	SBYI / ACTI / FCEVIDEO#
15	C / BE1#	51	D [24]	87	SUSPI / BLI
16	C / BE0#	52	VSS3	88	DACVSS1
17	A [2]	53	D [23]	89	CLK32K
18	A [3]	54	D [22]	90	DACVDD1
19	A [4]	55	D [21]	91	HSYNC
20	A [5]	56	D [20]	92	CRTVDD
21	A [6]	57	D [19]	93	VSYNC
22	A [7] / STOP#	58	D [18]	94	NTSC / PAL
23	A [8] / PAR	59	D [17]	95	CSYNC
24	A [9]	60	D [16]	96	BLUE
25	A [10]	61	D [15]	97	GREEN
26	A [11]	62	CVDD2	98	RED
27	A [12]	63	D [14]	99	IREF
28	A [13]	64	D [13]	100	Reserved
29	A [14]	65	D [12]	101	FCBLANK#
30	A [15]	66	D [11]	102	FPVEE
31	A [16]	67	VSS4	103	VCLK / FCDCLK
32	A [17]	68	D [10]	104	VSS6
33	A [18]	69	D [9]	105	FPBL
34	A [19]	70	D [8]	106	FPVCC
35	A [20]	71	D [7]	107	FPVDD2
36	CVDD1	72	D [6]	108	FPDE

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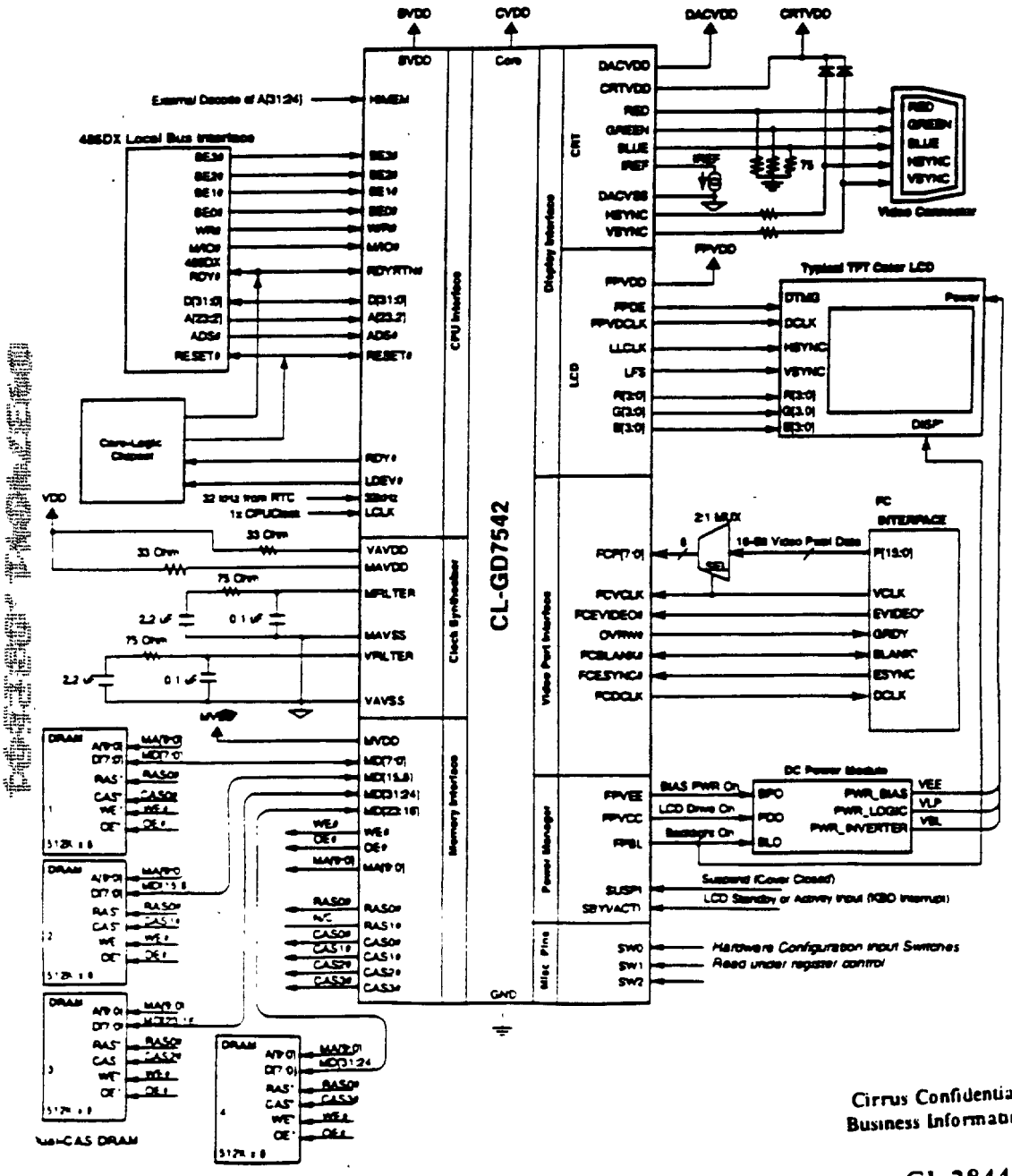
Table 1–1. Pins, by Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
109	DACVDD2	143	FCP [6]	177	MA[3]
110	LFS	144	FCP [7]	178	MA[2]
111	DACVSS2	145	VSS8	179	MA[1]
112	LLCLK	146	TVON / XRDACCS	180	MA[0]
113	FPVDCLK	147	FCESYNC#	181	CAS# / WE#
114	FP [0] / FCVCLK	148	PROG	182	OE#
115	FP [1] / OVRW#	149	SW1	183	RAS[0]
116	FP [2]	150	SW2	184	RAS[1]
117	FP [3] / MOD	151	MD[31]	185	VSS10
118	FP [4]	152	MD[30]	186	MD[15]
119	FP [5]	153	MD[29]	187	MD[14]
120	FP [6]	154	MD[28]	188	MD[13]
121	CVDD3	155	MD[27]	189	MD[12]
122	FP [7]	156	MD[26]	190	MD[11]
123	FP [8] / SBYST# / FCP[0]	157	MD[25] / VAFC	191	MD[10]
124	VSS7	158	MD[24]	192	CVDD4
125	FP [9] / SUSPST# / FCP[1]	159	MD[23] / PCI-MGE	193	MD[9]
126	FP [10]	160	MD[22]	194	WE[0]# / CAS[0]#
127	FP [11]	161	MD[21] / S46	195	WE[1]# / CAS[1]#
128	FP [12]	162	MVDD2	196	MD[8]
129	FP [13]	163	MD[20]	197	SW0
130	FP [14]	164	MD[19]	198	VSS11
131	FP [15]	165	MD[18] / FVL	199	MAVDD
132	FPVDD1	166	MD[17]	200	MFILTER
133	FP [16]	167	MD[16] / PCI	201	MAVSS
134	FP [17]	168	VSS9	202	MD[7]
135	FP [18]	169	WE[3]# / CAS[3]#	203	MD[6]
136	FP [19]	170	WE[2]# / CAS[2]#	204	MD[5]
137	FP [20]	171	MA[9]	205	MVDD1
138	FP [21]	172	MA[8]	206	MD[4]
139	FP [22]	173	MA[7]	207	MD[3]
140	FP [23]	174	MA[6]	208	MD[2]
141	FCP [4]	175	MA[5]		
142	FCP [5]	176	MA[4]		

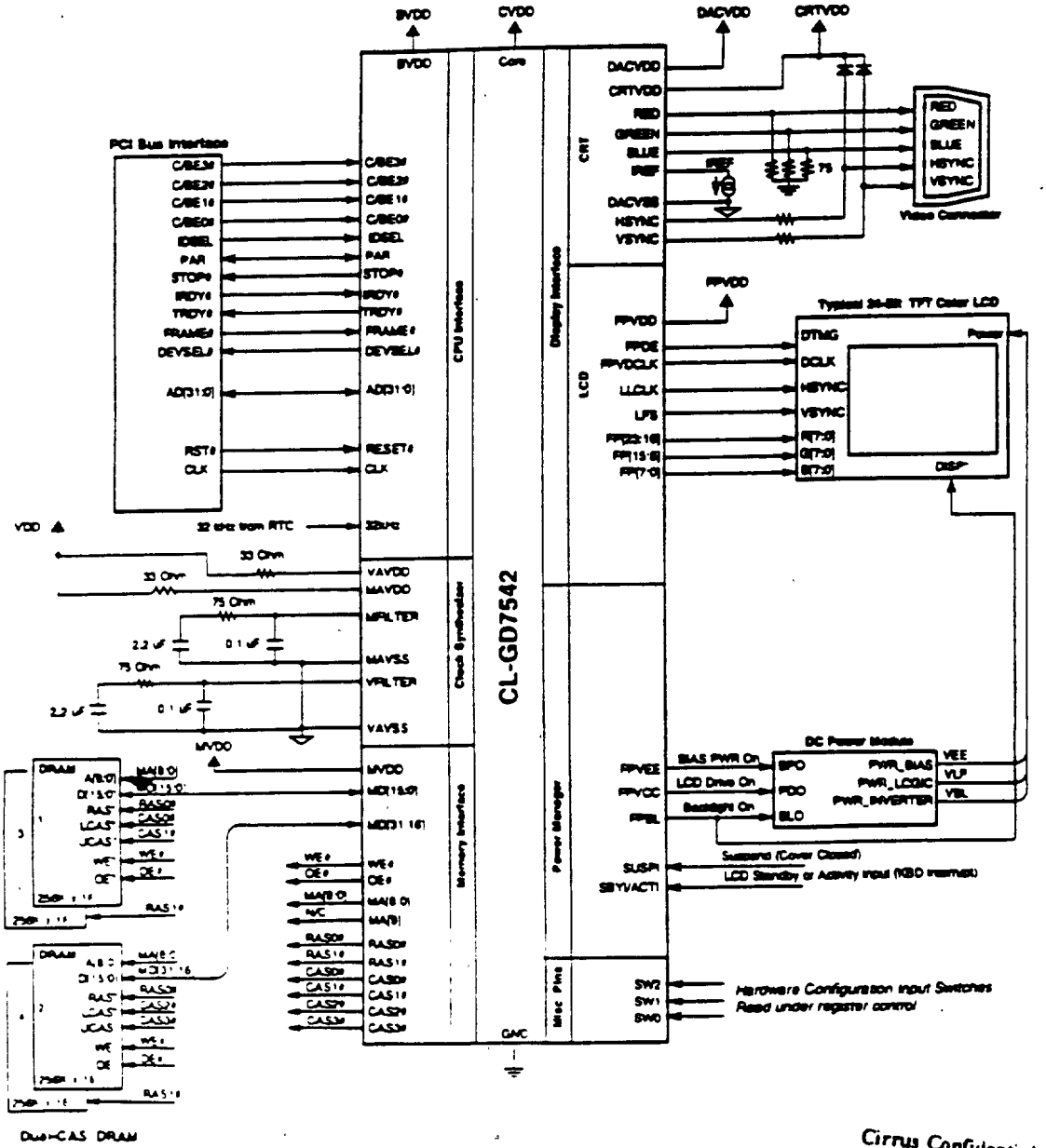
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1.2 Block Diagrams: LCD Interfaces to CL-GD7542

1.2.1 TFT (512-Color) to 486DX or VESA 32-Bit Local Bus, 2-Mbyte 512K x 8 DRAM, Video Port



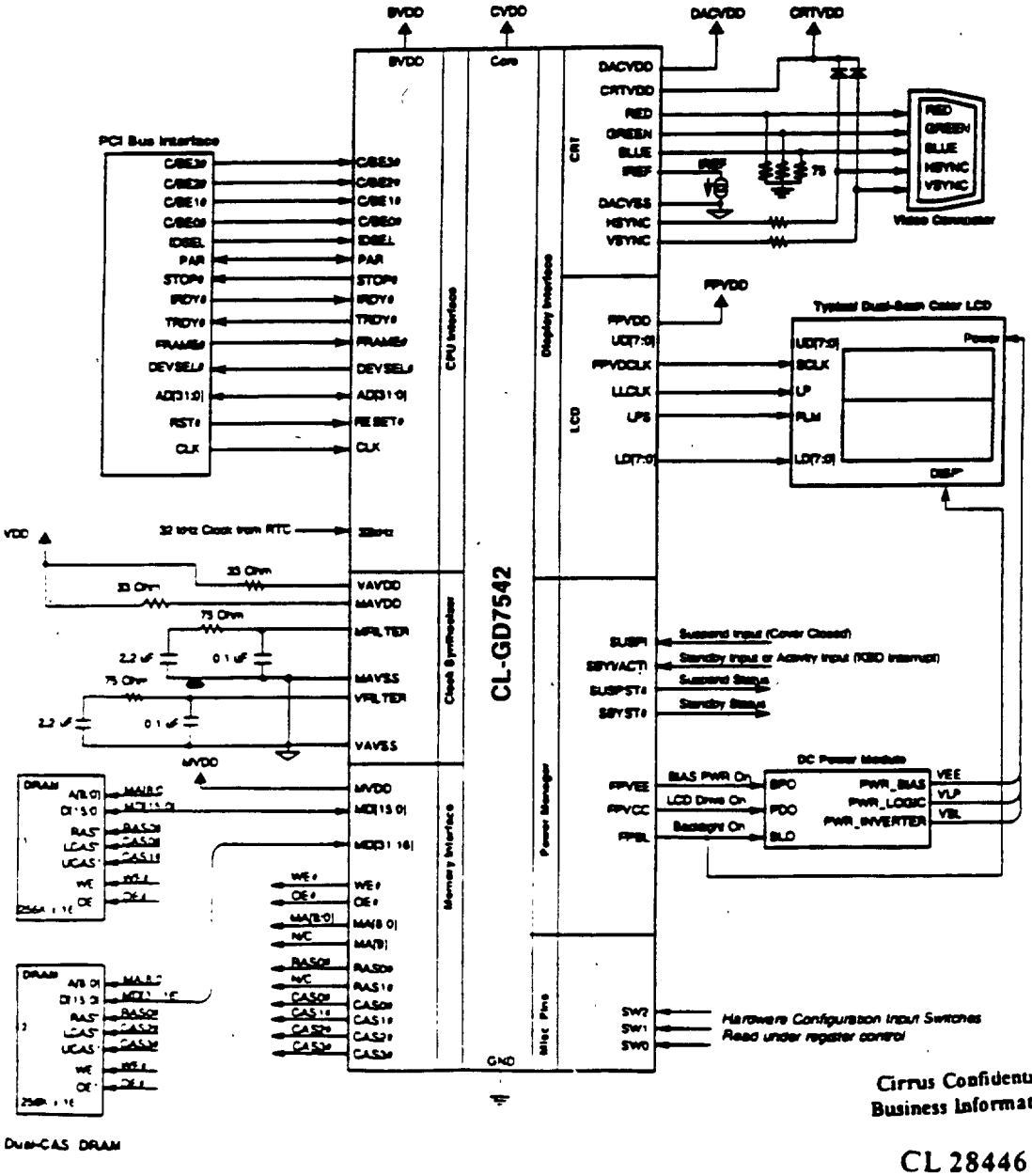
1.2.2 TFT (24-Bit Color) to PCI Bus, 2-Mbyte 256K x 16 DRAM.



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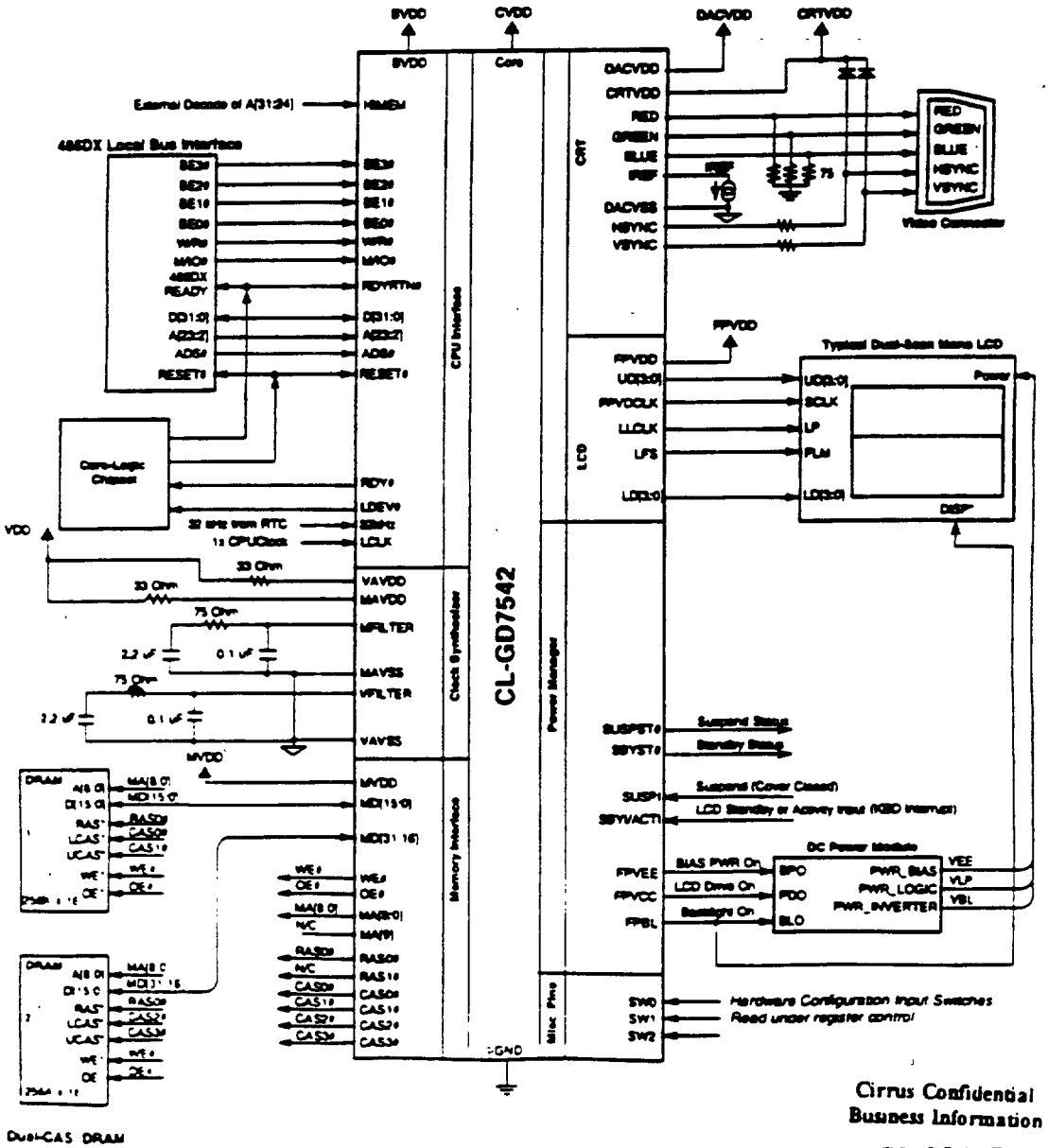
1.2.3 Dual-Scan Color (16-Bit) to PCI Bus, 1-Mbyte 256K x 16 DRAM.



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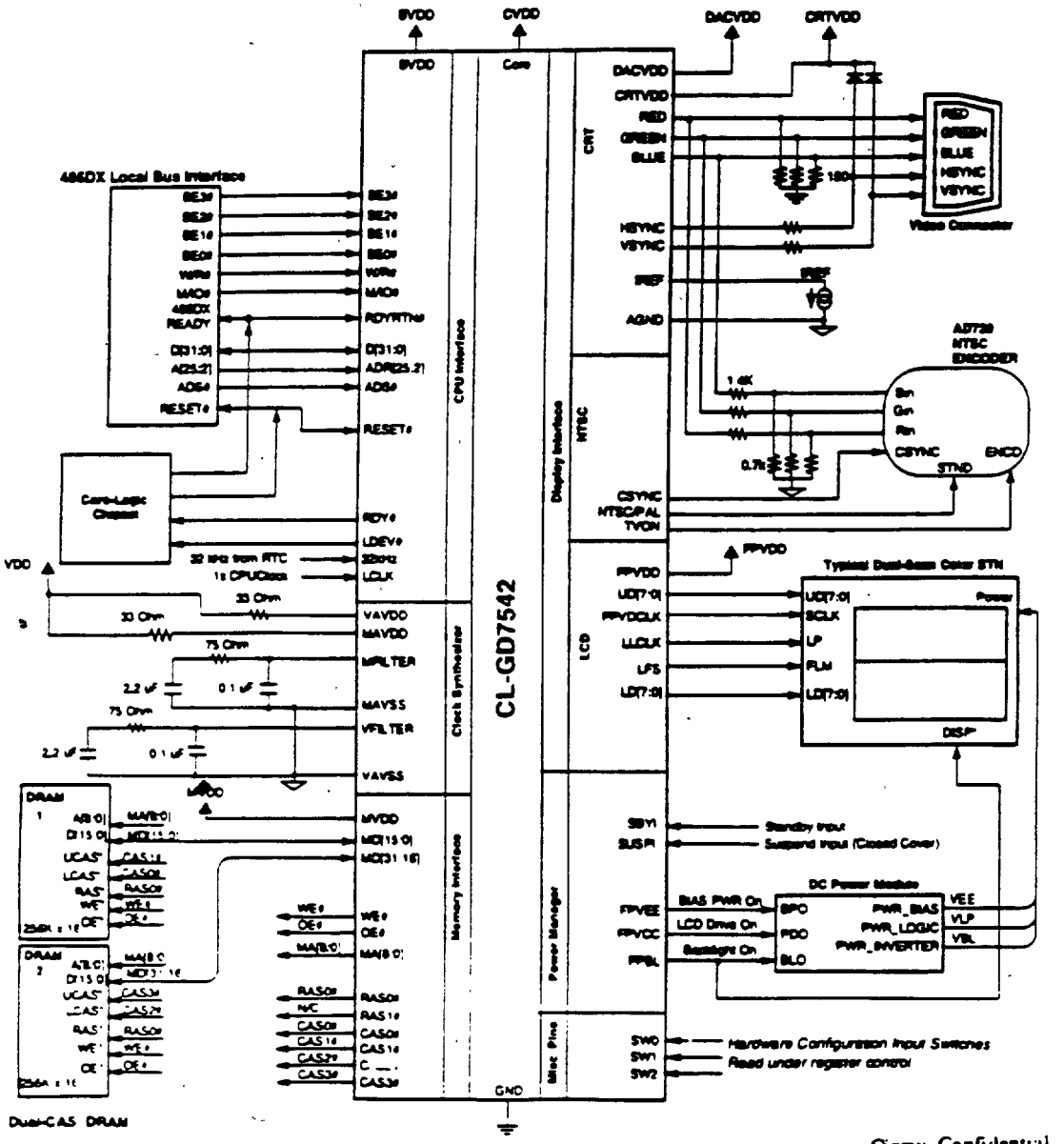
1.2.4 Dual-Scan Mono (8-Bit) to 486DX or VESA 32-Bit Local Bus, 1-Mbyte 256K x 16 DRAM



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1.2.5 Dual-Scan Color (16-Bit) to 486DX or VESA 32-Bit Local Bus, 1-Mbyte 256K x 16 DRAM, NTSC Output



Note

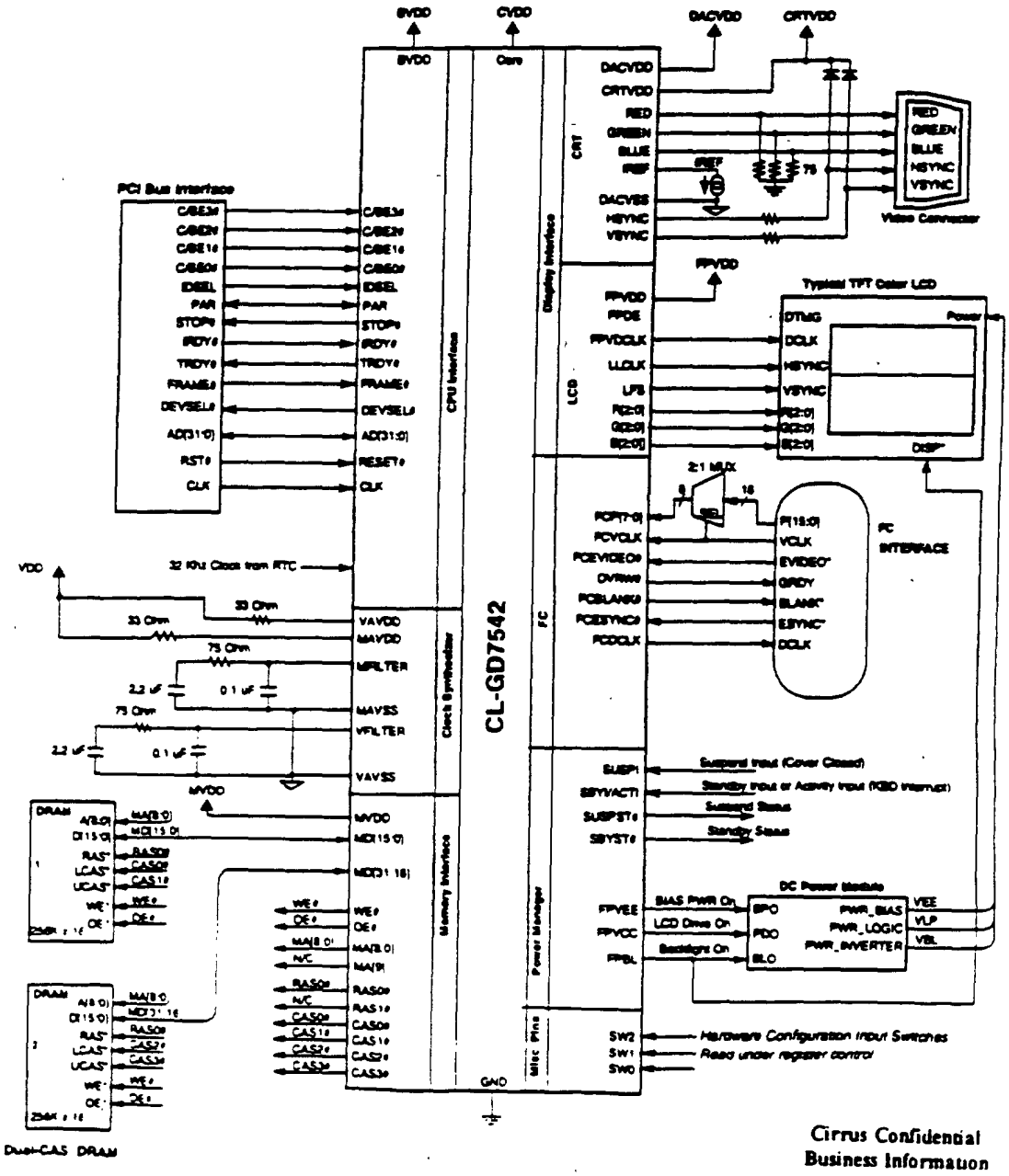
In this diagram the CRT must be disconnected when using the NTSC output

This diagram illustrates general signal connections. All information is preliminary and subject to change. For detailed design examples, refer to the CL-GD7542 Application Handbook

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1.2.6 TFT (9-Bit Color) to PCI Bus, 1-Mbyte 256K x 16 DRAM, FC Interface



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2. Detailed Pin Descriptions

The following abbreviations are used for pin types in the following sections:

- (I) indicates Input
- (O) indicates Output
- (I/O) indicates a bidirectional function
- (I or 0) indicates either an Input or Output function, depending on the mode
- (OC) indicates Open-Collector Output
- (3-S) indicates 3-State Output
- (#) indicates active-low function

2.1 Host Interface Pins — VESA Local Bus and PCI Bus Pin Identification

As explained in this section, a number of bus interface pins are defined according to the local bus type to which the CL-GD7542 is connected.

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2.1.1 Host Interface – '486 or VESA Local Bus Pins

Pin Name	Pin No.	Type	Local Bus Name/Description
A[23:2]	39:37 35:17	I	**ADDRESS [23:2]:** These inputs are used to select the resource to be accessed during memory or I/O operations.
BE[3:0]#	13:16	I	**BYTE ENABLE[3:0]#:** These active-low inputs are connected directly to the corresponding CPU byte-enable output.
D[31:0]	43:46,48:51 53:61,63,66 68:72,74:79	I/O	**DATA [31:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. For the VESA Local Bus or '486 32-bit Local Bus, these pins are connected directly to D[31:0].
HIMEM[0:1] A[24:25]	40,41	I	**HIGH MEMORY [1:0]:** These active-high inputs are a decode of the upper CPU Address bits. Normally, these inputs are used as A[24:25]. However, they can be used as A[31:30] and leave 2 GBytes of upper address space for MPEG (Moving Picture Experts Group) and JPEG (Joint Picture Expert Group) boards.
INTR	5	3-S	**INTERRUPT REQUEST:** This active-high output indicates that the CL-GD7542 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. For a description of controls for this pin, refer to Register CR11[3:0].
ADS#	9	I	**ADDRESS DATA STROBE#:** This active-low input indicates that a new cycle has begun. The ADS# signal is generated from a decode of the CPU output signals, A[23:2] and M/IO#. This output will be low before the middle of the first timing (T2) cycle after ADS# goes low. This pin must be connected directly to the ADS# pin on the local bus.
LCLK	7	I	**LOCAL CLOCK:** This active-low input is the timing reference when the CL-GD7542 is connected to a '486 Local Bus. For the VESA Local Bus, this pin is connected to LCLK. For the '486 Local Bus, this pin is connected to CLK1X. If no CLK1X is available from the '486, CLK2 must be divided by two and tied to the CL-GD7542 LCLK pin, and clock skew must be less than 2.0 ns.
LDEV#	3	OC	**LOCAL BUS DEVICE#:** This open-collector output is driven low to indicate that the CL-GD7542 will respond to the current cycle This pin is connected to LDEV#

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2.1.1 Host Interface — '486 or VESA Local Bus Pins *(cont.)*

Pin Name	Pin No.	Type	Local Bus Name/Description
M/IO#	11	I	**MEMORY I/O#** This input indicates whether a memory or I/O operation is to occur. It must be connected directly to the M/IO# pin on the CPU. When M/IO# is high, a memory operation is selected. When M/IO is low, an I/O operation is selected.
RDY#	4	3-S	**READY#:** This active-low signal is used as an output to terminate a CL-GD7542 bus cycle. For VESA Local Bus, this pin is connected to the LRDY# pin. For the '486 Local Bus, this pin is connected to the RDY# pin.
RDYRTN#	8	I	**READY RETURN#:** This input establishes a handshake between the CL-GD7542 and VESA Local Bus so that the CL-GD7542 is informed when the cycle has ended. RDYRTN# typically goes low in the same LCLK cycle that LRDY# goes low. When LCLK is higher than 33 MHz, RDYRTN# may trail LRDY# by one LCLK cycle. During DMA or system I/O bus master operations, RDYRTN# goes low for one LCLK cycle when the DMA or system I/O bus masters command ends. For the VESA Local Bus, this pin is connected to RDYRTN#. For the '486 Local Bus, this pin is connected to RDY#.
RESET#	12	I	**RESET#:** This input, when low, initializes the CL-GD7542 to a known state. The trailing (rising) edge of this input loads the Configuration registers SR22[7:0] and SR24[7] with the data on MD[25:16] pins. The data on the MD[25:16] pins is determined either by internal pull-down resistors or optional external pull-up resistors. When RESET# is low, it forces all outputs to a high-impedance state, and it initializes all registers to their Reset state
SLEEP#	81	I	**SLEEP#:** This active-low input is used by the external hardware to put the CL-GD7542 into bus Sleep mode. When this input is low, the memory and I/O interface is disabled, and the displays are turned off. Once this pin is low, no other chip access is possible until this pin goes high.
W/R#	10	I	**WRITE/READ#:** This input indicates whether a write or read operation is selected by the CPU. It must be connected directly to the W/R# pin on the CPU. When W/R# is high, a write will occur. When W/R# is low, a read will occur

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2.1.2 Host Interface – PCI Bus Pins

Pin Name	Pin No.	Type	Local Bus Name/Description
AD[31:0]	43:46, 48:51, 53:61, 63:66 68:72,74:79	I/O	**ADDRESS AND DATA [31:0]:** These multiplexed, bidirectional pins are used to transfer system address and data during any memory or I/O operation on the PCI Bus. During the first clock of a transaction, these pins contain a 32-bit physical byte address. During subsequent clocks, they contain data. These pins directly connect to AD[31:0] of the PCI Bus.
C/BE#[3:0]	13:16	I or O	**COMMAND AND BYTE ENABLE#[3:0]:** These multiplexed pins are used to transfer Bus Command and Byte Enables during any memory or I/O operation on the PCI Bus. During the address phase of the operation, these pins define the bus command. (Refer to Table 2–1.) During the data phase, these pins are used as Byte Enable Outputs. C/BE#0 applies to Byte 0. C/BE#3 applies to Byte 3. These pins directly connect to C/BE#[3:0] of the PCI Bus.

Table 2–1. Command and Byte Enable#

C/BE#				Command Type	Comments
[3]	[2]	[1]	[0]		
0	0	0	0	Interrupt Acknowledge	–
0	0	0	1	Special Cycle	–
0	0	1	0	I/O Read	Valid
0	0	1	1	I/O Write	Valid
0	1	0	0	Reserved	–
0	1	0	1	Reserved	–
0	1	1	0	Memory Read	Valid
0	1	1	1	Memory Write	Valid
1	0	0	0	Reserved	–
1	0	0	1	Reserved	–
1	0	1	0	Configuration Read	Valid
1	0	1	1	Configuration Write	Valid
1	1	0	0	Memory Read Multiple	–
1	1	0	1	Dual Address Cycle	–
1	1	1	0	Memory Read Line	–
1	1	1	1	Memory Write and Invalidate	–

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2.1.2 Host Interface – PCI Bus Pins *(cont.)*

Pin Name	Pin No.	Type	Local Bus Name/Description
CLK	7	I	**CLOCK:** This is the timing reference for the CL-GD7542, when it is connected to a PCI Bus. This pin must be connected directly to the PCI Bus CLK pin.
DEVSEL#	3	OC	**DEVICE SELECT#:** This open-collector output is driven low to indicate that the CL-GD7542 will respond to the current cycle.
FRAME#	9	I	**FRAME#:** This active-low input indicates the beginning and duration of an access. FRAME# goes low to indicate the beginning of a bus transaction. While FRAME# is low, data transfers continue. The transaction is in its final data phase when FRAME# goes high.
IDSEL	10	I	**INITIALIZATION DEVICE SELECT#:** This active-high input signal is used as a chip select in lieu of the upper 24 address lines during configuration read and write cycles.
INTR#	5	3-S	**INTERRUPT REQUEST#:** This active-low output indicates that the CL-GD7542 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. It is controlled by register CR11[3:0].
IRDY#	8	I	**INITIATOR READY#:** This active-low input establishes a handshake between the CL-GD7542 and PCI Bus, so that the CL-GD7542 knows when the cycle has ended. Wait states are inserted until both IRDY# and TRDY# are low.
PAR	23	3-S	**PARITY:** This signal provides even parity across AD[31:0] and C/BE#[3:0]. The CL-GD7542 samples this signal during write cycles, and transmits the correct parity for read cycles.
RST#	12	I	**RST#:** This input, when low, initializes the CL-GD7542 to a known state. The trailing (rising) edge of this input loads the Configuration registers SR22[7:0] and SR24[7] with the data on MD[25:16], which is determined either by internal pull-down resistors or optional external pull-up resistors.
STOP#	22	3-S	**STOP#:** This active-low output indicates a current request to the PCI Bus Master to stop the current transaction.
TRDY#	4	3-S	**TARGET READY#:** This active-low signal is used as an output to terminate a CL-GD7542 bus cycle.

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2.2 Flat Panel LCD Interface Pins

The flat panel LCD interface is determined by the type of LCD flat panel used. Refer to the Cirrus Logic **CL-GD7542 Panel Interface Connection Table** in the *CL-GD7542 Applications Book* for specific connection information. Also, see Table 1-3 for LCD-vs-Pin cross-reference.

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[0]	114	O	B0	**24-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data Bit 0 (LSB) for 24-bit TFT color LCDs.
FP[1]	115	O	B1	**24-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data Bit 1 for 24-bit TFT color LCDs.
FP[2]	116	O	B2	**24-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data Bit 2 for 24-bit TFT color LCDs.
			B0	**18-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data Bit 0 (LSB) for 18-bit TFT color LCDs.
FP[3]	117	O	B3	**24-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data Bit 3 for 24-bit TFT color LCDs.
			B1	**18-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data Bit 1 for 18-bit TFT color LCDs.
FP[4]	118	O	B4	**24-BIT TFT BLUE BIT [4]:** This bit is BLUE Color Data Bit 4 for 24-bit TFT color LCDs.
			B2	**18-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data Bit 2 for 18-bit TFT color LCDs.
			B0	**12-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data Bit 0 (LSB) for 12-bit TFT color LCDs.
			SLD0	**16-BIT STN COLOR LOWER BIT [0]:** This bit is Lower Data Bit 0 (LSB) for 16-bit dual-scan and single-scan STN color LCDs.
			SLD0	**8-BIT STN COLOR LOWER BIT [0]:** This bit is Lower Data Bit 0 (LSB) for 8-bit dual-scan and single-scan STN color LCDs.
			LD0	**LOWER DATA [0]:** This bit is Lower Panel Data Bit 0 (LSB) for dual-scan STN monochrome LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[5]	119	O	B5	**24-BIT TFT BLUE BIT [5]:** This bit is BLUE Color Data Bit 5 for 24-bit TFT color LCDs.
			B3	**18-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data Bit 3 for 18-bit TFT color LCDs.
			B1	**12-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data Bit 1 for 12-bit TFT color LCDs.
			B0	**9-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data Bit 0 (LSB) for 9-bit TFT color LCDs.
			SLD1	**16-BIT STN COLOR LOWER BIT [1]:** This bit is Lower Data Bit 1 for 16-bit dual-scan and single-scan STN color LCDs.
			SLD1	**8-BIT STN COLOR LOWER BIT [1]:** This bit is Lower Data Bit 1 for 8-bit dual-scan and single-scan STN color LCDs.
			LD1	**LOWER DATA [1]:** This bit is Lower Panel Data Bit 1 for dual-scan STN monochrome LCDs.
FP[6]	120	O	B6	**24-BIT TFT BLUE BIT [6]:** This bit is BLUE Color Data Bit 6 for 24-bit TFT color LCDs.
			B4	**18-BIT TFT BLUE BIT [4]:** This bit is BLUE Color Data Bit 4 for 18-bit TFT color LCDs.
			B2	**12-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data Bit 2 for 12-bit TFT color LCDs.
			B1	**9-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data Bit 1 for 9-bit TFT color LCDs.
			SLD2	**16-BIT STN COLOR LOWER BIT [2]:** This bit is Lower Data Bit 2 for 16-bit dual-scan and single-scan STN color LCDs.
			SLD2	**8-BIT STN COLOR LOWER BIT [2]:** This bit is Lower Data Bit 2 for 8-bit dual-scan and single-scan STN color LCDs.
			LD2	**LOWER DATA [2]:** This bit is Lower Panel Data Bit 2 for dual-scan STN monochrome LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[7]	122	O	B7	**24-BIT TFT BLUE BIT [6]:** This bit is BLUE Color Data Bit 7 (MSB) for 24-bit TFT color LCDs.
			B5	**18-BIT TFT BLUE BIT [4]:** This bit is BLUE Color Data Bit 5 (MSB) for 18-bit TFT color LCDs.
			B3	**12-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data Bit 3 (MSB) for 12-bit TFT color LCDs.
			B2	**9-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data Bit 2 (MSB) for 9-bit TFT color LCDs.
			SLD3	**16-BIT STN COLOR LOWER BIT [3]:** This bit is Lower Data Bit 3 for 16-bit dual-scan and single-scan STN color LCDs.
			SLD3	**8-BIT STN COLOR LOWER BIT [3]:** This bit is Lower Data Bit 3 (MSB) for 8-bit dual-scan and single-scan STN color LCDs.
			LD3	**LOWER DATA [3]:** This bit is Lower Panel Data Bit 3 (MSB) for dual-scan STN monochrome LCDs.
FP[8]	123	O	G0	**24-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data Bit 0 (LSB) for 24-bit TFT color LCDs.
FP[9]	125	O	G1	**24-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data Bit 1 for 24-bit TFT color LCDs.
FP[10]	126	O	G2	**24-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data Bit 2 for 24-bit TFT color LCDs.
			G0	**18-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data Bit 0 (LSB) for 18-bit TFT color LCDs.
			SUD4	**16-BIT STN Color Upper Bit [4]:** This bit is Upper Data Bit 4 for 16-bit dual-scan and single-scan STN color LCDs.
FP[11]	127	O	G3	**24-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data Bit 3 for 24-bit TFT color LCDs.
			G1	**18-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data Bit 1 for 18-bit TFT color LCDs.
			SUD5	**16-BIT STN Color Upper Bit [5]:** This bit is Upper Data Bit 5 for 16-bit dual-scan and single-scan STN color LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[12]	128	O	G4	**24-BIT TFT GREEN BIT [4]:** This bit is GREEN Color Data Bit 4 for 24-bit TFT color LCDs.
			G2	**18-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data Bit 2 for 18-bit TFT color LCDs.
			G0	**12-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data Bit 0 (LSB) for 12-bit TFT color LCDs.
			SLD4	**16-BIT STN COLOR LOWER BIT [0]:** This bit is Lower Data Bit 4 for 16-bit dual-scan and single-scan STN color LCDs.
			SUD0	**8-BIT STN COLOR UPPER BIT [0]:** This bit is Upper Data Bit 0 (LSB) for 8-bit dual-scan and single-scan STN color LCDs.
			UD0	**UPPER DATA [0]:** This bit is Upper Panel Data Bit 0 (LSB) for dual-scan STN monochrome LCDs.
FP[13]	129	O	G5	**24-BIT TFT GREEN BIT [5]:** This bit is GREEN Color Data Bit 5 for 24-bit TFT color LCDs.
			G3	**18-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data Bit 3 for 18-bit TFT color LCDs.
			G1	**12-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data Bit 1 for 12-bit TFT color LCDs.
			G0	**9-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data Bit 0 (LSB) for 9-bit TFT color LCDs.
			SLD5	**16-BIT STN COLOR LOWER BIT [5]:** This bit is Lower Data Bit 5 for 16-bit dual-scan and single-scan STN color LCDs.
			SUD1	**8-BIT STN COLOR UPPER BIT [1]:** This bit is Upper Data Bit 1 for 8-bit dual-scan and single-scan STN color LCDs.
			UD1	**UPPER DATA [1]:** This bit is Upper Panel Data Bit 1 for dual-scan STN monochrome LCDs

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[14]	130	O	G6	**24-BIT TFT GREEN BIT [6]:** This bit is GREEN Color Data Bit 6 for 24-bit TFT color LCDs.
			G4	**18-BIT TFT GREEN BIT [4]:** This bit is GREEN Color Data Bit 4 for 18-bit TFT color LCDs.
			G2	**12-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data Bit 2 for 12-bit TFT color LCDs.
			G1	**9-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data Bit 1 for 9-bit TFT color LCDs.
			SLD6	**16-BIT STN COLOR LOWER BIT [6]:** This bit is Lower Data Bit 6 for 16-bit dual-scan and single-scan STN color LCDs.
			SUD2	**8-BIT STN COLOR UPPER BIT [2]:** This bit is Upper Data Bit 2 for 8-bit dual-scan and single-scan STN color LCDs.
			UD2	**UPPER DATA [2]:** This bit is Upper Panel Data Bit 2 for dual-scan STN monochrome LCDs.
FP[15]	131	O	G7	**24-BIT TFT GREEN BIT [6]:** This bit is GREEN Color Data Bit 7 (MSB) for 24-bit TFT color LCDs.
			G5	**18-BIT TFT GREEN BIT [4]:** This bit is GREEN Color Data Bit 5 (MSB) for 18-bit TFT color LCDs.
			G3	**12-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data Bit 3 (MSB) for 12-bit TFT color LCDs.
			G2	**9-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data Bit 2 (MSB) for 9-bit TFT color LCDs.
			SLD7	**16-BIT STN COLOR LOWER BIT [7]:** This bit is Lower Data Bit 7 (MSB) for 16-bit dual-scan and single-scan STN color LCDs.
			SUD3	**8-BIT STN COLOR UPPER BIT [3]:** This bit is Upper Data Bit 3 (MSB) for 8-bit dual-scan and single-scan STN color LCDs.
			UD3	**UPPER DATA [3]:** This bit is Upper Panel Data Bit 3 (MSB) for dual-scan STN monochrome LCDs.
FP[16]	133	O	R0	**24-BIT TFT RED BIT [0]:** This bit is RED Color Data Bit 0 (LSB) for 24-bit TFT color LCDs.
FP[17]	134	O	R1	**24-BIT TFT RED BIT [1]:** This bit is RED Color Data Bit 1 for 24-bit TFT color LCDs.
FP[18]	135	O	R2	**24-BIT TFT RED BIT [2]:** This bit is RED Color Data Bit 2 for 24-bit TFT color LCDs.
			R0	**18-BIT TFT RED BIT [0]:** This bit is RED Color Data Bit 0 (LSB) for 18-bit TFT color LCDs.
			SUD6	**16-BIT STN COLOR UPPER BIT [6]:** This bit is Upper Data Bit 6 for 16-bit dual-scan and single-scan STN color LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[19]	136	O	R3	**24-BIT TFT RED BIT [3]:** This bit is RED Color Data Bit 3 for 24-bit TFT color LCDs.
			R1	**18-BIT TFT RED BIT [1]:** This bit is RED Color Data Bit 1 for 18-bit TFT color LCDs.
			SUD7	**16-BIT STN COLOR UPPER BIT [7]:** This bit is Upper Data Bit 7 (MSB) for 16-bit dual-scan and single-scan STN color LCDs.
FP[20]	137	O	R4	**24-BIT TFT RED BIT [4]:** This bit is RED Color Data Bit 4 for 24-bit TFT color LCDs.
			R2	**18-BIT TFT RED BIT [2]:** This bit is RED Color Data Bit 2 for 18-bit TFT color LCDs.
			R0	**12-BIT TFT RED BIT [0]:** This bit is RED Color Data Bit 0 (LSB) for 12-bit TFT color LCDs.
			SUD0	**16-BIT STN COLOR UPPER BIT [0]:** This bit is Upper Data Bit 0 (LSB) for 16-bit dual-scan and single-scan STN color LCDs.
FP[21]	138	O	R5	**24-BIT TFT RED BIT [5]:** This bit is RED Color Data Bit 5 for 24-bit TFT color LCDs.
			R3	**18-BIT TFT RED BIT [3]:** This bit is RED Color Data Bit 3 for 18-bit TFT color LCDs.
			R1	**12-BIT TFT RED BIT [1]:** This bit is RED Color Data Bit 1 for 12-bit TFT color LCDs.
			R0	**9-BIT TFT RED BIT [0]:** This bit is RED Color Data Bit 0 (LSB) for 9-bit TFT color LCDs.
			SUD1	**16-BIT STN COLOR UPPER BIT [1]:** This bit is Upper Data Bit 1 for 16-bit dual-scan and single-scan STN color LCDs.
FP[22]	139	O	R6	**24-BIT TFT RED BIT [6]:** This bit is RED Color Data Bit 6 for 24-bit TFT color LCDs.
			R4	**18-BIT TFT RED BIT [4]:** This bit is RED Color Data Bit 4 for 18-bit TFT color LCDs.
			R2	**12-BIT TFT RED BIT [2]:** This bit is RED Color Data Bit 2 for 12-bit TFT color LCDs.
			R1	**9-BIT TFT RED BIT [1]:** This bit is RED Color Data Bit 1 for 9-bit TFT color LCDs.
			SUD2	**16-BIT STN COLOR UPPER BIT [2]:** This bit is Upper Data Bit 2 for 16-bit dual-scan and single-scan STN color LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[23]	140	O	R7	**24-BIT TFT RED BIT [6]:** This bit is RED Color Data Bit 7 (MSB) for 24-bit TFT color LCDs.
			R5	**18-BIT TFT RED BIT [4]:** This bit is RED Color Data Bit 5 (MSB) for 18-bit TFT color LCDs.
			R3	**12-BIT TFT RED BIT [3]:** This bit is RED Color Data Bit 3 (MSB) for 12-bit TFT color LCDs.
			R2	**9-BIT TFT RED BIT [2]:** This bit is RED Color Data Bit 2 (MSB) for 9-bit TFT color LCDs.
			SUD3	**16-BIT STN COLOR UPPER Bit [2]:** This bit is Upper Data Bit 3 (for 16-bit dual-scan and single-scan STN color LCDs.
FPDE	108	O		**FLAT PANEL DISPLAY ENABLE:** For those LCDs that require an external display enable, this pin is used to provide a data enable. For the CL-GD7542, it is the second Shift Clock output for single-scan dual-clock STN color LCDs.
FPVDCLK	113	O		**FLAT PANEL VIDEO CLOCK:** This signal is used to drive the LCD shift clock which is designated as CP2 by some LCD manufacturers.
LFS	110	O		**LCD FRAME START:** This output provides a pulse to start a new frame on LCDs.
LLCLK	112	O		**LCD LINE CLOCK:** This output is used to drive the LCD line clock. This signal is also designated as LP or CP1 by some LCD manufacturers.
MOD	117	O		**MODULATION:** This output provides AC inversion. It should be connected to the MOD, FR, or DF inputs of the LCD, as appropriate. Some LCD manufacturers provide this function in the LCD circuitry, in which case this pin does not need to be connected.

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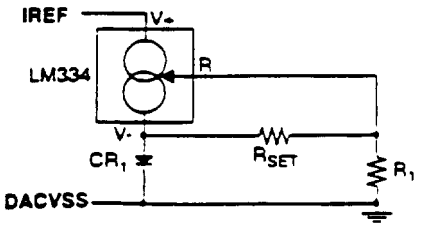
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2.3 CRT Interface Pins

Pin Name	Pin No.	Type	Description
BLUE	96	O	**BLUE VIDEO:** This analog output supplies current that corresponds to the blue value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the Lookup Table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to the IREF signal as follows: $I_{full} = (63/30) \times IREF$ To maintain IBM VGA compatibility, each DAC output is typically terminated to monitor ground with a 150-ohm 2% resistor. This resistor, in parallel with the 75-ohm resistor in the monitor, will yield a 50-ohm impedance to ground. For a full-scale voltage of 700 mV, the full-scale current output should be 14 mA.
GREEN	97	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
HSYNC	91	3-S	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin may be connected directly to the corresponding pin on the monitor connector.
IREF	99	I	**DAC CURRENT REFERENCE:** The current drawn from AVDD2/AVDD3 through this pin determines the full-scale output of each DAC. This pin should be connected to a constant-current source. For information on how to calculate the IREF constant current, refer to the IREF application note in the 7542 Applications Book

Example

V_{DD}	R_{SET} ± 1%	R_1 ± 1%	Diode CR_1
5.0 Volts	22.1 Ω	200 Ω	1N4148 or equivalent
3.3 Volts	15 Ω	121 Ω	Schottky Diode (V_F < 0.4V)



2.3 CRT Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Description
RED	98	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
VSYNC	93	3-S	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin may be connected directly to the corresponding pin on the monitor connector.

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2.4 NTSC and PAL Interface Pins

Because flat panel LCD control pins are used with NTSC and PAL interfaces, while the NTSC and PAL interface pins are used, flat panels should be isolated. External AND gates should be used to force flat panel control signals to the proper levels. (For design details, refer to the Application Note on NTSC.)

Name	Pin No.	Type	Description
BLUE	96	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the Lookup Table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $I_{full} = (63/30) \times IREF$ When an NTSC/PAL Encoder is used at the same time as the CRT, there must be a 1.4k-ohm series termination resistor between the CL-GD7542 and the R, G, and B inputs of the encoder. There is also a 0.7k ohm resistor connected to ground from each R, G, and B input, to provide the correct input-voltage level for the encoder. To maintain a full-scale voltage of 700 mV across the CRT inputs, the full-scale current output should be 14 mA. For termination details, refer to Section 2.3.
CSYNC	95	O	**COMPOSITE SYNC:** This output provides the Composite SYNC for the analog NTSC/PAL Encoder. For NTSC/PAL interfaces, connect CSYNC to the Encoder SYNC input.
GREEN	97	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
NTSC/PAL	94	O	**NTSC/PAL ENCODING SELECTION:** This output is used by the CL-GD7542 to select the desired NTSC or PAL encoding format. Register bits CR30[3:2] control the level on this pin.
RED	98	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
TVON	146	O	**TVON:** When SR25[6] = 0, this output controls the power to the NTSC/PAL Encoder. When this output is high, the encoder is powered on. When this output is low, the encoder is turned off.
XRDACCS			**EXTERNAL RAMDAC CHIP SELECT:** When SR25[6] = 1, a high on this output is used to enable an external RAMDAC. This function is not supported for PCI bus applications.

2.5 Dual-Frequency Synthesizer Interface Pins

Pin Name	Pin No.	Type	Description
CLK32k	89	I	**32-kHz CLOCK:** This input may be connected to an externally supplied 32-kHz clock signal to be used for memory refresh during Suspend Mode. If this pin is not used, it should be tied to ground.
MCLK/XMCLK	197	I/O	**MCLK/XMCLK:** When SR23[3] = 0, the internal MCLK is available on this pin. When SR23[3] = 1, this pin is used as an input from an external XMCLK source. These configurations are intended for testing only.
MFILTER	200	O	**MEMORY CLOCK FILTER:** This pin **must** be connected to a Pi RC filter which is returned to MAVSS. The filter components, especially the input capacitor and the resistor, **must** be placed as close as possible to the MFILTER pin.

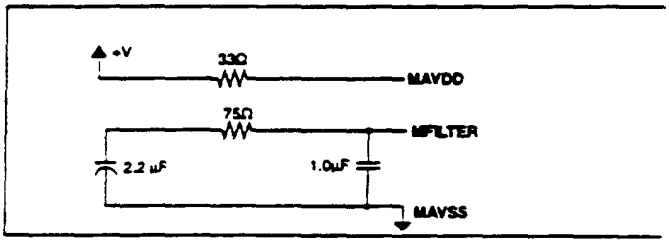


Figure 2–1. Typical Memory Clock Filter

OSC	85	I	**OSCILLATOR INPUT:** This TTL input pin supplies the reference frequency for the Dual-frequency Synthesizer. It requires an input frequency of 14.31818 MHz ± 0.01% with a duty cycle of 50% ± 10%. This input can be supplied from the appropriate pin on the PCI Bus, or from an oscillator.
XVCLK		I	**XVCLK INPUT:** External video clock source input – intended for testing only.
VFILTER	83	O	**VIDEO CLOCK FILTER:** This pin **must** be connected to a Pi RC filter which is returned to VAVSS. The filter components, especially the input capacitor and the resistor, **must** be placed as close as possible to the VFILTER pin.

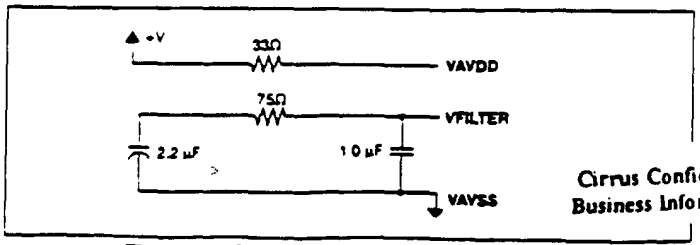


Figure 2–2. Typical Video Clock Filter

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2.6 Display Memory Interface Pins

Pin Name	Pin No.	Type	Description
CAS#	181	O	**COLUMN ADDRESS STROBE#:** This active-low output is used to latch the column address from MA[9:0] into the DRAMs. When register SRF[0] = 0 (dual-WE# DRAMs), this pin is defined as CAS#, and must be connected to the CAS# inputs of the DRAMs.
WE#			**WRITE ENABLE#:** When register SRF[0] = 1 (dual-CAS# DRAMs), this pin is defined as WE#, and must be connected to the WE# inputs of the DRAMs.
CAS[3:0]#	169:170	O	**COLUMN ADDRESS STROBE#:** These active-low outputs are used to control the CAS# (or WE#) inputs to the DRAMs. When register SRF[0] = 1 (dual-CAS# DRAMs), these active-low outputs must be connected to the CAS# inputs of the DRAMs.
WE[3:0]#	169:170, 195:194		**WRITE ENABLE# [3:0]:** When register SRF[0] = 0 (dual-WE# DRAMs), these active-low outputs must be connected to the WE# inputs of the DRAMs.
MA[9.0]	171:180	O	**MEMORY ADDRESS [9:0]:** These outputs drive the address inputs of the DRAMs.
MD[31:0]	151:161, 163:167, 186:191, 193,196, 202:204, 206:208,1:2	I/O	**MEMORY DATA [31:0]:** These 32 bidirectional pins are used to transfer data between the CL-GD7542 and display memory. These pins must be connected to the data pins of the DRAMS.
OE#	182	O	**OUTPUT ENABLE#:** This active-low output is used to control the Output Enables of the DRAMs. For 256K x 16 DRAMs with Dual-Write Enables, this pin must be connected to the OE# pins of all the DRAMs in the display memory array.
RAS#[1:0]	184:183	O	**ROW ADDRESS STROBE#:** These active-low outputs are used to latch the row address from MA[9:0] into the DRAMs. Each RAS pin is used for one bank of memory, for a total of two banks. These pins must be connected to the RAS# pins of all the DRAMs in the display memory array.

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2.7 Configuration Input Pins

During the rising edge of Reset#, the levels on these configuration input pins are read and stored in register SR22 and SR24[7].

Pin Name	Pin No.	Type	Description
FC	157	I	**FEATURE CONNECTOR:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR24[7] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 to supply all the Feature Connector signals. (Refer to section 2.10.) When no pull-up, this pin is configured for other operations.
FVL	165	I	**FAST VESA Local BUS:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR22[2] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 for a 50-MHz bus clock input. (Refer to Note a.)
PCI	167	I	**PCI BUS SELECT:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR22[0] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 for PCI bus operation, and a minimum-grant value of 250 ns. PCI Burst Mode is selected when this pin is high and GRE[4] = 1. (Refer to Note a.)
PCI-MGE	159	I	**PCI BUS with MEMORY-GRANT EXTEND:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR22[7] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 to support the PCI bus, and to extend the minimum-grant value from 250 ns to 500 ns. PCI Burst Mode is selected when this pin is high and register GRE[4] = 1. (Refer to Note a.)
S46	161	I	**SLEEP ADDRESS SELECT:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR22[5] during the rising edge of the Reset# pulse. This high level selects the sleep address at 46E8[3], which is used when the CL-GD7542 is used as an adapter. When no pull-up resistor is supplied, the CL-GD7542 selects a sleep address at 3C3[0], which is the normal mother-board configuration.
XCLK	164	I	**EXTERNAL CLOCK SELECT:** An external pull-up resistor configures the CL-GD7542 for external clock inputs on the SW0 / MCLK / XMCLK and OSC / XVCLK pins. This configuration is used for testing only, and no pull-up resistor should be attached during normal operation. When no resistor is supplied, the CL-GD7542 uses its internal clock sources.

Note a To choose the system bus, only one pull-up resistor may be supplied on PCI-MGE (pin 159), FVL (pin 165), or PCI (pin 167). When no pull-up resistor is supplied, the CL-GD7542 is configured for a VESA Local bus operation of 33 MHz or less

2.8 Switch and Miscellaneous Configuration Input Pins

Pin Name	Pin No.	Type	Description
SW0	197	I	**SWITCH 0:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in register SR24[0].
SW1	149	I	**SWITCH 1:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in register SR24[1].
SW2	150	I	**SWITCH 2:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in register SR24[2].
TWR#	100	I	**TEST WRITE#:** This active-low input is for factory testing and must not be connected to the system for normal operation. It has an internal pull-up resistor.

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2.9 Power Management Pins

Pin Name	Pin No.	Type	Description
ACTI	86	I	**ACTIVITY:** When SR23[6] = 1, this pin is an optional activity-sense input. With register masking, any low-to-high transition on this input may be used to reset the internal power-down timers. When SR23[6] = 1 and CR2D[6] = 1, the ACTI input when high can reset the Standby timer. When SR23[6] = 1 and CR2D[3] = 1, the ACTI input, when high, resets the Backlight timer.
SBYI			**STANDBY INPUT:** When SR23[6] = 0, this input is the hardware control for the Standby Mode. When SBYI goes high, it initiates the power-down sequence that starts the Standby Mode. When not used, this input should be connected to ground.
BLI	87	I	**BACKLIGHT INPUT:** When SR23[5] = 1, a high on this input turns off the backlight of the LCD display.
SUSPI			**SUSPEND INPUT:** When SR23[5] = 0, a high on this internally de-bounced input initiates hardware-controlled Suspend Mode. The hardware-controlled Suspend Mode is the most efficient power-saving mode for the system.
CLK32k	89	I	**32-kHz Clock:** This input may be connected to an externally supplied 32-kHz clock signal to be used for memory refresh during Suspend Mode. If not used, this pin should be tied to ground.
FPBL	105	O	**FLAT PANEL BACKLIGHT:** This output is part of the LCD power sequencing. It should be connected to the LCD backlight enable.
FPVCC	106	O	**FLAT PANEL VCC:** This output is part of the LCD power sequencing. It should be connected to the LCD logic-power enable.
FPVEE	102	O	**FLAT PANEL VEE:** This output is part of the LCD power sequencing. It should be connected to the LCD power enable.
PROG	148	O	**PROGRAMMABLE OUTPUT:** This output pin is forced high or low under the control of register CR30[7]. It is used by the BIOS to select 3.3V or 5.0V power supplies to support the operating frequencies selected.
SBYST#	123	O	**STANDBY STATUS#:** This output, when low, indicates that the CL-GD7542 is in Standby mode.
SLEEP#	81	I	**SLEEP#:** This active-low input is used by the external hardware to put the CL-GD7542 into bus Sleep mode.
SPST#	125	O	**SUSPEND STATUS#:** This output, when low, indicates that the CL-GD7542 is in Suspend mode.

2.10 Feature Connector Pins

When an external pull-up resistor (<60k ohms) is attached to the FC / MD[25] pin, a logic high is read and stored in SR24[7] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 to supply all the following Feature Connector signals. When no pull-up resistor is supplied, these pins are configured for other operations.

Pin Name	Pin No.	Type	Description
FCBLANK#	101	I or O	**FEATURE-CONNECTOR BLANK#:** When FCESYNC# is high, FCBLANK# is an output which supplies a blanking signal to the feature connector. When FCESYNC# is low, FCBLANK# is an input which can force RGB outputs to zero current.
FCDCLK	103	O	**FEATURE-CONNECTOR DOT CLOCK:** When the Feature Connector configuration is active, this pin provides the dot clock output to the subsystem that is driven by the Feature Connector.
VCLK			**VCLK:** Video clock output. This pin is intended to be used for testing only.
FCESYNC#	147	I	**FEATURE-CONNECTOR ESYNC#:** When this input is high, the HSYNC, VSYNC, and FCBLANK# outputs are enabled. When this input is low, the HSYNC and VSYNC outputs are forced to high-impedance (off), and FCBLANK# is configured as an input.
FCEVIDEO#	86	I	**FEATURE-CONNECTOR ENABLE VIDEO#:** This input controls the buffers on FCP[7:0]. When FCEVIDEO# is high, the FCP[7:0] pins are pixel data outputs. When FCEVIDEO# is low, the FCP[7:0] pins are inputs, and the contents of display memory are ignored.
FCP[7.0]	144:141, 134,133, 125, 123	I or O	**FEATURE-CONNECTOR PIXEL DATA:** When FCEVIDEO# is high, these pins are pixel data outputs that copy the pixel address to the palette RAM. When FCEVIDEO# is low, these pins are inputs that can be used to drive pixel data into the palette DAC.
FCVCLK	114	I	**FEATURE-CONNECTOR VIDEO CLOCK:** This pin should be connected to the pixel clock from the Feature Connector. (For more information, refer to SR23[7].)
OVRW#	115	O	**OVERLAY WINDOW:** This active-low output is asserted during the active portion of the video overlay window. It is intended to be used in applications involving video overlays. For additional connectivity information, see Appendix A8.

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2.11 Ground Pins

Pin Name	Pin No.	Description
DACVSS[1:2]	88, 111	**DIGITAL-TO-ANALOG CONVERTER VSS GROUND:** These two pins are used to supply ground reference to the Palette DAC of the CL-GD7542. Each pin **must** be connected to the Analog ground rail, which should be isolated from VSS (digital) ground.
MAVSS	201	**MCLK ANALOG VSS GROUND:** This pin is used to supply ground reference to the memory clock synthesizer of the CL-GD7542. This pin **must** be connected to the Analog ground rail, which should be isolated from VSS (digital) ground.
VAVSS	82	**VCLK ANALOG VSS GROUND:** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD7542. This pin **must** be connected to the Analog ground rail, which should be isolated from VSS (digital) ground.
S[1:11]	6,42,52,67 80,104,124 145,168,185 198	**VSS (Digital) GROUND:** These 11 pins are used to supply ground reference for the core logic and pin groups of the CL-GD7542. Each pin **must** be connected directly to the ground rail. When a multi-layer board is used, each VSS pin **must** be connected to the ground plane.

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2.12 Power Pins

Pin Name	Pin No.	Description
BVDD[1:2]	47,73	**BUS VDD:** These two pins are used to supply either +3.3V or +5.0V to the bus interface pin group of the CL-GD7542. 1. Each pin **must** be connected directly to the VDD rail. 2. Each pin **must** be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. 3. When a multi-layer board is used, connect each BVDD pin to the power plane.
CRTVDD	92	**CRT VDD:** This pin is used to supply +3.3V or +5.0V to the CRT interface pin group of the CL-GD7542. 1. This pin **must** be connected directly to the VDD rail. 2. This pin **must** be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible. 3. When a multi-layer board is used, connect this CRTVDD pin to the power plane.
CVDD[1:4]	36,62, 121,192	**CORE VDD:** These four pins are used to supply +3.3V or +5.0V to the internal core logic of the CL-GD7542. 1. Each pin **must** be connected directly to the VDD rail. 2. Each pin **must** be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. 3. When a multi-layer board is used, connect each CVDD pin to the power plane.
DACVDD[1:2]	90, 109	**DIGITAL-TO-ANALOG CONVERTER VDD:** These two pins are used to supply +3.3V or +5.0V to the Palette DAC of the CL-GD7542. 1. Each pin **must** be connected directly to the VDD rail. 2. Each pin **must** be bypassed with 0.1-µF and 10 µF capacitors that have the proper high-frequency characteristics and are as close to each pin as possible. 3. When a multi-layer board is used, connect each DACVDD pin to the power plane.

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2.12 Power Pins *(cont.)*

Name	Pin No.	Description
FPVDD[1:2]	132,107	**FLAT PANEL VDD:** This pin is used to supply +3.3V or +5V to the flat panel interface pin group of the CL-GD7542. 1. Each pin must be connected directly to the VDD rail. 2. Each pin must be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible. 3. When a multi-layer board is used, connect these FPVDD pins to the power plane.
MAVDD	199	**MCLK ANALOG VDD:** This pin is used to supply +3.3V or +5.0V to the Memory Clock Synthesizer of the CL-GD7542. This pin must be connected to the VDD rail via a 33-ohm resistor and bypassed to MAVSS with 0.1 µF and 10 µF capacitors.
MVDD[1:2]	205,162	**MEMORY VDD:** These two pins are used to supply +3.3V or +5.0V to the internal memory (DRAM) interface pin group of the CL-GD7542. 1. Each pin must be connected directly to the VDD rail. 2. Each pin must be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. 3. When a multi-layer board is used, connect each MVDD pin to the power plane.
VAVDD	84	**VCLK ANALOG VDD:** This pin is used to supply +3.3V or +5.0V to the Video Clock Synthesizer of the CL-GD7542. This pin must be connected to the VDD rail via a 33-ohm resistor and bypassed to VAVSS with 0.1 µF and 10 µF capacitors.

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3. Functional Description

This section provides functional information and design guidelines for the CL-GD7542 Graphics User Interface Accelerator (GUIX) SVGA LCD Controller with MVA™.

3.1 General

The CL-GD7542 offers a tightly integrated, high-performance motherboard solution. Multiple designs can be developed, ranging from a relatively simple GUIX solution to a portable multimedia solution capable of displaying accelerated video playback windows with graphics or an overlaid live video window with graphics. All hardware necessary for CPU updates to memory, display refresh, and DRAM refresh is included in the CL-GD7542. A complete SVGA-compatible motherboard solution can be implemented with the CL-GD7542 plus two 256K x 16 DRAMs.

3.2 Functional Blocks

Figure 3–1 shows a block diagram of the CL-GD7542 GUIX SVGA LCD Controller with MVA. The functional blocks integrated in the CL-GD7542 are described in the following sections.

3.2.1 CPU Bus Interface

The CL-GD7542 connects directly to a '486/ VESA VL-Bus or a PCI bus. No additional logic circuitry is required to implement these bus interfaces

486/VL-Bus

The CL-GD7542 interfaces directly to '486DX microprocessors and the VESA VL-Bus, at speeds up to 50 MHz with the core VDD at 5V. The CL-GD7542 supports both 1X and 2X bus clocks, but will require external circuitry to support the 2X clocks

PCI Bus

The CL-GD7542 interfaces directly to the PCI bus . No additional logic is required to support the CL-GD7542 multiplexed address and data pins The CL-GD7542 executes 32-bit I/O and memory accesses at speeds up to 33 MHz The CL-GD7542 also supports memory burst cycles. PCI bandwidth is at least 50% better utilized with burst cycles.

Linear Memory Addressing

The CL-GD7542 supports linear memory addressing, as an alternative to the standard VGA method of accessing display memory with 64-Kbyte segments. With linear memory addressing, the CL-GD7542 is configured so that it accesses display memory as a one- or two-MByte linearly addressed string of bytes.

For applications or drivers that support this method, Linear Memory Addressing improves graphics performance by simplifying access to display memory, since it is not necessary to calculate offsets into a relatively small window, nor is it necessary to test for a crossing of the window boundary.

The CL-GD7542 supports Linear Memory Addressing of the VGA address space, which may reside within any 1-Mbyte segment above the first 16 MBytes in a 4-GByte address space. For '486 local bus interfaces that use a 32-bit address, to select the desired 16-Mbyte partition with the A[31:24] address line, an external decoder may be needed. However, in general, there is no need for an external decode of the CPU addresses. Any one of the A[31] to A[24] lines can be directly connected to HIMEM0 or HIMEM1. For instance, if HIMEM1 is connected to A[31], then CL-GD7542 is mapped into the upper 2 GBytes of the CPU address space.

The register bits SR2D[7:6] extend the address space to 64 MBytes by re-mapping HIMEM0 and HIMEM1 within this address space. An external decoder may be needed only if a fully decoded 16M-byte partition within the 4 GByte address space is desired. The output from this address-line decoder drives the HIMEM0 and HIMEM1 inputs. The SR7[7:4] register is used to select the 1M-byte through 16M-byte range in any 16M-byte space allowed by the microprocessor. (Note HIMEM0 and HIMEM1 are used only with VL-bus and 32-bit local buses).

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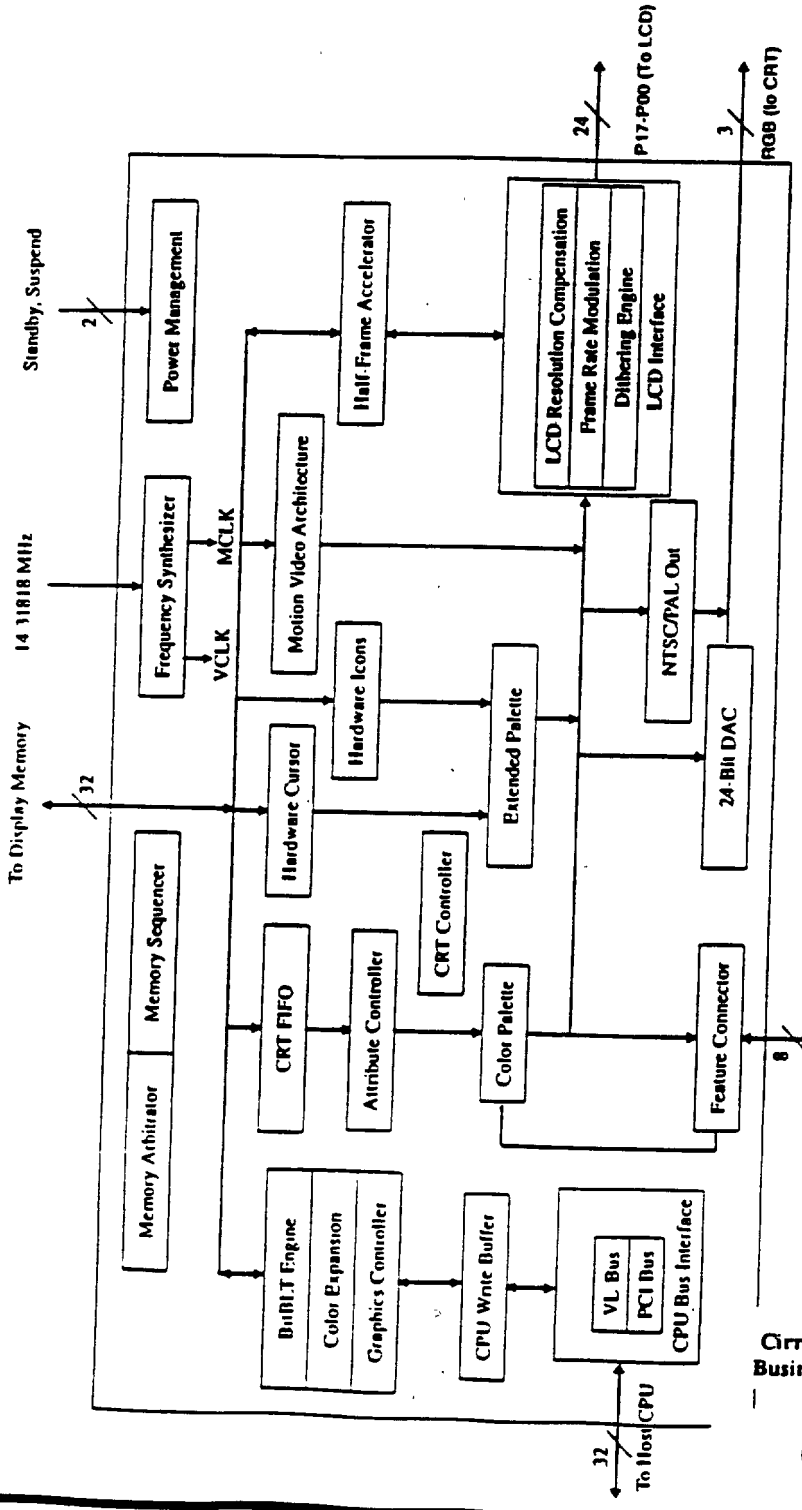


Figure 3–1. CL-GD7542 Block Diagram

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3.2.2 CPU Write Buffer

The CPU Write Buffer contains a queue of CPU write accesses to display memory that have not been executed due to memory arbitration. Maintaining this queue of write accesses allows the CL-GD7542 to release the CPU bus as soon as it has recorded the address and data. The CL-GD7542 therefore executes the operation when display memory is available, increasing CPU performance. For all text and graphics modes, the CL-GD7542's Write Buffer depth is two 32-bit or four 16-bit levels. The CL-GD7542 has the capability to page CPU cycles if they are accumulated in the write buffer.

3.2.3 Graphics Controller

The Graphics Controller operates in either text or graphics modes and performs the following major functions:

- Provides the host CPU a read/write access path to display memory
- Controls all four memory planes in planar modes
- Allows data to be manipulated prior to being written to display memory
- Formats data for use in various backward compatibility modes
- Provides color read comparators for use in color painting modes
- Reads/writes 32-bit words through the 32-bit display memory interface

The Graphics Controller directs data from the display memory to the CPU. Figure 3–2 and Figure 3–3 illustrate typical write and read operations respectively.

For a write operation, the data from the CPU bus are combined with the data from the Set/Reset Logic in the CPU, depending on the Write mode. In addition, the data may be combined with the contents of the read latches, and some bits or planes may be masked (prevented from being changed) by using the Bit Mask Register. For more information refer to the Graphics Controller registers in Section 6.5.

3.2.4 Color Expansion

Color expansion is the automatic conversion of a monochrome bit map (which typically defines a character, icon, or pattern) into foreground and background color values. These values are then written into display memory and held in a CL-GD7542 register.

Color Expansion improves CPU write performance by optimizing use of the available host bandwidth via expanding single bits across the bus into complete 8- or 16-bit pixels.

When color expansion is used, only monochrome bit maps must be transmitted across the bus. Each bit of the monochrome map is converted into 8-bit or 16-bit pixel modes. The bus traffic is reduced by a factor of 8 to 16, making it possible to use nearly all of the available display memory bandwidth.

3.2.5 Bit Block Transfer (BitBLT) Engine

The BitBLT (Bit Boundary Block Transfer) engine moves a rectangle of data either within display memory, or between system memory and display memory, with minimal CPU intervention. The BitBLT engine can also perform pattern fills (filling an area with a repeating pattern), raster operations (combining the source bytes with the destination bytes using various logic operations), and color expansion/ transparency.

The CL-GD7542's BitBLT engine provides 16 two-operand ROPs (Raster Operations) to move data in packed-pixel modes from the source area to the destination area. This operation occurs in packed-pixel modes with 8-bit or 16-bit pixel transfers. The transfers from CPU are always taken in four-byte increments. For screen-system transfers, the BitBLT operation acts as a read cache. The BitBLT accelerates Graphics User Interfaces (GUIs), such as Microsoft Windows 3.1, Windows NT, and OS/2 2.1. Refer to Appendix A1 "BitBLT Engine" for more information.

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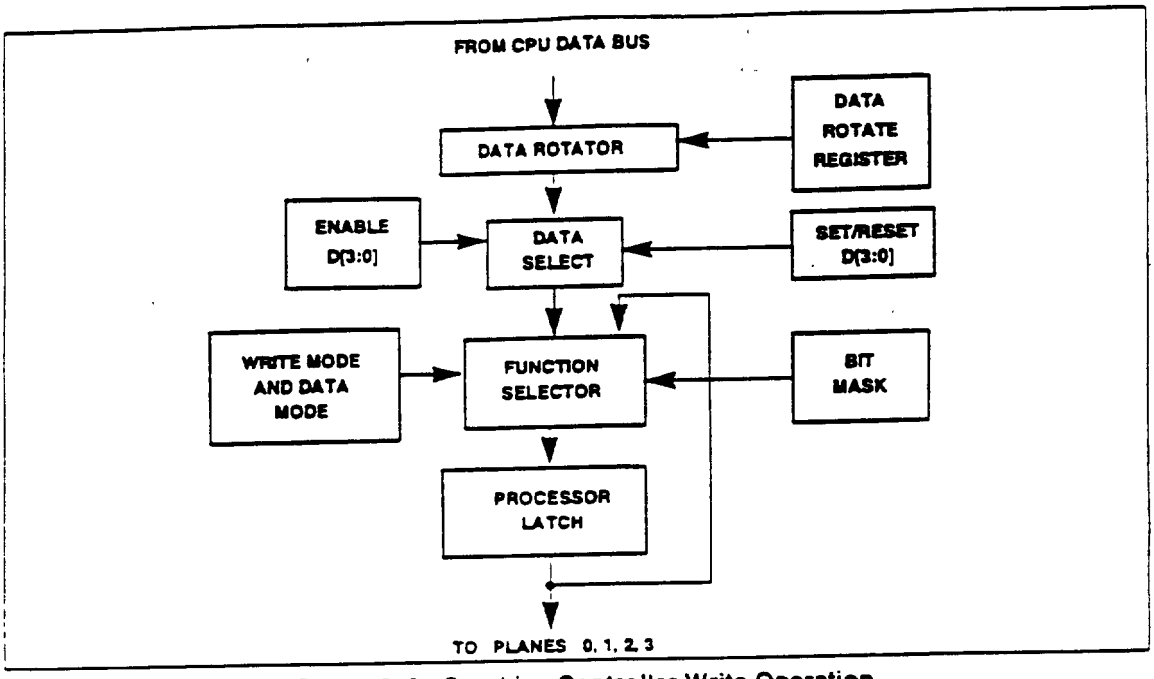


Figure 3–2. Graphics Controller Write Operation

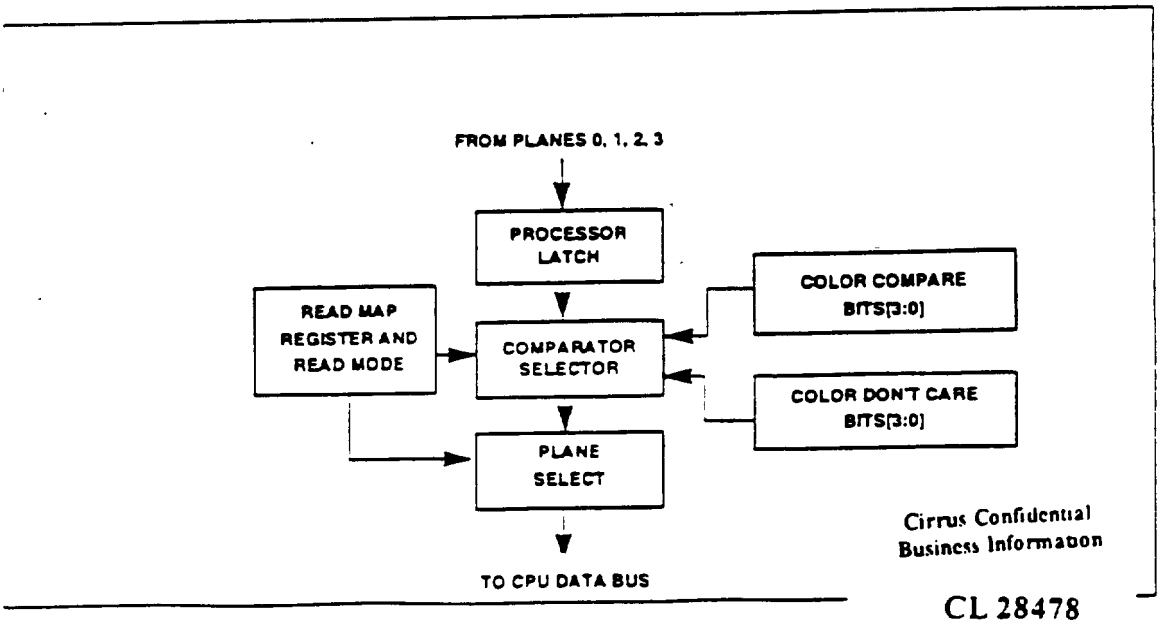


Figure 3–3. Graphics Controller Read Operation

3.2.6 Memory Arbitrator

The Memory Arbitrator allocates bandwidth to the following functions, which compete for the limited bandwidth of display memory:

- CPU access
- Display refresh
- DRAM refresh
- BitBLT
- Half-Frame Accelerator (for dual-scan STN LCDs)
- Hardware Cursor
- Hardware Icons

DRAM refresh is handled invisibly by allocating a selectable number of CAS*-before-RAS* refresh cycles at the beginning of each scanline. Cycles are allocated to display refresh and CPU/BitBLT according to the FIFO-control parameters, with priority given to display refresh.

3.2.7 Memory Sequencer

The Memory Sequencer generates all necessary timing and control signals for display memory. This includes RAS*, CAS*, and multiplexed-address timing, as well as WE* and OE* timing. The Sequencer generates CAS*-before-RAS* refresh, random-read, random-early-write, fast-page-mode read, and early-write cycles. The Memory Sequencer generates multiple-CAS* or multiple-WE* signals, depending on the memory type being used. The CL-GD7542 supports the following memory configurations, which have a 32-bit-wide memory interface.

- Two 256K x 16 DRAMs for 1-MByte display memory
- Four 256K x 16 DRAMs for a 2-MByte display memory
- Four 512K x 8 DRAMs (symmetric only) for a 2-MByte display memory

The CL-GD7542 supports both dual-CAS# and dual-WE# 256K x 16 DRAMs.

Refer to Appendix A6 "Memory Configurations" for more information.

The Memory Sequencer ensures that the necessary display refresh transfer cycles and dynamic memory refresh cycles are executed and that the remaining memory cycles are made available for CPU read/write operations.

The CL-GD7542 fully supports all the standard IBM VGA memory organizations, along with the following extended video memory modes:

- 2-color packed-pixel modes (1-bit/pixel) in linear 32-bit words or VGA-style 8-bit words
- 16-color planar mode (4 bits/pixel)
- 16-color packed-pixel modes (4 bits/pixel), which is useful for PowerPC applications
- 256-color packed-pixel modes (8 bits/pixel)
- Direct-Color (32K or 64K colors) packed-pixel modes (16 bits/pixel)
- Mixed 32K- and 256-color packed-pixel modes (15 bits/pixel)
- True-Color 16.8M-color packed-pixel modes (24 bits/pixel)

In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. This is in contrast with VGA chain-4 addressing, a type of addressing that stores consecutive pixels at every fourth byte address in display memory. For more information, refer to Appendix A13 "Extended Video Modes Programming" and Appendix A5 "True Color Modes".

3.2.8 CRT FIFO Register

The CRT FIFO (First-In, First-Out) Register allows the Memory Sequencer to execute display memory accesses needed for display refresh at maximum memory speed, rather than at the display refresh rate. This register makes it possible to take advantage of DRAM's fast-page mode operation. The CRT FIFO Register is 16 words deep and 32 bits wide.

3.2.9 Attribute Controller Registers

The Attribute Controller Registers format the display for the screen. They perform the following:

- serialization of memory data
- display color selection
- text blinking
- underlining in both text and graphics modes

The Attribute Controller Registers are described in Section 6.6.

Figure 3–4 is a functional block diagram of the Attribute Controller.

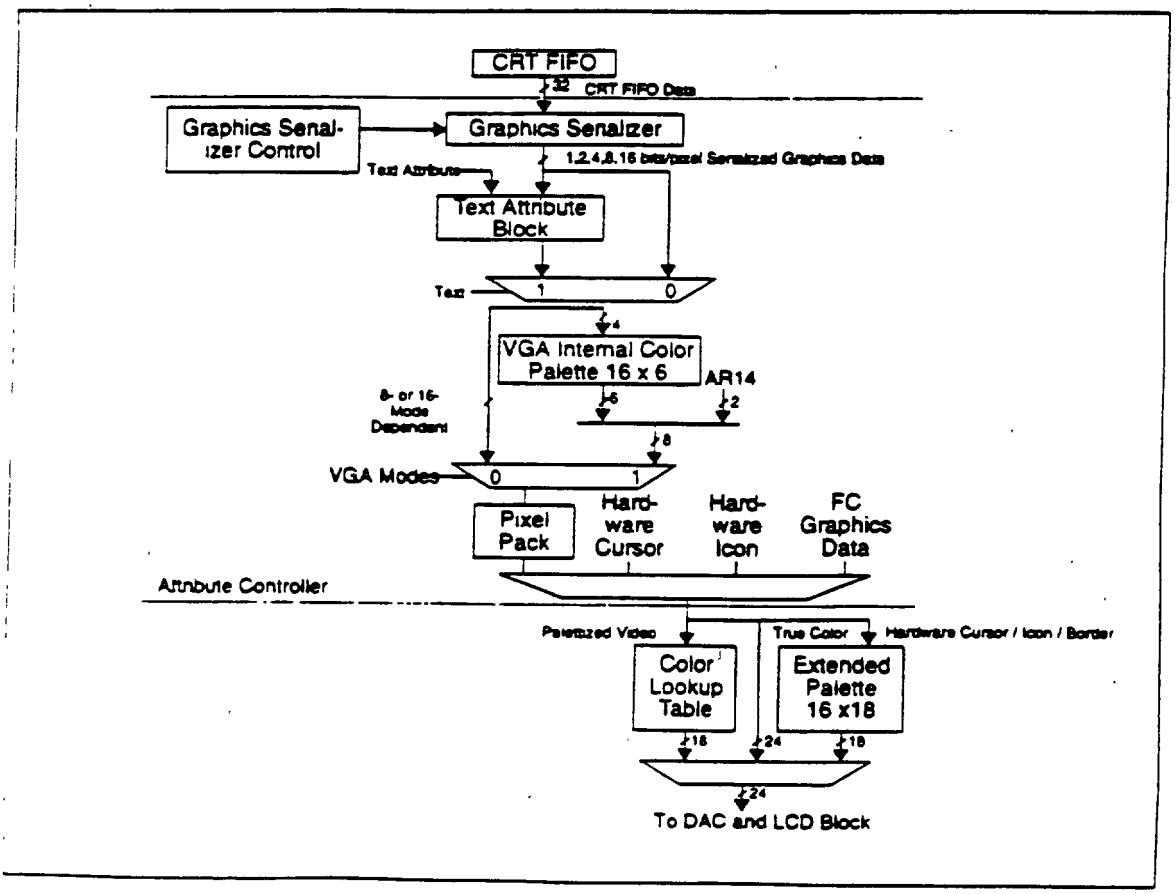


Figure 3–4. Attribute Controller Functional Block Diagram

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3.2.10 CRT Controller Registers

The CRT Controller (CRTC) Registers generate horizontal and vertical synchronization signals (HSYNC and VSYNC) for the CRT display. The CRTC Registers also generate the BLANK# signals required by the Palette DAC. In addition, they support both standard VGA-compatible modes and extended modes and provide for the following:

- configuration options, including user-configurable horizontal/vertical timing and polarity)
- cursor positioning
- horizontal scanlines
- pixel and byte panning
- split-screen capability and smooth scrolling

Figure 3–5 is a functional block diagram of the CRT controller.

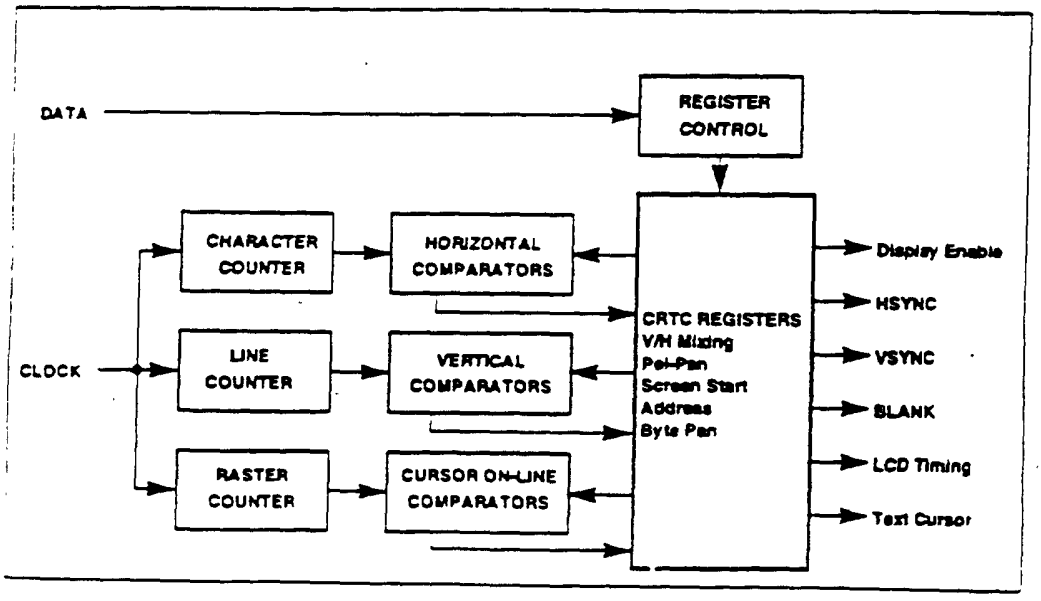


Figure 3–5. CRT Controller Functional Block Diagram

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In addition to supporting standard VGA text modes, the CL-GD7542 supports the following text modes: 132 x 25, 132 x 43, and 132 x 50.

In addition to supporting standard graphics modes, the CL-GD7542 supports the following graphics modes:

- For CRTs:
  - 1280 x 1024 interlaced, up to 16 colors
  - 1024 x 768 non-interlaced, up to 256 colors
- For CRTs and LCDs (non-interlaced)
  - 800 x 600, up to 64K colors
  - 640 x 480, up to 16.8M colors

SimulSCAN™, the simultaneous display capability, is supported at resolutions of 640 x 480 or 800 x 600. For a complete listing of all modes supported by the CL-GD7542, refer to Chapter 4.

Up to 1024 x 768 16-bit/pixel modes (that is, 5-5-5 or 5-6-5 R-G-B direct-color modes) are supported with either a 1X VCLK (pixel rate is equal to VCLK) or with a 2X VCLK (pixel rate is equal to twice the VCLK). The 640 x 480 24-bit/pixel modes (8-8-8, the R-G-B true-color modes) are supported with a 3X VCLK (that is, the pixel rate is equal to three times the VCLK)

3.2.11 Hardware Cursor

The hardware cursor replaces the software mouse pointer commonly used by GUI applications. The hardware cursor eliminates the need for application software to save and restore the display data as the mouse pointer position changes. The application software typically initializes the hardware cursor once, and from that point it needs only to update the cursor (x,y) position to move the cursor on the display

The hardware cursor offers a smoothly moving mouse pointer with improved performance as compared to a software cursor. The hardware cursor is always displayed on top of graphics, or video, or the hardware icons.

The hardware cursor consists of either 64 x 64 two-bit pixels or 32 x 32 two-bit pixels. Each pixel in the hardware cursor may be either transparent or one of two colors from an 18-bit palette

The hardware cursor's palette is stored in the Extended Palette, such that it may be different from the VGA color palette. The first bit of each pixel in the hardware cursor defines whether or not the pixel is transparent. If the pixel is not transparent, the second bit defines the pixel's color. The second bit selects one of two 18-bit colors in the Extended Palette.

The following types of 2-bit hardware cursor patterns can be loaded into upper display memory:

- 64 x 64 hardware cursor patterns (up to 8 patterns)
- 32 x 32 hardware cursor patterns (up to 32 patterns)

After the hardware cursor patterns are loaded into upper display memory, application programs can quickly select one pattern as the active cursor pattern. The hardware cursor is available in all modes except text modes and mode 13. Note the hardware cursor is not supported in 640 x 480 24-bit/pixel modes. For more information, refer to Appendix A2 "Hardware Cursor".

3.2.12 Hardware Pop-up Icons

The CL-GD7542 provides hardware pop-up icons for displaying small, on-screen symbols that indicate system status (for example, a battery "fuel gauge"). These hardware icons are stored in upper display memory and can be displayed at the touch of a key. The hardware icons are independent of the graphics mode being used.

The CL-GD7542 supports two hardware icon modes:

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- Hardware Icon Mode 1.
  Up to four icons, each 64 x 64 pixels in size, can be displayed simultaneously in a vertical column. Each icon is independently controlled for color (up to 4 colors or 3 colors plus transparency). Each icon can be expanded either horizontally by pixel doubling, vertically by scanline doubling, or both horizontally or vertically to a maximum size of 128 x 128 pixels per icon

- When one of the icons is doubled vertically, that icon extends down, which forces all other icons down.
- When one of the icons is doubled horizontally, that icon expands to the right of the display.
- Each of the four icons is allocated two memory maps. (A total of eight hardware icon memory maps can be stored in display memory.)

- Hardware Icon Mode 2.
  One 64 x 64 pixel hardware icon, from a menu of eight hardware icon memory maps, can be displayed. Each icon is independently controlled for color (up to 4 colors or 3 colors plus transparency) and for all other icon attributes (such as blink, horizontal and vertical doubling, icon enable, and memory map selection).

Hardware icon(s) are supported in all text and graphics modes, except 24-bit/pixel modes with a 3X clock, 16-bit/pixel modes with a 2X clock, and interlaced modes.

Hardware icon(s) are independent of the hardware cursor. When both a hardware cursor and hardware icon(s) are displayed, the hardware cursor passes on top of the hardware icon(s).

The CL-GD7542 priority of display overlays is as follows:

- Hardware cursor - always displayed on top
- Hardware icon
- MotionVideo™ Window data, or VGA graphics, or text data

3.2.13 Color Palette

The CL-GD7542 Color Palette consists of a 256 18-bit-word Color Lookup Table (CLUT). Each 18-bit word consists of three 6-bit values, one for each primary color (Red, Green, and Blue). The 18-bit word defines one of 2^{18} or 262,144 (referred to as "256K") colors.

The CLUT converts an 8-bit color code that specifies the color of a pixel into an 18-bit value, such that 256 simultaneous colors are displayed from a palette of 256K colors. Refer to Figure 3–6.

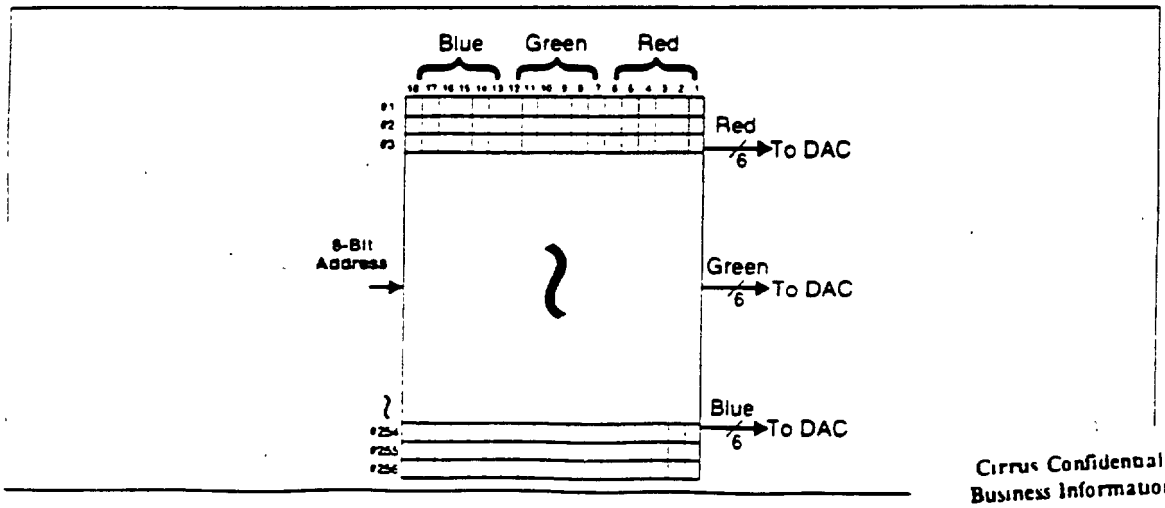


Figure 3–6. Color Lookup Table

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The contents of the CLUT are accessed via its 8-bit-wide host interface. An 8-bit address value applied to the pixel-address inputs defines the memory location for reading an 18-bit color data word from the CLUT.

An internal synchronizing circuit allows the color value accesses to be completely asynchronous to the pixel video operation. Special display operations, such as flashing objects and overlays, are possible because the palette incorporates a pixel word mask to allow the incoming pixel address to be altered. As a result, changes to the contents of the CLUT can be made immediately.

The CLUT has anti-sparkle circuitry to reduce random noise on the display during CPU accesses to the palette.

Direct-Color and True-Color Modes

In addition to graphics modes that use the 256 x18 CLUT, the CL-GD7542 supports the following Direct-Color and True-Color modes, which are useful in graphics and multimedia applications:

- 5-5-5 RGB 32K Direct-Color Mode.
  This mode bypasses the CLUT. Each pixel is represented by 15 bits, consisting of five bits each of Red, Green, and Blue color information to provide 32,768 (2^{15}) simultaneously displayed colors.
- 5-6-5 RGB 64K Direct-Color Mode.
  This mode bypasses the CLUT. Each pixel is represented by 16 bits, consisting of five bits of Red, six bits of Green, and 5-bits of Blue color information to provide 65,536 (2^{16}) simultaneously displayed colors.
- 8-8-8 RGB 16.8M True-Color Mode.
  This mode bypasses the CLUT. Each pixel is represented by 24 bits, consisting of one byte each of Red, Green, and Blue color information to provide 16,777,216 (2^{24}) simultaneously displayed colors.
- Mixed-Color Mode.
  This mode combines 256-color packed-pixel modes (which use the CLUT) and 5-5-5 RGB 32K-color modes (which bypass the CLUT).

  Each pixel consists of 16 bits. The pixel data bit [15] is used to select between the 5-5-5 RGB mode and the standard palette mode on a pixel-by-pixel basis.

For a block diagram showing the above-mentioned modes bypassing the CLUT, refer to Figure 3–7. For more information on true-color modes, refer to Appendix A5 "True-Color Modes".

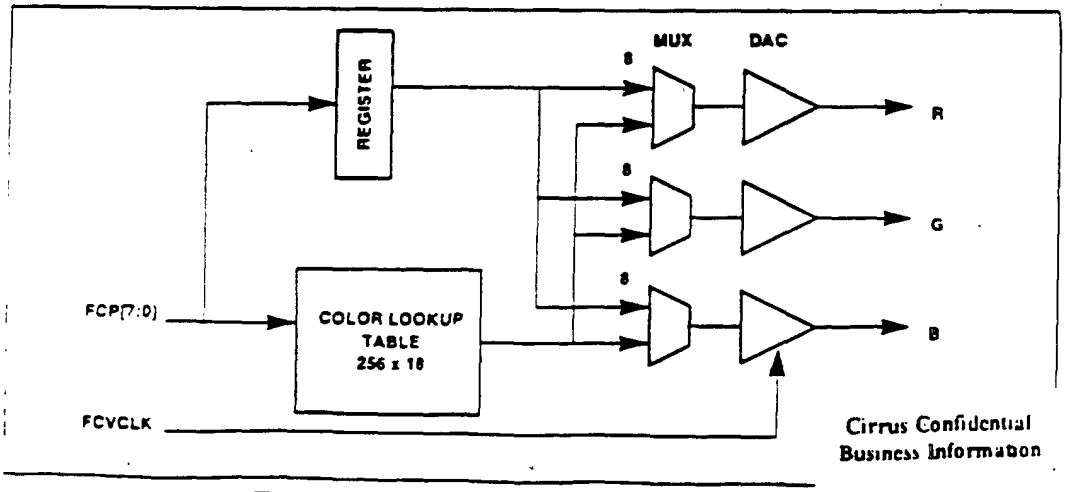


Figure 3–7. 256-Color Direct-Color Palette DAC

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Monochrome STN LCDs

On monochrome STN LCDs, the CL-GD7542 produces up to 256 gray scales. (For more information on gray scales, refer to Section 3.2.20 and Section 3.2.23.)

For graphics modes, these outputs -- the 6-6-6 RGB (from the CLUT), the 5-5-5 RGB, 5-6-5 RGB, and the 8-8-8 RGB – are converted to either 64 or 256 gray scales. The conversion to gray scales takes place by programming register CR1E[7:6] for one of the following three options:

- NTSC weighting
  (30% Red + 59% Green + 11% Blue)
- Green-only
- Attribute controller (6-bits)

For text modes, pixel data is converted into gray scales as follows:

- 4-bit pixel data (4 bits for foreground/background color) is directly converted into 16 gray scales.
- 6-bit pixel data (the lower 6 of 8 bits packed-pixel) is directly converted into 64 gray scales.

The CL-GD7542 also provides the following types of text contrast enhancements:

- General Contrast Enhancement:
  - If the background color is *greater* than the foreground color, the foreground color is set to 0, and the background color remains unchanged.
  - If the background color is *less* than the foreground color, the background color is set to 0, and the foreground color remains unchanged
- Foreground-Only Contrast Enhancement.
  - If the background color is *greater* than the foreground color, the foreground color is set to 0 and the background color remains unchanged.
  - If the background color is *less* than the foreground color, the foreground color is set to 7 and the background color remains unchanged

The CL-GD7542 provides reverse video:

- Reverse video for text modes is provided by programming register CR1E[5].
- Reverse video for graphics modes is provided by programming register CR1E[4].

3.2.14 Extended Palette RAM

The CL-GD7542's Extended Palette RAM provides 18-bit/pixel data (6-6-6 RGB) for the following functions:

- Hardware cursor
- Hardware icon
- Overscan border color

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As shown in Table 3–1, the Extended Palette RAM enables the colors of the hardware cursor, hardware icons, and the border to be programmed independently from the standard 256 x 18 VGA Color Lookup Table.

Table 3–1. Extended Palette RAM

I/O Address	Physical RAM Location	Function
X0h	256	Hardware cursor background color
XFh	257	Hardware cursor foreground color
X2h	258	Fix color of overscan (the border)
X3h	259	Hardware icon color #0 (Not for 3 colors + transparent mode)
X4h	260	Hardware icon color #1
X5h	261	Hardware icon color #2
X6h	262	Hardware icon color #3
XCh	268	Used by Video BIOS
XDh	269	Used by Video BIOS
XEh	270	Used by Video BIOS

3.2.15 Triple DAC

The DAC includes three 8-bit digital-to-analog converters (DACs). The DAC outputs drive the Red, Green, and Blue color video inputs to the CRT. The DAC outputs are designed to produce a 0.7-volt peak-white amplitude when supplied with a reference current (IREF). The IREF current is supplied with the circuit shown in the IREF pin description in Chapter 2. For all IREF values and output loading:

- $V_{Black\ Level}$ = 0 volts
- $V_{Maximum\ White}$ = 0.7 volts

Two sense methods — analog and digital — can be used to detect the type of CRT monitor that is connected.

With the analog sense method, the CL-GD7542 places specific color values on the RGB lines and then compares the resulting voltage level against a known internal reference voltage.

Extended graphics modes are capable of 75-Hz vertical refresh rates in a non-interlaced format.

- With the core voltage CVDD = 5.0V, the DACs operate up to 85 MHz and support the non-interlaced refresh rates shown in Table 3–2.
- With the core voltage CVDD = 3.3V, the DACs operate up to 65 MHz and support the non-interlaced refresh rates shown in Table 3–2.

For information on CRT-only video modes, refer to Section 4.1.

Table 3–2. Refresh Rates for CRTs in SimulSCAN Mode

Panel Type	Bits/Pixel	Refresh Rate for CRTs in SimulSCAN Mode					
		Case 1. CRTs in SimulSCAN Mode with Single-Scan STNs[a]		Case 2. CRTs in SimulSCAN Mode with Dual-Scan Color STNs[a]		Case 3. CRTs in SimulSCAN Mode with Dual-Scan Mono STNs[a]	
		50-MHz MCLK	45-MHz MCLK	50-MHz MCLK	45-MHz MCLK	50-MHz MCLK	45-MHz MCLK
640 x 480	8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	75 Hz	75 Hz
640 x 480	16 bpp	75 Hz	75 Hz	70 Hz	60 Hz	75 Hz	71 Hz
640 x 480	24 bpp	60 Hz	56 Hz	48 Hz	44 Hz	56 Hz	56 Hz
640 x 480	80-character text	75 Hz	75 Hz	75 Hz	72 Hz	75 Hz	75 Hz
800 x 600	8 bpp	75 Hz	75 Hz	65 Hz	61 Hz	75 Hz	75 Hz
800 x 600	16 bpp	58 Hz	55 Hz	45 Hz	39 Hz	54 Hz	47 Hz
800 x 600	80-character text[b]	60 Hz	60 Hz	54 Hz	56 Hz	58 Hz	58 Hz
1024 x 768	8 bpp	71 Hz	66 Hz	Not supported			
1024 x 768	16 bpp	Not supported					

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a. In Case 1, the refresh rate is given for CRTs that are used in SimulSCAN mode with single-scan STNs.
In Case 2, when CRTs are used in SimulSCAN mode with dual-scan color STNs, the dual-scan STN LCDs have double the CRT refresh rates shown in the table.
For LCDs not in the SimulSCAN mode, it is possible to achieve higher refresh rates by reducing the non-display time.

b. Character cells are 10 dots wide, whether or not the text is expanded.

3.2.16 MotionVideo™ Architecture

The MotionVideo™ Architecture (MVA™) provides the following video multimedia features:

- Cost-effective, high-quality video-playback hardware acceleration for file formats
- Video playback of other file formats (for example MPEG, the Motion Picture Experts Group format) via a software driver that is compatible with the Device Control Interface (DCI)

Video playback using a VGA controller *without* MVA has a number of limitations:

- The video playback's pixel color depth must be the same as the pixel color depth of the surrounding graphics. For a 24-bit/pixel video playback window, the entire 640 x 480 or 800 x 600 display must operate in 24-bit/pixel modes.
- Pixel performance on a 640 x 480 24-bit/pixel display is very slow, because bandwidth is limited by the 32-bit display memory interface.
- With a 32-bit display memory interface, 800 x 600 and 1024 x 768 24-bit/pixel resolutions are not possible. The display memory interface would require 2 to 3 MBytes of display memory, with a 64-bit wide display memory interface, which is not economical in mainstream notebooks.
- Mixing video and graphics functions such as zooming in software introduces additional overhead and does not alleviate the display memory bottleneck.

When playing back video while using a VGA controller *without* the MVA advantage, the above limitations result in the following disadvantages:

- the video playback window's pixel color depth is low (typically 8 bits per pixel)
- the screen resolution is small (typically 160 x 120 or 320 x 240)
- the frame rate is low (typically 15 frames/second)
- the graphics performance is sluggish
- the display memory requirements are high

3.2.16.1 MotionVideo™ Window

MVA creates a MotionVideo Window that utilizes off-screen memory and which is positioned on top of the VGA graphics mode data. (The hardware icons and hardware cursor are displayed on top of the MotionVideo Window).

The MotionVideo Window functions as an overlay image that can be positioned anywhere on the display. Position and size of the MotionVideo™ Window are programmable via registers CR3X, with 8-pixel horizontal resolution and 1-scanline vertical resolution.

The MotionVideo Window can be displayed with SimulSCAN on both CRT monitors and the following LCDs:

- 640 x 480
- 800 x 600

With MVA, the display memory becomes a multi-format display memory. As a result, as listed below, different color pixel depths and data formats can be mixed in the MotionVideo™ Window display.

- The MotionVideo Window's color pixel depth is independent of the color pixel depth of the surrounding graphics.
  - For example, a MotionVideo Window may operate in a 24-bits/pixel mode, while the surrounding graphics operate in a 8-bits/pixel or 4-bits/pixel mode (even in planar modes).
- 640 x 480 Single-Scan Color/Mono LCDs
- 640 x 480 Dual-Scan Color/Mono LCDs
- 800 x 600 Single-Scan Color/Mono LCDs
- 800 x 600 Dual-Scan Color/Mono LCDs
- The MotionVideo Window's data format is independent of the data format of the surrounding graphics.
  - For example, 4:2:2 YUV video data can be stored with 4-bit or 8-bit RGB graphics data in the display memory. (The 4:2:2 YUV format is compressed, since 4:2:2 uses an average of 16-bits/pixel to provide the same color quality as 24-bit/pixel RGB modes.)

This mixing of color pixel depth modes and data formats provides high-quality video playback, along with high-performance graphics, while minimizing display memory requirements.

The MotionVideo Window's video data is stored in MotionVideo Memory, a contiguous portion of off-screen display memory. As shown in Figure 3–8, MotionVideo Memory is located as follows:

- *above* graphics memory (where pixel data for standard and extended VGA modes is stored).
- *in* the half-frame accelerator if and only if a dual-scan LCD is used.
- *below* the last 16KB of display memory (where data for the hardware cursor and the hardware icons is stored.

Off-screen display memory is not required when the MotionVideo Window and surrounding graphics use the same pixel color depth and format.

During display refresh, data is accessed from either MotionVideo Memory or Graphics Memory on a pixel-by-pixel basis.

Note that no double accesses to display memory are required, alleviating the display memory bandwidth bottleneck.

Any data format supported by MVA can be displayed. Furthermore, new data formats can be added as needed.

The MotionVideo Window (MVW) supports the following color space formats:

- 24-bit/pixel RGB 8-8-8
- 16-bit/pixel 4:2:2 YUV linear (Y0UY1V)
- 16-bit/pixel RGB 5-6-5
- 16-bit/pixel RGB 5-5-5
- 8-bit/pixel RGB 3:3:2 through the palette
- 8-bit/pixel RGB 3-3-2 (3:3:2) direct

For a description of 16-bit/pixel and 24-bit/pixel RGB formats, refer to Section 3.2.13.

The MVA optimizes display memory bandwidth while minimizing display memory requirements. As a result, high-quality MVWs may be displayed with high-resolution graphics modes by using only 1 MByte of display memory.

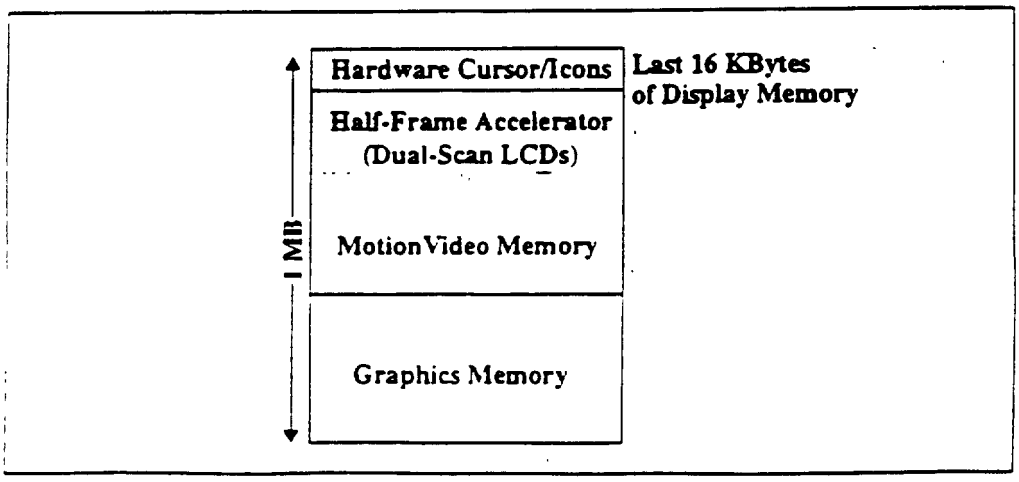


Figure 3–8. MotionVideo™ Memory, Stored as Part of Display Memory

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Table 3–3 shows the graphics display modes that are possible when using various combinations of MotionVideo Windows and when up to 1 MByte of display memory is available. Note that:

- With a 640 x 480 graphics display mode (on either a color TFT LCD, STN LCD, or a CRT) the following MVWs may be displayed:
  - A 640 x 480 (full-screen) MVW, with 8, 16, or 24 bits/pixel format. Surrounding graphics display modes (SGDMs) may be 4, 8, or 16 bits/pixel.
  - A 320 x 240 MVW, with any bits/pixel format. SGDMs may be 4, 8, 16, or 24 bits/pixel.
- With an 800 x 600 color graphics display mode (on either a color TFT LCD or a CRT), the following MVWs may be displayed:
  - A 640 x 480 MVW, with 8 bits/pixel format. SGDMs may be 4 or 8 bits/pixel.
  - A 640 x 480 MVW, with 16 bits/pixel format. SGDMs may be 4 bits/pixel.
  - A 320 x 240 MVW, with 8 or 16 bits/pixel. SGDMs may be 4 or 8 bits/pixel.
  - MVWs with SGDMs of 24 bits/pixel are not possible because of the display memory size and the 32-bit memory interface.
- With a 800 x 600 color dual-scan STN LCD, MVWs may not be displayed with 800 x 600 single-scan displays since a portion of the display memory is used for the Half-Frame Accelerator.
- With a 1024 x 768 color graphics display mode, the following MVWs may be displayed:
  - A 640 x 480 MVW, with 8 bits/pixel. SGDMs may be 4 bits/pixel.
  - A 320 x 240 MVW, with 8 bits/pixel. SGDMs may be 4 or 8 bits/pixel.

The MVW's pixel color depth corresponds to the formats above. The MVWs resolution is for the source data. Using hardware "zooming," this resolution may be doubled horizontally and vertically on the display. For more information, refer to Section 3.2.16.2.

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Table 3–3. MotionVideo™ Window / Graphics Modes Possible with 1-MByte Display Memory

Type of LCD Display or CRT Monitor	Graphics Display Modes					MotionVideo Window			
	Resolution	(Bits Per Pixel)				Resolution	(Bits Per Pixel)		
		4	8	16	24		8	16	24
Color TFT LCD	640 x 480	Full-screen MVW				640 x 480	✓	✓	✓
		✓	✓	✓	✓	320 x 240	✓	✓	✓
Color Dual-Scan STN LCD		Full-screen MVW				640 x 480	✓	✓	✓
		✓	✓	✓	✓	320 x 240	✓	✓	✓
Color TFT LCD	800 x 600	Full-screen MVW				800 x 600	✓	✓	
		✓	✓			640 x 480	✓		
		✓					✓	✓	
		✓	✓	✓		320 x 240			
		✓	✓				✓	✓	
Color Dual-Scan STN LCD		Full-screen MVW				800 x 600	✓		
		✓	✓			640 x 480	✓		
		✓					✓	✓	
		✓	✓			320 x 240	✓	✓	
CRT Monitor	1024 x 768	Full-screen MVW				1024 x 768	✓		
		✓	✓			640 x 480			
		✓					✓		
		✓	✓			320 x 240	✓		

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Table 3–4 shows combinations of MVWs (resolutions and color depths) and surrounding graphics modes (resolutions and color depths) available for various displays that have 2 MBytes of display memory. With 2 MBytes of display memory, a MVW up to 800 x 600 16-bits/pixel can be combined with 800 x 600 16-bit/pixel graphics. A MVW up to 640 x480 16-bits/pixel can be combined with 1024x768 8-bit/pixel graphics. In addition, 2 MBytes of display memory enables the software drivers to optimize performance by using 64 KBytes to 256 KBytes for caching.

Table 3–4. MotionVideo Window / Graphics Modes Possible with 2-MByte Display Memory

Type of LCD Display or CRT Monitor	Graphics Display Modes					MotionVideo Window			
	Resolution	(Bits Per Pixel)				Resolution	(Bits Per Pixel)		
		4	8	16	24		8	16	24
Color TFT LCD	640 x 480	Full-screen MVW				640 x 480	✓	✓	✓
		✓	✓	✓	✓	320 x 240	✓	✓	✓
Color Dual-Scan STN LCD		Full-screen MVW				640 x 480	✓	✓	✓
		✓	✓	✓	✓	320 x 240	✓	✓	✓
Color TFT LCD	800 x 600	Full-screen MVW				800 x 600	✓	✓	
		✓	✓	✓		640 x 480	✓	✓	
		✓	✓	✓		320 x 240	✓	✓	
Color Dual-Scan STN LCD		Full-screen MVW				800 x 600	✓		
		✓	✓	✓		640 x 480	✓	✓	
		✓	✓	✓		320 x 240	✓	✓	
CRT Monitor	1024 x 768	Full-screen MVW				1024 x 768	✓		
		✓	✓			640 x 480	✓		
		✓	✓			320 x 240	✓		

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MVWs may use several aspect ratios, and they are not limited to a 4:3 aspect ratio. However, one MVW limitation is the amount of available display memory for MotionVideo™ Memory, as shown in the equation below.

MVWM = DMEM - GMEM - ACEL - 16 KBytes

Where:

- MVWM = MotionVideo window memory
- DMEM = Total available memory
- GMEM = Memory required for graphics
- ACEL = Memory required to support the half-frame accelerator required for dual-scan STN panels
- 16 KBytes = Memory reserved for hardware cursor and icon

MVA, which can be used in full-screen configurations, enables the creation of special graphics modes (such as, 24-bit/pixel with a 1X dot clock).

3.2.16.2 Hardware Zooming

As explained in Table 3–5, hardware zooming provides a programmable 2X magnification by doubling pixels either horizontally only, vertically only, or both horizontally and vertically simultaneously.

Table 3–5. Programming for Hardware Zoom

Type of MVW Hardware Zoom	CR3C
Horizontal pixel doubling	CR3C[7] = 1
Vertical pixel doubling	CR3C[6] = 1
Horizontal and vertical pixel doubling	CR3C[7] = 1, and CR3C[6] = 1

3.2.16.3 YUV to RGB Color Space Converter

The integrated YUV-to-RGB Color Space Converter supports two types of YUV-to-RGB algorithms, which are selected by register CR36[5]:

- Format 1 (Standard):
  - R = Y + 1.375V
  - G = Y - 0.375U - 0.75V
  - B = Y + 1.75U
- Format 2:
  - R = Y + V
  - G = Y - 0.25U - 0.5V
  - B = Y+ U

Register CR36[5] determines whether the YUV-to-RGB conversion uses the 2's complement U,V formats (which is useful for Philips SAA15B and SAA9051 TV decoders) or excess 128 format.

3.2.16.4 Video Playback

The MVA provides a MotionVideo Window, consisting of one of the color space formats in Section 3.2.16.1, on top of standard/extended VGA modes. The MotionVideo Window's pixel color depth may be different from the pixel color depth of the surrounding graphics. The internal color space converter may be used to expand 4:2:2 YUV data to 24-bit RGB.

For video playback, the hardware zoom feature may be used to double the MotionVideo Window horizontally, vertically, or both horizontally and vertically, or to fill the display's full resolution.

File Formats

The MVA may be used to accelerate the playback of files in a MotionVideo™ Window. The files would be stored in MotionVideo Memory in a 5-5-5 file format with 320 x 240 resolution.

If a data format is 4:2:2 YUV, then during display refresh, the internal color space converter converts the 4:2:2 format to 24-bit/pixel RGB.

If the display color resolution is less than 24 bits/pixel, the MVA dithering algorithm may be employed by programming registers CR4D and CR4E to increase the displayed pixel color depth to 24-bits/pixel, independently of the graphics color resolution.

By programming registers CR33 through CR39, the MotionVideo Window may be re-positioned anywhere on the display. By programming register CR3C, the 320 x 240 MotionVideo™ Window may

be expanded so that the 320 x 240 window may be doubled to 640 x 480 on 800 x 600 LCDs.

The pixel depth of the MotionVideo Window may be different from the pixel depth of the surrounding graphics.

Figure 3–9 shows a 320 x 240 video clip (5-5-5 RGB) that is displayed as a 640 x 480 15-bit/pixel MotionVideo Window on a 256-color 800 x 600 display, which can be accomplished using just one MByte of display memory.

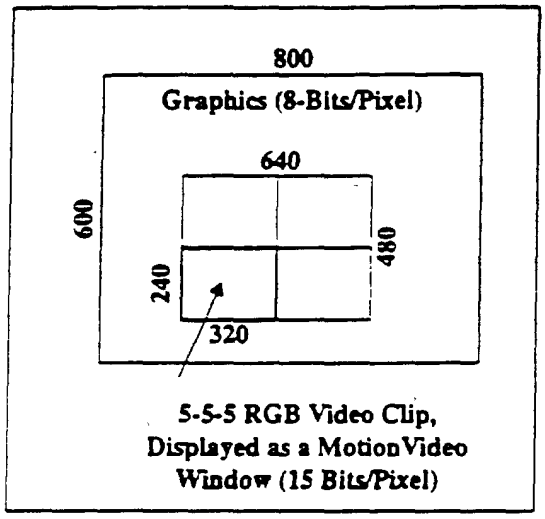


Figure 3–9. MotionVideo Window

3.2.17 Feature Connector

The CL-GD7542 provides the functionality of a standard VGA Feature Connector. The CL-GD7542's Feature Connector includes the following pins.

- FCP[7.0]. bi-directional 8-bit data port
- FCDCLK. dot clock output
- FCVCLK: video clock input
- FCESYNC#: enable syncs input, to enable the HSYNC, VSYNC, and FCBLANK# outputs
- FCBLANK#: either a blanking signal output, or an input that forces RGB outputs to zero current
- OVRW#: Overlay Window output

The CL-GD7542 supports the Feature Connector, such that video data may be input and displayed as an overlay video window. The Baseline Output Mode (8-bit indexed, one pixel per clock), is directly supported. The CL-GD7542 supports 8-bit/pixel indexed data (FC extended mode).

The 8-bit data is input either by using both phases of the clock or by using a 2X clock. An 8-bit value, stored in the Color Key Compare Register GRC, is compared to the video data input from FCP[7:0] on a pixel-by-pixel basis. A match will cause the pixel's graphics data to be replaced with the video data input.

3.2.18 NTSC/PAL Out

The CL-GD7542 outputs digital RGB data in an interlaced format to an external analog TV encoder, such as Analog Devices AD720 or Motorola MC1377. Only a minimum amount of additional logic circuitry is required. With the addition of an analog encoder, a portable computer can output the following signals, for use with a standard TV monitor or video cassette recorder (VCR):

- NTSC (National Television Standards Committee) signals
- PAL (phase-altering line) signals

The CL-GD7542 will operate in a locked interlaced mode and will use the LCD support shadowing mechanism (which shadows the Horizontal and Vertical CRTC registers) to prevent the application from changing the CRTC setup. Even the dot clock frequency will be locked. Horizontal and vertical display enable will be open to the application.

The NTSC/PAL output will operate in the standard VGA modes. The CL-GD7542 outputs analog RGB, composite sync signals, a NTSC/PAL standard select signal, and TV-On (a power management signal).

Due to TV image limitations, graphics mode 13 and text mode 0 provide the best display quality.

3.2.19 Half-Frame Accelerator

The CL-GD7542 integrates a Half-Frame Accelerator, required by dual-scan LCDs. With the Half-Frame Accelerator, a dual-scan LCD can run at a twice the CRT's refresh rate. The CL-GD7542 provides simultaneous CRT and LCD display operation (SimulScan™) for the following dual-scan LCDs:

- 640 x 480 STN/TFT dual-scan LCDs: the Half-Frame Accelerator provides all the standard VGA modes and extended video modes up to 640 x 480
- 800 x 600 STN/TFT dual-scan LCDs: the Half-Frame Accelerator provides all the standard VGA modes and extended video modes up to 800 x 600

3.2.20 LCD Interface

The CL-GD7542 directly interfaces with a variety of LCDs (and CRTs as well, for SimulSCAN operations). These LCDs include the following:

- Monochrome 640 x 480 dual-scan and single-scan STN LCDs
- Color 640 x 480 and 800 x 600 dual-scan and single-scan STN LCDs (with 8-bit and 16-bit interfaces)
- Color 640 x 480 and 800 x 600 TFT LCDs with the following interfaces:
  - 9-bit (3 bits each for Red, Green, Blue)
  - 12-bit (4 bits each for Red, Green, Blue)
  - 18-bit (6 bits each for Red, Green, Blue)
  - 24-bit (8 bits each for Red, Green, Blue)

3.2.21 LCD Resolution Compensation

With its LCD Resolution Compensation, the CL-GD7542 allows a spectrum of PC applications, originally written for analog CRT monitors that use various VGA modes, to run transparently on LCDs.

The LCD Resolution Compensation feature is necessary, in that unlike CRTs, LCDs have a fixed horizontal and vertical resolution. As a result, when a PC application is selected, VGA modes that are concurrently selected may use a resolution that is lower than the fixed resolution of the LCD. Consequently, unless LCD Resolution Compensation is used, a section of the LCD is left blank.

For example, when VGA text mode 3, which consists of 400 lines, is displayed on a 640 x 480 LCD that does not have use of LCD Resolution Compensation, 80 blank lines remain at the bottom of the LCD. (For a list of various horizontal and vertical resolutions for standard VGA modes, refer to Chapter 4.)

To remove blank space, the CL-GD7542 LCD Resolution Compensation presents these options:

- Automatic expansion of VGA text modes
- Custom fonts to replace standard VGA fonts
- Horizontal centering of displayed lines
- Horizontal expansion of VGA graphics modes
- Vertical centering of displayed lines
- Vertical expansion of VGA graphics modes

Resolution Compensation for 640 x 480 LCDs

For 640 x 480 LCDs, the CL-GD7542 provides the following LCD Resolution Compensation options to display lower-resolution VGA text and graphics:

- Auto-Text Expansion.
  Auto-Text Expansion of a VGA font makes the font consistent across the LCD and eliminates any breaks or artifacts in fonts that connect to adjacent fonts.
  - The 9-pixel-wide VGA fonts (used in the popular VGA text modes 3 and 7) are horizontally displayed as 8-pixel-wide-fonts. As a result, 80 characters fill all 640 pixels across.

  The following methods vertically expand VGA character fonts to 19 pixels. As a result, 475 lines of the LCD's 480 vertical lines are filled.

  - The 8 x 8 (200-line) VGA fonts are double-scanned, vertically expanding the font to equal 16 pixel lines. An extra top pixel line and two extra bottom pixel lines are added to each character row of the font, further vertically expanding the font to equal 19 pixel lines.
  - For 8 x 14 (350-line) VGA fonts, two extra top pixel lines and three extra bottom pixel lines

are added to each character row to vertically expand the font to 19 pixel lines.

- For the 8 x 16 (400-line) VGA fonts, an extra top pixel line and two extra bottom pixel lines are added to each character row to vertically expand the font to 19 pixel lines.

- Custom Fonts.
  Standard VGA fonts (8 x 8, 8 x 14, and 9 x 16) may be replaced with a custom 8 x 19 font to fill 640 x 475 pixels on a 640 x 480 LCD.

- Vertical Centering of Displayed Lines.
  - If Auto-Text Expansion or a custom font is used, the 475 lines that result can be vertically centered on the 480-line LCD.
  - If Auto-Text Expansion or a custom font is not used, 200-, 350-, or 400-line VGA text or graphics modes can also be vertically centered on the 480-line LCD.

- Vertical Graphics Expansion.
  On a 640 x 480 LCD, Vertical Graphics Expansion may be used to run PC application programs that use lower-resolution VGA graphics modes.
  - The 200-line VGA graphics modes are vertically expanded to 475 lines by expanding every 8 lines to 19 lines, using a pattern of 2,2,3,2,2,3,2,3 (double-scan and triple-scan).
  - The 350-line VGA graphics modes are vertically expanded to 475 lines by expanding every 14 lines to 19 lines using a pattern of 1,1,2,1,1,2,1,2,1,1,2,1,1,2 (single-scan and double-scan).

  Popular Graphics User Interface-based applications, such as Windows or OS/2, employ a CL-GD7542 driver that selects the proper VGA graphics mode (such as 2-, 16-, 256-, 32K-, 64K-, or 16.8M-color modes) to run application programs at the full resolution of the 640 x 480 LCD.

Resolution Compensation for 800 x 600 LCDs

For 800 x 600 LCDs, the CL-GD7542 provides the following LCD Resolution Compensation options to display lower-resolution VGA text and graphics:

- Auto-Text Expansion.
  Auto-Text Expansion of a VGA font makes the font consistent across the LCD and eliminates any breaks or artifacts in fonts that connect to adjacent fonts.
  - The 9-pixel-wide VGA fonts (used in the popular VGA text modes 3 and 7) are horizontally displayed as 10-pixel-wide fonts, by replicating the last pixel once. As a result, 80 characters fill all 800 pixels across.

  The following methods vertically expand the VGA character fonts.
  - The 8 x 8 (200-line) VGA fonts are triple-scanned, vertically expanding the font to equal 24 pixel lines. As a result, all of the LCD's 600 vertical lines are filled.
  - For the 8 x 14 (350-line) VGA fonts, every odd scanline is replicated to vertically expand the font to 21 lines. As a result, 525 lines of the LCD's 600 vertical lines are filled.
  - For the 8 x 16 (400-line) VGA fonts, every odd scanline is replicated to vertically expand the font to 24 lines. As a result, all of the LCD's 600 vertical lines are filled.

- Custom Fonts.
  Standard VGA fonts (8 x 8, 8 x 14, and 9 x 16) may be replaced with a custom 10 x 24 font to fill all 800 x 600 pixels on a 800 x 600 LCD.

- Horizontal Centering of Display Lines.
  - VGA text modes that are 720 pixels wide can be horizontally centered, leaving 40 blank pixels each on the left and right sides of the 800 x 600 LCD display.
  - VGA text modes that are 640 pixels wide can be horizontally centered, leaving 80 blank pixels each on the left and right sides of the 800 x 600 LCD display.

- Horizontal Graphics Expansion.
  VGA graphics modes that are 640 pixels wide can be horizontally expanded to 800 pixels by replicating every fourth pixel. (However, currently this expansion is not available for VGA graphics modes that have either 2X dot clocks with 16-bits/pixel or 3X dot clocks with 24-bits/pixel).
- Vertical Centering of Displayed Lines.
  - If Auto-Text Expansion or Vertical Graphics Expansion is used, the 525 lines that result can be vertically centered on the 600-line LCD.
  - If Auto-Text Expansion is not used, the 200-, 350-, or 400-line VGA text or graphics modes can also be vertically centered on the 600-line LCD.
- Vertical Graphics Expansion.
  On a 800 x 600 LCD, Vertical Graphics Expansion may be used to run PC application programs that use lower-resolution VGA graphics modes.
  - The 350-line VGA graphics modes are vertically expanded to 525 lines by replicating all odd scanlines.
  - The 400-line VGA graphics modes are vertically expanded to 600 lines by replicating all odd scanlines.
  - The 480-line VGA graphics modes are vertically expanded to 600 lines by replicating every fourth scanline.

  Popular Graphics User Interface-based applications, such as Windows or OS/2, employ a CL-GD7542 driver that selects the proper VGA graphics mode (such as 2-, 16-, 256-, 32K-, or 64K-color modes) to run the application programs at the full resolution of the 800 x 600 LCD

3.2.22 Frame Rate Modulation

The CL-GD7542 employs a new, improved frame rate modulation (FRM) algorithm to create gray scales on monochrome and color STN LCDs. Over multiple frames in time, the FRM algorithm modulates the "on" and "off" times of individual pixels in the LCD, such that the eye integrates the superimposed pixels as perceptible gray scales.

Proprietary techniques reduce or eliminate entirely the gray scales' artifacts (for example, flicker, noise and pattern motion). On state-of-the-art STN LCDs with fast response times of approximately 100 ms, the result is an outstanding display quality.

The CL-GD7542 provides three FRM options:

- 16-frame FRM.
  This FRM option modulates the pixel over 16 frames in time to create 16 shades for each red, green, and blue (RGB) primary color, for 4,096 (16^3) colors total.

  This option is intended to support STN LCDs currently available and in development, including STN LCDs with very fast response times of approximately 100 ms. This algorithm allows masking of undesirable gray scales (that is, those that exhibit flicker or pattern motion).

  - By setting RBX[4], gray scales 7 and 9 can be converted to gray scales 6 and 8, respectively.
  - By setting RBX[3], gray scales 1 and 15 can be converted to gray scales 0 and 16, respectively.
  - If two gray scales are masked, the FRM algorithm produces 2,744 (14^3) colors.
  - If four gray scales are masked, the FRM algorithm produces 1,728 (12^3) colors.

- 8-frame FRM.
  This FRM option modulates the pixel over 8 frames in time to create 8 shades for each RGB primary color, for 512 (8^3) colors total.

  This option is intended to reduce flicker and "submanning" (that is, the temporary disappearance of the mouse pointer) on future STN LCDs that may have response times that are too fast for the 16-frame FRM option.

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- 4-frame FRM.
  This FRM option modulates the pixel over 4 frames in time to create 4 shades for each RGB primary color, for 64 (4^3) colors total.

  This option is intended to reduce flicker and "submarining" (that is, the temporary disappearance of the mouse pointer) on future STN LCDs that may have response times too fast for both the 16- and 8-frame FRM options.

In summary, the FRM algorithm produces 2, 3, or 4 bits of color depth for each RGB primary color on STN LCDs.

- To add up to 6 bits of color depth to each primary color, the CL-GD7542's Dithering Engine may be used with an FRM algorithm.
- To add up to 8 bits of color depth to each primary color (or 256 gray scales for each primary color) for a total of 16.8M colors, the CL-GD7542's Dithering Engine may be used with only a 4-frame FRM algorithm.

3.2.23 Dithering Engine

The CL-GD7542's Dithering Engine increases the number of perceived colors displayed on the LCD and/or CRT, relative to what the display can physically produce without dithering.

A propietary intercalating spatial dithering technique preserves the spatial resolution of the displayed image. For example, when a 640 x 480 resolution image is dithered, its resolution is maintained, instead of being reduced to 320 x 240.

The Dithering Engine works by automatically selecting a dithering pattern. As shown in Table 3–6, an increase in the dithering pattern increases the number of displayed bits per RGB primary color, depending upon the image's color depth.

Table 3–6. Effective Dithering Patterns

Effective Dithering Pattern	Increased Number of Displayed Bits per RGB Primary Color
2 x 1 Pattern	1 bit
2 x 2 Pattern	2 bits
4 x 2 Pattern	3 bits
4 x 4 Pattern	4 bits
8 x 4 Pattern	5 bits
8 x 8 Pattern	6 bits

The Dithering Engine may automatically add up to 6 bits per primary color, and it may be used for color and monochrome STN LCDs and TFT LCDs. (By programming register CR4C, this automatic feature may be overridden, and the number of bits per primary color limited to a programmable number.)

As shown in Figure 3–1 in Section 3.2, in the data path, the Dithering Engine is after the LCD Resolution Compensation, such that dithering is applied to the expanded image.

The Dithering Engine contains two separate dithering registers:

- Dithering register for standard/extended VGA modes
- Dithering register for MotionVideo™ Window

To render the appropriate colors, the CL-GD7542 dynamically switches dithering between surrounding graphics and the MotionVideo Window. (For more information on the MotionVideo™ Window, refer to Section 3.2.16.1.)

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Table 3–7 shows the number of gray scales that may be displayed on a monochrome STN LCD, by using a combination of the various FRM and dithering options.

As shown in the table, the 4-frame frame-rate-modulation option produces only four gray scales (2 bits/pixel), which are insufficient for displaying 32-, 64-, or 256-gray scale images.

The various dithering options may automatically add up to 6 bits/pixel depending upon the displayed image's color depth.

- To display a 32-gray-scale image (5 bits), the Dithering Engine automatically adds 3 bits to the 2 bits produced by FRM.
- To display a 64-gray-scale image (6 bits), the Dithering Engine automatically adds 4 bits to the 2 bits produced by the FRM.
- To display a 256-gray-scale image (8-bits), the Dithering Engine automatically adds 6 bits to the 2 bits produced by FRM.

Table 3–7. Number of Gray Scales On Mono STN LCDs

Frame-Rate-Modulation Option	Effective Dithering		Resulting Image on Mono STN LCD That Has:		
	Pattern	No. of Bits	32 Gray Scales (5 bits)	64 Gray Scales (6 bits)	256 Gray Scales (8 bits)
4 frames (2 bits)	None	0	4 (2^2)		
	2 x 1	1	8 (2^3)		
	2 x 2	2	16 (2^4)		
	4 x 2	3	32 (2^5)		
	4 x 4	4	32 (2^5)	64 (2^6)	
	8 x 4	5		64 (2^6)	128 (2^7)
	8 x 8	6			256 (2^8)
8 frames (3 bits)	None	0	8 (2^3)		
	2 x 1	1	16 (2^4)		
	2 x 2	2	32 (2^5)		
	4 x 2	3	32 (2^5)	64 (2^6)	
	4 x 4	4		64 (2^6)	128 (2^7)
	4 x 8	5			256 (2^8)
16 frames (4 bits)	None	0	16 (2^4)		
	2 x 1	1	32 (2^5)		
	2 x 2	2	32 (2^5)	64 (2^6)	
	4 x 2	3		64 (2^6)	128 (2^7)
	4 x 4	4			256 (2^8)

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Table 3–8 shows the number of displayed colors on a color STN LCD, with various FRM and dithering options. As shown in Table 3–8, each FRM/dithering option produces the same number of color shades per primary color as gray scales for monochrome LCDs shown in Table 3–7.

Note that the total number of colors is equal to 3X the number of color per primary color RGB.

For example, a 4-frame FRM and 8 x 8 dithering pattern produces 2^6 (256) gray scales on monochrome STN LCDs and 2^{24} (16.8M colors) on color STN LCD.

Table 3–8. Number of Colors On Color STN LCDs

Primary Color RGB			Resulting Image on on Color STN LCD That Has:		
Frame-Rate-Modulation Option	Generated by LCD		32 colors (15 bits)	256K colors (18 bits)	16.8M colors (24 bits)
	Dithering Pattern	No. of Bits			
4 frames (2 bits)	None	0	64 (2^6)		
	2 x 1	1	512 (2^9)		
	2 x 2	2	4K (2^{12})		
	4 x 2	3	32K (2^{15})		
	4 x 4	4	32K (2^{15})	256K (2^{18})	
	8 x 4	5		256K (2^{18})	2M (2^{21})
	8 x 8	6			16.8M (2^{24})
8 frames (3 bits)	None	0	512 (2^9)		
	2 x 1	1	4K (2^{12})		
	2 x 2	2	32K (2^{15})		
	4 x 2	3	32K (2^{15})	256K (2^{18})	
	4 x 4	4		256K (2^{18})	2M (2^{21})
	4 x 8	5			16.8M (2^{24})
16 frames (4 bits)	None	0	4K (2^{12})		
	2 x 1	1	32K (2^{15})		
	2 x 2	2	32K (2^{15})	256K (2^{18})	
	4 x 2	3		256K (2^{18})	2M (2^{21})
	4 x 4	4			16.8M (2^{24})

Table 3–9 shows the number of colors various dithering patterns produce on 512-color TFT LCDs. If an image using the standard VGA 18-bit color palette is displayed on a 512-color TFT LCD (that is, which has only a 9-bit color palette), significant banding or contour lines are readily apparent.

Table 3–9. Number of Colors On 512-Color TFT LCDs

Primary Color RGB Generated by LCD		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	No. of Bits	32K colors (15 bits)	256K colors (18 bits)	16.8M colors (24 bits)
None	0	512 (2^9)		
2 x 1	1	4K (2^{12})		
2 x 2	2	32K (2^{15})	32K (2^{15})	
4 x 2	3		256K (2^{18})	256K (2^{18})
4 x 4	4			2M (2^{21})
8 x 4	5			16.8M (2^{24})

Consequently, the Dithering Engine automatically employs a 4 x 2 pattern to increase the number of displayed colors from the 3 bits per primary color that the LCD produces to the full 6 bits per primary color to meet the 18-bit VGA color palette requirement upon the displayed image's color depth.

- To display a 32-gray-scale image (5 bits), the Dithering Engine automatically adds 3 bits to the 2 bits produced by FRM.
- To display a 64-gray-scale image (6 bits), the Dithering Engine automatically adds 4 bits to the 2 bits produced by FRM.
- To display a 256-gray-scale image (8 bits), the Dithering Engine automatically adds 6 bits to the 2 bits produced by FRM.

The number of bits the Dithering Engine needs to add is reduced when either a 8-frame FRM or a 16-frame FRM is used.

Table 3–10 shows the number of colors various dithering patterns produce on 4K-color TFT LCDs.

Table 3–10. Number of Colors On 4K-Color TFT LCDs

Primary Color RGB Generated By LCD		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	No. of Bits	32K colors (15 bits)	256K colors (18 bits)	16.8M colors (24 bits)
None	0	4K (2^{12})		
2 x 1	1	32K (2^{15})		
2 x 2	2	32K (2^{15})	256K (2^{18})	
4 x 2	3		256K (2^{18})	2M (2^{21})
4 x 4	4			16.8M (2^{24})

Table 3–11 shows the number of colors that dithering patterns produce on 256K-color TFT LCDs.

Table 3–11. Number of Colors On 256K-Color TFT LCDs

Primary Color RGB		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	No. of Bits	32K colors (15 bits)	256K colors (18 bits)	16.8M colors (24 bits)
None	0	32K (2^{15})	256K (2^{18})	256K (2^{18})
2 x 1	1			2M (2^{21})
2 x 2	2			16.8M (2^{24})

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3.2.24 Frequency Synthesizer

The Frequency Synthesizer generates all clock frequencies for VGA and extended modes operation. Using a single reference frequency of 14.31818 MHz that is supplied from an external TTL-level source, the Frequency Synthesizer generates two fully programmable clocks – the memory clock (MCLK) and the video clock (VCLK).

Refer to Figure 3–10 for the Frequency Synthesizer Functional Diagram.

- MCLK
  - MCLK (the memory clock) generates all clocks needed for memory timing signals (for example, RAS*, CAS*, etc.).
  - MCLK must be optimized for the speed of the display memory used.
  - MCLK frequencies are programmed with SR1F.
  - For optimal selection of DRAM speeds, the CL-GD7542 supports MCLKs up to 45 MHz at 3.3V or 50 MHz at 5.0V.
- VCLK
  - VCLK (the video clock), is the fundamental video timing clock which generates all clocks needed for video display timing signals (for example, HSYNC and VSYNC) and for the pixel clock.
  - VCLK must be changed to support various display resolutions and refresh rates.
  - The VCLK frequencies are programmed with registers SRB through SRE and SR1B through SR1F.
  - The CL-GD7542 supports VCLKs up to 65 MHz at 3.3V or 80 MHz at 5.0V.

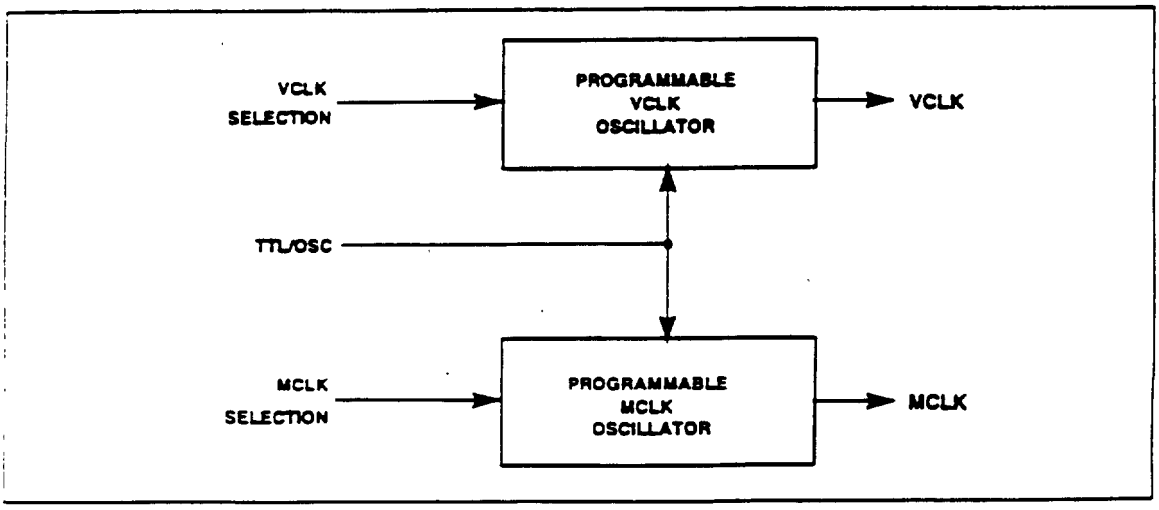


Figure 3–10. Programmable Dual-Frequency Synthesizer Functional Diagram

3.2.25 Power Management

The CL-GD7542 supports a variety of power management techniques to maximize battery life, including:

- LCD-only power savings.
  During LCD-only operations, the video DAC (including its monitor sense comparators) is powered down, and the video clock (VCLK) may be reduced to a level that still minimizes flicker.
- LCD power-up/down sequence control.
  To protect the LCD, the FPVEE and FPVCC output signals control the LCD's power-up and power-down sequence. [Damage can occur if VEE (the LCD's high-voltage power) is applied without VDD (the LCD's logic power)]. The FPBL output signal controls the LCD's backlight enable.
- Mixed-voltage interfaces.
  The host bus, display memory, LCD, and CRT interfaces can each be implemented at either 3.3V or 5V. The voltages used for each interface may be mixed in any combination.
- Standby Mode.
  This mode reduces power consumption by turning off the display while allowing application programs to continue to run normally in the background.

  Standby is entered via the Standby pin, by using the internal Standby Counter, or by programming a register.

  During Standby, using the proper power sequencing, the LCD and CRT are turned off, the video clock (VCLK) is stopped, and the video DAC is powered down. The CPU can still access and modify the display memory and palette.

  The Standby Mode is exited as it is entered, via the Standby pin, by using the internal Standby Counter, or by programming a register.
- Suspend Mode.
  This mode reduces power consumption when the system remains inactive for a relatively long period of time, while maintaining the contents of the controller's registers, palette, and display memory. Unlike Standby mode, however, during the Suspend Mode, applications are suspended and do not continue to run normally in the background.

  Hardware-controlled Suspend is entered via the Suspend Pin. Software-controlled Suspend is entered by setting register CR20[3].

  In contrast to Hardware-controlled Suspend, Software-controlled Suspend allows the CPU to access the internal registers, which requires an active clock and I/O capability, and therefore, more power.

  During Hardware-controlled Suspend, the display is turned off, the video (VCLK) and memory (MCLK) clocks are both stopped, and CPU accesses to the display memory, palette, and I/O registers cease.

  The controller configures display memory for self-refresh or uses the 32-kHz clock for memory refresh.

  Hardware-controlled Suspend is exited via the Suspend Pin. When Suspend Mode is exited, any application programs that were previously running can be quickly re-started from the point at which they suspended.
- VESA Display Power Management.
  The CL-GD7542 supports the VESA Display Power Management Specification for CRT power management to allow systems to comply with the U.S. Environmental Protection Agency's Energy Star Computer qualifications.

For more information, refer to Appendix A9. "Power-Management Solutions".

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3.3 Performance

The CL-GD7542 is designed with the following performance-enhancing features:

- BitBLT Engine.
  The BitBLT Engine is used to accelerate Graphics User Interfaces (GUIs), such as Microsoft Windows.
- Bus Interface Choices.
  The CL-GD7542 provides a choice of bus interfaces for optimum performance:
  - 32-bit VESA VL-Bus
  - '486 local-bus interface
  - PCI bus interface
- CPU Interfaces to I/O registers and memory.
  For increased performance, the CL-GD7542 supports the following CPU interfaces:
  - 32-bit CPU interface to display memory, for faster CPU host access to memory for all modes, including planar modes
  - 16-bit CPU interface to I/O Registers, for faster CPU host access to the registers
- Extended-Write Modes.
  - For faster CPU write performance, the extended-write modes can be used on 8 pixels at a time in 8- or 16-bit/pixel graphics modes that have packed-pixel addressing.
  - These write modes can be used for faster text writing, pattern filling, and block-moving operations in graphics modes.

  For more information, refer to Appendix A4 "Color Expansion and Extended-Write Modes".
- Hardware Cursor.
  GUI performance can be improved by using either the 32 x 32 or the 64 x 64 Hardware Cursor.
- Memory Data Fast Access.
  For faster access to display memory, the CL-GD7542 supports the following:
  - a 32-bit display memory data bus.
  - DRAM Fast-page Mode operations
- Video FIFO.
  Video FIFO minimizes memory contention.
- Zero-wait-state performance.
  For faster CPU access for writes to display memory, the CL-GD7542 provides zero-wait-state performance and a CPU Write Buffer.

3.4 RAMDAC Operation

3.4.1 Writing to the Color Lookup Table

To write a color definition to the Lookup Table, a value specifying an address location in the Lookup Table is first written to the Write Mode Address Register. The color values for the Red, Green, and Blue intensities are then written in succession to the Color Value Register. After the Blue data bits are latched, the new color data bits are then written into the Lookup Table at the defined address, and the CL-GD7542 automatically increments the Address Register.

Since the CL-GD7542 increments the Address Register after each transfer of data to the Lookup Table, it is best to write a set of consecutive locations at once. The start address of the set of locations is first written to the Write Mode Address Register. The color data bits for each address location are then sequentially written to the Color Value Register. After each CPU host transfer of three bytes of color data, the CL-GD7542 automatically writes data to the Lookup Table and increments the Address Register.

3.4.2 Reading from the Color Lookup Table

To read color data from the Lookup Table, a value specifying the address location of the data is written to the Read Mode Address Register. After the address is latched, the data bits from this location are automatically read out to the Color Value Register, and the CL-GD7542 automatically increments the Address Register.

The color intensity values are then read from the Color Value Register by a sequence of three read (RD*) commands. After the Blue value is transferred out, new data bits are read from the Lookup Table's current address to the Color Value Register, which causes the CL-GD7542 to automatically increment the Address Register again.

If the CL-GD7542 loads the Address Register with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This action occurs for both read and write operations.

3.5 Programmable Core Voltage

To optimize graphics performance and power consumption, the CL-GD7542 supports selective switching of the core VDD between 3.3V and 5V, based upon the video mode that is being used.

3.5.1 3.3V Core Voltage

When the CL-GD7542 is operating at 3.3V, the CL-GD7542's memory clock operates up to 45 MHz, which is sufficient for the following pixel modes:

- 1024 x 768 4-bit/pixel
- 800 x 600 8-bit/pixel
- 640 x 480 16-bit/pixel

The core VDD and Analog VDDs must always be at the same voltage.

3.5.2 5.0V Core Voltage

When the CL-GD7542 is operating at 5.0V, the CL-GD7542's memory clock should be at 50 MHz to maximize performance in the following pixel modes

- 1024 x 768 8-bit/pixel
- 800 x 600 16-bit/pixel
- 640 x 480 24-bit/pixel modes

The core VDD and Analog VDDs (which must always be at the same voltage) should be 5V with a 50 MHz memory clock.

3.6 Compatibility

The CL-GD7542 includes all registers and data paths required for standard VGA controllers. It also supports the following extended VGA modes:

- 1024 x 768 with 256 colors (interlaced and non-interlaced modes)
- 1280 x 1024 with 256 colors (interlaced modes)

Additionally, various 132-column text modes are supported

3.7 Extension Registers

While expanding or centering VGA modes on 640 x 480 or 800 x 600 LCDs, the appropriate VGA registers are shadowed, for VGA compatibility.

3.8 Testability

The CL-GD7542 chip is testable by using Pin-Scan Testing and a Signal Generator.

Pin-scan testing tests the signal state of every pin on the chip. Any pins that are not connected to the board, or which are shorted to a neighboring pin or trace will be detected. For more information, refer to Appendix A11, "Pin-Scan Testing."

The Signature Generator allows the entire system, including display memory, to be tested at speed. For more information, refer to Appendix A10, "Signature Generator".

3.9 Configuration Inputs

To configure the chip for operation, the CL-GD7542 uses a combination of hardware and software configurations.

3.9.1 Hardware Configuration Inputs

Pull-up resistors are used on some of the memory data pins, which are read during the low-to-high transition of the Reset# pulse or when the External Pull-Up Reset register SR24[3] is toggled.

- 32-bit PCI Bus.
  This configuration selects the 32-bit PCI bus with Min-grant timing of 8 PCI CLKs (-250 ns at 33 MHz).
- 32-bit PCI Bus with Min-Grant Extended.
  This configuration selects the 32-bit PCI bus, but with Min-grant timing extended from 8 PCI CLKs (-250 ns at 33 MHz) to 16 PCI CLKs (-500 ns at 33MHz), allowing burst write mode capability.
- Enable Feature Connector.
  This configuration uses the appropriate pins for the Feature Connector video port. (Refer to Pin Descriptions in Chapter 1. and Chapter 2. for the affected pins).

- Sleep Address Select.
  This configuration selects either I/O address 46E8h or 3C3h (the default) as the sleep address.
- VESA VL-Bus with 50-MHz MCLK.
  This configuration sets the VL-Bus for >33 MHz local bus operation.

If no resistors are present, the above pins are read as low because of the internal pull-down resistors. The status of these inputs is stored in registers SR22 and SR24.

Three hardware switch inputs (SW[2:0]) are read during each horizontal retrace period. These inputs are used by the BIOS to monitor external activities that can affect the chip operation. The status of these three inputs is stored in SR24[2:0].

3.9.2 Software Configuration Inputs

A software programmable register, SR23, is used to select the desired function of some multi-function pins as defined below:

- ACTI / FCEVIDEO# / SBYI Select.
  Registers SR23[6] and SR24[7] configure the ACTI / FCEVIDEO# / SBYI input (pin 86) as either the Activity Sense input or the hardware-controlled Standby input.
- BLI / SUSPI Enable.
  Registers SR23[5] and SR24[7] configure the BLI / SUSPI input (pin 87) as either the Hardware-Controlled Suspend input or the Backlight input control.
- FCDCLK Output Select.
  Register SR24[4] is used to output either the VCLK or PCLK0 on the FCDCLK pin.
- FCVCLK Enable.
  Register SR23[7] selects whether FCVCLK is sent to the DAC only or is also used for VCLK generation.
- VCLK Output Enable.
  Registers SR23[4] and SR24[7] either make the VCLK output pin low or output the internal VCLK on the FCDCLK / VCLK output (pin 103).

For more configuration information, refer to Appendix A14, "Configuration Notes" and Section 2.7.

3.10 Software Support

The CL-GD7542 supports big-endian word swapping, which allows it to load either x86 little-endian data or PowerPC big-endian data into display memory, depending upon the application requirements.

A VGA BIOS, which is fully compatible with the standard IBM VGA BIOS and the Interrupt 10h video service functions, is available from Cirrus Logic and third-party BIOS vendors.

The Cirrus Logic CL-GD7542 VGA BIOS is a high-quality, feature-rich firmware product designed to take maximum advantage of the CL-GD7542 controller, especially in the areas of display quality, power management, and graphics performance. The key features of the VGA BIOS are:

- Super VGA-compatible BIOS
- Supports SimulSCAN operation (simultaneous LCD and CRT display)
- Supports the power-management modes
- Supports display-enhancement features
- Can be integrated with the system BIOS
- Supports switchless configuration
- Can be customized without source code through use of utility programs such as OEMSI
- Provides VESA-compatible modes and 1.2-function support for Video BIOS Extensions (VBE)
- Supports multiple monitor refresh rates

The CL-GD7542 VGA controller and BIOS can be implemented as an adapter board or placed directly on the system board. The VESA local bus BIOS can be located at C000h or E000h. There is a separate BIOS for PCI bus implementations.

The core BIOS requires 32 KBytes. Extra functionality, such as EGA-compatible fonts, can be located in a 16-KByte optional BIOS. This optional BIOS may be either appended to the core BIOS (for VL-bus or PCI bus implementations) or loaded into the same segment as the core BIOS (for VL-bus implementations). For system implementations which do not have ROM space for the 16-KByte optional BIOS, a TSR is provided to support the extra functionality in DOS environments.

3.10.1 Software Support for OEMs

Cirrus Logic provides the following CL-GD7542 software utilities for OEM development use:

- CL_STEST.
  This utility is a DOS-based screen-testing utility that provides for the following:
  - CL_STEST enables the user to display and adjust the position and RGB color of a variety of patterns (including color bars, lines and rectangles) to test the display's quality.
  - CL_STEST may operate with pixel resolutions of:
    - 640 x 400
    - 640 x 480
    - 800 x 600
    - 1024 x 768
- CLPanel.
  This utility is a DOS-based LCD-parameter optimization utility that provides for the following:
  - Via a serial link to an external monitor, CLPanel enables a variety of LCD parameters to be adjusted.
  - CLPanel may be used to view a variety of display test images and bit-map (BMP) images.
  - CLPanel may be used to switch the active display between LCD, CRT, or SimulScan modes.
- CLRegs.
  This utility is a DOS-based VGA-controller register viewer/editor utility that provides for the following.
  - CLRegs enables users to easily view and edit the CL-GD7542's standard VGA and extension registers and color palette.
  - The CLRegs Help screen provides a brief explanation of each bit in each register.
  - CLRegs enables register values to be changed by typing in a new hex value or toggling individual bits.
  - CLRegs also displays a variety of the CL-GD7542's configuration data, including the status of the CRT Controller, the graphics mode being used, information about the video BIOS, and hardware cursor information.
- CLView.
  This utility is a DOS-based image-viewing utility that provides for the following:
  - CLView loads the following types of image files: BMP, Graphics Interchange Format (GIF), TGA, or PCX.
  - The CLView's full-screen menu lists all current BMP, GIF, TGA, or PCX image files.
  - By pressing a CLView function key, each image's width, height, bits per pixels, number of colors, and file size can be displayed.
  - CLView allows image files to be marked for inclusion in a slide show.
  - CLView may be used to switch the active display between LCD, CRT, or SimulScan modes.
- OEMSI.
  This utility is a Cirrus Logic BIOS-customization utility for OEM development use.

3.10.2 Software Support for End Users

Cirrus Logic provides the following CL-GD7542 software utilities for distribution to end users:

- CL_Mode.
  CL_Mode is a DOS-based graphics-mode utility and display-configuration utility.
  - CL_Mode's user-friendly VGA Configuration menu enables users to turn "on" and "off" a variety of graphics configuration options, including the following:
    - automatic text expansion
    - bold fonts
    - power-management options
    - reverse video
    - shading of graphics and text
    - text enhancement
    - vertical position of display
  - CL_Mode's Monitor Type Setup menu enables users to set CRT monitor resolution and refresh rate.
  - CL_Mode's Video Modes Preview menu en-

ables users to display the various VGA modes.
  - New settings of the above options enabled by the user can be updated in the AUTOEXEC.BAT file by this program.
- CLVESA.
  This utility is a Terminate-and-Stay-Resident (TSR) utility that supports the VESA BIOS extensions.
- CSwitcher.
  This utility is a video-configuration TSR.
- SETRES.
  This utility is a Windows application for defining the resolution and bit depth of the CL-GD7542 Windows Driver.
  - SETRES enables users to set the CRT resolution to: 640 x 480, 800 x 600, 1024 x 768, or 1280 x 1024
  - SETRES enables users to select bit depth used on either the CRT or LCD, such as: 16, 256, 64K, or 16.8M.
  - SETRES enables users to turn the Hardware Cursor "on" and "off".
  - SETRES enables users to make the font size normal or large.
- WinMode.
  This utility is a Windows application for video-mode configurations.
- WinPanel.
  This utility is very similar in operation to CL_MODE, and performs the same basic functions in the Windows environment.
  - WinPanel enables users to turn "on" and "off" a variety of graphics configuration options, including:
    - automatic text expansion
    - bold fonts
    - power-management options (such as the timer intervals for Standby mode or backlight)
    - reverse video
    - shading of graphics and text
    - text enhancement
    - vertical position of display
  - WinPanel allows users to select between LCD, CRT, or SimulScan display options.
  - WinPanel allows users to set high-refresh rates for CRT monitors.
  - New settings of the above options enabled by the user can be updated in the AUTOEXEC.BAT file by this program.

3.11 Package

The CL-GD7542 is available in a standard EIAJ 208-pin QFP package with a 28 x 28 mm body size and 0.5 mm lead pitch.

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4. CL-GD7542 Video Mode Tables

This chapter lists tables for configuring the CL-GD7542 for various CRT and flat-panel video modes. For detailed information on specific LCD flat panels that the CL-GD7542 can drive, refer to the CL-GD7542 *Panel Interface Guide* for details.

NOTE: The parameters detailed in the tables of Chapter 4 define standard capabilities of the CL-GD7542 when it is used with the Cirrus Logic Video BIOS. Consult with the appropriate BIOS vendor for information about the modes and parameters supported by those video BIOSes that are not from Cirrus Logic.

4.1 Video Modes: CRT-Only

This section lists IBM Standard VGA and Cirrus Logic Extended CRT-only video modes.

4.1.1 IBM® Standard VGA CRT-Only Video Modes

The IBM® Standard VGA video BIOS supports the CRT-only video modes listed in Table 4–1.

Table 4–1. IBM® Standard VGA CRT-Only Video Modes

Mode Number (hex)	Number of Colors	Characters x Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horizontal Freq. (kHz)	Vertical Frequency (Hz)	Minimum MCLK (MHz)
0, 1	16/256K	40 x 25	9 x 16	360 x 400	Text	28	31.5	70	36
2, 3	16/256K	80 x 25	9 x 16	720 x 400	Text	28	31.5	70	36
4, 5	4/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	36
6	2/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70	36
7	Mono.	80 x 25	9 x 16	720 x 400	Text	28	31.5	70	36
D	16/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	36
E	16/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70	36
F	Mono.	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70	36
10	16/256K	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70	36
11	2/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	36
12	16/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	36
12[a]	16/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	72	36
13	256/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	36

a Modes denoted by (a) are IBM® Standard VGA modes that have been enhanced by Cirrus Logic for a higher vertical frequency.

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4.1.2 Cirrus Logic Extended CRT-Only Video Modes

The Cirrus Logic video BIOS supports the extended CRT-only video modes listed in Table 4–2. (Columns one and two compare the hex number of the Cirrus Logic extended CRT-only video mode with the hex number of the equivalent VESA CRT-only video mode.)

- If the BIOS used is not the Cirrus Logic BIOS, modes may differ.
- Some video modes are not supported by all monitors.
- For the monitor type that is selected, the best-quality vertical refresh rate will be used automatically.

Table 4–2. Cirrus Logic Extended CRT-Only Video Modes

Mode No. (hex)	VESA No. (hex)	Number of Colors	Characters x Rows	Chara. Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Min. MCLK (MHz)[g]
11[a]	–	2/256	80 x 30	6 x 16	640 x 480	Graphics	31.5	37.9	75[a]	36
12[a]	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	75[a]	36
tbd[b]	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	36
16[b]	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	75	36
14	–	16/256K	132 x 25	8 x 16	1056 x 400	Text	41.5	31.5	70	45
54	10A	16/256K	132 x 43	8 x 8	1056 x 350	Text	41.5	31.5	70	45
55	109	16/256K	132 x 25	8 x 14	1056 x 350	Text	41.5	31.5	70	45
58, 6A[c]	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56	40
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.8	60	40
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72	45
tbd[b]	–	16/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.8	60	40
17[b]	–	16/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	75	45
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56	40
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.9	60	45
5C[a]	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	50[a]	48.1	72	40
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60	45
5D[c]	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87[c]	40
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70	50
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	75	50
tbd[b]	–	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60	45
18[b]	–	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	75	50
5E	100	256/256K	80 x 25	8 x 16	640 x 400	Graphics	25	31.5	70	36
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	36
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	72	36
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87[c]	40
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60	45
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70	50

Table 4–2. Cirrus Logic Extended CRT-Only Video Modes (Continued)

Mode No. (hex)	VESA No. (hex)	Number of Colors	Characters x Rows	Chara. Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Min. MCLK (MHz)[g]
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	75	50
64	111	64K	–	–	640 x 480	Graphics	25	31.5	60	45
64	111	64K	–	–	640 x 480	Graphics	31.5	37.9	75	45
65	114	64K	–	–	800 x 600	Graphics	36	35.2	56	50
65	114	64K	–	–	800 x 600	Graphics	40	37.8	60	45
66[e]	110	32K[e]	–	–	640 x 480	Graphics	25	31.5	60	45
66[e]	110	32K[e]	–	–	640 x 480	Graphics	31.5	37.9	75	45
67[e]	113	32K[e]	–	–	800 x 600	Graphics	36	31.5	56	50
6C[c]	106	16/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87[c]	50
6C[c]	–	256/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87[c]	50
71	112	16M	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	50
74[c]	–	64K	–	–	1024 x 768	Graphics	44.9	35.5	87[c]	45
tbd[f]	–	16/256	80 x 25	8 x 8	640 x 200	Text	13.5	tbd	tbd	45
tbd[f]	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	13.5	tbd	tbd	45
tbd[f]	–	256/256K	80 x 30	8 x 16	640 x 480	Graphics	13.5	tbd	tbd	45

a Modes denoted by (a) are IBM® Standard VGA modes that have been enhanced by Cirrus Logic for a higher vertical frequency

b. Modes denoted by (b) are 4-bit-per-pixel packed-pixel modes.

c All modes with (Vertical Frequency = 87 Hz) are interlaced modes.

d Application programs should use mode 6A, rather than mode 58, to retain compatibility with other VGA BIOS products

e Modes denoted by (e) are true-color packed-pixel mode.

f Modes denoted by (f) are interlaced modes for NTSC-OUT functions.

g The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the controller may be run without any adverse effects to the function of the controller. Better benchmark performance may be achieved with an MCLK frequency other than the frequency specified in this column.

h These modes are NOT available when the controller is operated with a core VDD of 3.3VDC. For the full operational range of the clocks at 3.3VDC, refer to Chapter 7, for the electrical specification section of this document.

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4.2 Video Modes: LCD Only

This section lists IBM Standard VGA and Cirrus Logic Extended LCD-only video modes.

4.2.1 IBM® Standard VGA LCD-Only Video Modes

The IBM® Standard VGA BIOS supports the LCD-only video modes listed in Table 4–3.

Table 4–3. IBM® Standard VGA LCD-Only Video Modes

Mode No. (hex)	Mono. STN No. of Shades	Color STN No. of Colors	Color TFT No. of Colors	Characters x Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Expanded Panel (pixels)
0, 1	16/16	16/256K	16/256K	40 x 25	8 x 16	360 x 400	Text	640 x 475
2, 3	16/16	16/256K	16/256K	80 x 25	8 x 16	720 x 400	Text	36
4, 5	4/64	4/256K	4/256K	40 x 25	8 x 8	320 x 200	Graphics	36
6	2/16	2/256K	2/256K	80 x 25	8 x 8	640 x 200	Graphics	36
7	2/16	Mono.	Mono.	80 x 25	8 x 16	720 x 400	Text	36
D	16/64	16/256K	16/256K	40 x 25	8 x 8	320 x 200	Graphics	36
E	16/16	16/256K	16/256K	80 x 25	8 x 8	640 x 200	Graphics	36
F	2/16	Mono.	Mono.	80 x 25	8 x 14	640 x 350	Graphics	36
10	16/16	16/256K	16/256K	80 x 25	8 x 14	640 x 350	Graphics	36
11	2/16	2/256K	2/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
12	16/16	16/256K	16/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
13	64/256K	256/256K	256/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 475

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4.2.2 Cirrus Logic Extended LCD-Only Video Modes

The extended LCD-only video modes listed in Table 4–4 are supported by the Cirrus Logic video BIOS. (Columns one and two compare the hex number of the Cirrus Logic extended LCD-only video mode with the hex number of the equivalent VESA LCD-only video mode.)

- If the BIOS used is not the Cirrus Logic BIOS, modes may differ.
- Some video modes are not supported by all monitors.
- For the monitor type that is selected, the best-quality vertical refresh rate will be used automatically.

Table 4–4. Cirrus Logic Extended LCD-Only Video Modes

Mode No. (hex)	VESA No. (hex)	Number of Colors	Characters x Rows	Chara. Cell (pixels)	Screen Format (pixels)	Graphics Panel Type	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Min. MCLK (MHz)[d]
16[a]	–	16/256K	80 x 30	8 x 16	640 x 480	STN/TFT	31.5	tbd	tbd	36
58, 6A[b]	102	16/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	40
17	–	16/256K	100 x 37	8 x 16	800 x 600	STN/TFT	50	tbd	tbd	45
5C	103	256/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	40
5E	100	256/256K	80 x 25	8 x 16	640 x 400	STN/TFT	25	tbd	tbd	36
5F	101	256/256K	80 x 30	8 x 16	640 x 480	STN/TFT	31.5	tbd	tbd	36
64	111	64K	–	–	640 x 480	TFT	25	tbd	tbd	50
65	114	64K	–	–	800 x 600	TFT	36	tbd	tbd	50
66[c]	110	32K[c]	–	–	640 x 480	TFT	25	tbd	tbd	50
67[c]	113	32K[c]	–	–	800 x 600	TFT	36	tbd	tbd	50
71	112	16M	80 x 30	8 x 16	640 x 480	TFT	25	tbd	tbd	50

a. Modes denoted by (a) are 4-bit-per-pixel packed-pixel modes.

b Application programs should use mode 6A, rather than mode 58, to retain compatibility with other VGA BIOS products.

c Modes denoted by (c) are true-color packed-pixel mode.

d The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the controller may be run without any adverse effects to the function of the controller. Better benchmark performance may be achieved with an MCLK frequency other than the frequency specified in this column.

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4.3 Video Modes: SimulSCAN

This section lists IBM Standard VGA and Cirrus Logic Extended SimulSCAN video modes.

4.3.1 IBM® Standard VGA SimulSCAN Video Modes

The IBM® Standard VGA video BIOS supports the SimulSCAN video modes listed in Table 4–5.

Table 4–5. IBM® Standard VGA SimulSCAN Video Modes

Mode No. (hex)	Mono. STN No. of Shades	Color STN No. of Colors	Color TFT No. of Colors	Characters x Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Expanded Panel (pixels)
0, 1	16/16	16/256K	16/256K	40 x 25	8 x 16	360 x 400	Text	640 x 475
2, 3	16/16	16/256K	16/256K	80 x 25	8 x 16	720 x 400	Text	640 x 475
4, 5	4/64	4/256K	4/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 475
6	2/16	2/256K	2/256K	80 x 25	8 x 8	640 x 200	Graphics	640 x 475
7	2/16	Mono.	Mono.	80 x 25	8 x 16	720 x 400	Text	640 x 475
D	16/64	16/256K	16/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 475
E	16/16	16/256K	16/256K	80 x 25	8 x 8	640 x 200	Graphics	640 x 475
F	2/16	Mono.	Mono.	80 x 25	8 x 14	640 x 350	Graphics	640 x 475
10	16/16	16/256K	16/256K	80 x 25	8 x 14	640 x 350	Graphics	640 x 475
11	2/16	2/256K	2/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
12	16/16	16/256K	16/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
13	64/256K	256/256K	256/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 480

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4.3.2 Cirrus Logic Extended SimulSCAN Video Modes

The extended SimulSCAN video modes listed in Table 4–6 are supported by the Cirrus Logic video BIOS. (Columns one and two compare the hex number of the Cirrus Logic extended SimulSCAN video mode with the hex number of the equivalent VESA SimulSCAN video mode.)

- If the BIOS used is not the Cirrus Logic BIOS, modes may differ.
- Some video modes are not supported by all monitors.
- For the monitor type that is selected, the best-quality vertical refresh rate will be used automatically.

Table 4–6. Cirrus Logic Extended SimulSCAN Video Modes

Mode No. (hex)	VESA No. (hex)	Number of Colors	Characters x Rows	Chara. Cell (pixels)	Screen Format (pixels)	Graphics Panel Type	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Min. MCLK (MHz)[e]
16[a]	–	16/256K	80 x 30	8 x 16	640 x 480	STN/TFT	25	tbd	tbd	40
58, 6A[b]	102	16/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	45
17	–	16/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	45
5C	103	256/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	45
5E	100	256/256K	80 x 25	8 x 16	640 x 400	STN/TFT	25	tbd	tbd	40
5F	101	256/256K	80 x 30	8 x 16	640 x 480	STN/TFT	25	tbd	tbd	45
64	111	64K	–	–	640 x 480	TFT	25	tbd	tbd	50
65[d]	114	64K	–	–	800 x 600	TFT	36	tbd	tbd	50[d]
66[c]	110	32K[c]	–	–	640 x 480	TFT	25	tbd	tbd	50
67[c,d]	113	32K[c]	–	–	800 x 600	TFT	36	tbd	tbd	50[d]
71[d]	112	16M	80 x 30	8 x 16	640 x 480	TFT	25[f]	tbd	tbd	50[d]

a Modes denoted by (a) are 4-bit-per-pixel packed-pixel modes.

b Application programs should use mode 6A, rather than mode 58, to retain compatibility with other VGA BIOS products.

c Modes denoted by (c) are true-color packed-pixel mode.

d Modes denoted by (d) indicate that dual-scan color LCDs do not support SimulSCAN on these modes.

e The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the controller may be run without any adverse effects to the function of the controller. Better benchmark performance may be achieved with an MCLK frequency other than the frequency specified in this column.

f These modes are NOT available when the controller is operated with a core VDD of 3.3VDC. For the full operational range of the clocks at 3.3VDC, refer to the Electrical Specification section of this document.

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5. VGA Register Port Map

Table 5–1. VGA Register Port Map

Address	Port	Port Type
94	POS 102 Access Control (3C3 Sleep)	
102	POS 102 Register	
3B4	CRT Controller Index — Monochrome	Read/Write
3B5	CRT Controller Data — Monochrome	Read/Write
3BA	Feature Control — Monochrome	Write
	Input Status Register 1 — Monochrome	Read
3C0	Attribute Controller Index / Data	Write
3C1	Attribute Controller Index / Data	Read
3C2	Miscellaneous Output	Write
	Input Status Register 0	Read
3C3	Motherboard Sleep	Read/Write
3C4	Sequencer Index	Read/Write
3C5	Sequencer Data	Read/Write
3C6	Video DAC Pixel Mask (R/W), Hidden DAC Register	Read/Write
3C7	Pixel Address Read mode	Write
	DAC State	Read
3C8	Pixel Mask Write Mode	Read/Write
3C9	Pixel Data	Read/Write
3CA	Feature Control Readback	Read
3CC	Miscellaneous Output Readback	Read
3CE	Graphics Controller Index	Read/Write
3CF	Graphics Controller Data	Read/Write
3D4	CRT Controller Index — Color	Read/Write
3D5	CRT Controller Data — Color	Read/Write
3DA	Feature Control — Color	Write
	Input Status Register 1 — Color	Read
46E8	Adapter Sleep	Read/Write

6. CL-GD7542 Registers

6.1 Register Summary

6.1.1 Introduction to Registers

The registers in this chapter include standard VGA registers, as well as extension registers added by Cirrus Logic.

6.1.2 Summary of External/General Registers in Section 6.2

The External and General Registers in the CL-GD7542 are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
MISC	Miscellaneous Output Register	–	3C2 (Write)	103
MISC	Miscellaneous Output Register	–	3CC (Read)	103
FC	Feature Control Register	–	3?A (Write)	106
FC	Feature Control Register	–	3CA (Read)	106
FEAT	Input Status Register 0	–	3C2	107
STAT	Input Status Register 1	–	3?A	108
3C3	Sleep-Mode Register	–	3C3	112
3C6	Pixel Mask Register	–	3C6	110
3C7	Pixel Address Read Mode Register	–	3C7 (Write)	111
3C7	DAC State Register	–	3C7 (Read)	112
3C8	Pixel Address Write Mode Register	–	3C8	113
3C9	Pixel Data Register	–	3C9	114
PCI00	PCI Device/Vendor ID Register	–	00	115
PCI04	PCI Command Register	–	04	116
PCI04	PCI Status Register	–	04	117
PCI10	PCI Base Address Register	–	10	118
PCI3C	PCI Interrupt Line and Interrupt Pin Register	–	3C	119
46E8	Alternate Sleep-Mode Register	–	46E8	112

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

6.1.3 Summary of Sequencer Registers in Section 6.3

The CL-GD7542 Sequencer Registers are summarized in the following table. Note that there are Extension Registers that are accessed using the Sequencer Ports.

Abbreviation	Register Name	Index	Port	Page
SRX	Sequencer Index Register	–	3C4	123
SR0	Reset Register	0	3C5	125
SR1	Clocking Mode Register	1	3C5	126
SR2	Plane Mask Register	2	3C5	128
SR3	Character Map Select Register	3	3C5	129
SR4	Memory Mode Register	4	3C5	131

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6.1.4 Summary of CRT Controller Registers in Section 6.4

The CL-GD7542 VGA CRT Controller Registers are summarized in the following table. Note that there are Extension Registers that are accessed using the VGA CRT Controller Ports.

Abbreviation	Register Name	Index	Port	Page
CRX	CRTC Index Register	–	3?4	135
CR0	Horizontal Total Register	0	3?5	136
CR1	Horizontal Display End Register	1	3?5	139
CR2	Horizontal Blanking Start Register	2	3?5	140
CR3	Horizontal Blanking End Register	3	3?5	141
CR4	Horizontal Sync Start Register	4	3?5	143
CR5	Horizontal Sync End Register	5	3?5	144
CR6	Vertical Total Register	6	3?5	146
CR7	Overflow Register	7	3?5	147
CR8	Screen A Preset Row Scan Register	8	3?5	148
CR9	Character Cell Height Register	9	3?5	149
CRA	Text Cursor Start Register	A	3?5	150
CRB	Text Cursor End Register	B	3?5	151
CRC	Screen A Start Address High Register	C	3?5	152
CRD	Screen A Start Address Low Register	D	3?5	153
CRE	Text Cursor Location High Register	E	3?5	154
CRF	Text Cursor Location Low Register	F	3?5	155
CR10	Vertical Sync Start Register	10	3?5	156
CR11	Vertical Sync End Register	11	3?5	157
CR12	Vertical Display End Register	12	3?5	159
CR13	Offset Register	13	3?5	160
CR14	Underline Row Scanline Register	14	3?5	161
CR15	Vertical Blanking Start Register	15	3?5	162
CR16	Vertical Blanking End Register	16	3?5	163
CR17	Mode Control Register	17	3?5	164
CR18	Line Compare Register	18	3?5	166
CR22	Graphics Data Latches Read-back Register	22	3?5	167
CR24	Attribute Controller Toggle Read-back Register	24	3?5	168
CR26	Attribute Controller Index Read-back Register	26	3?5	169

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

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6.1.5 Summary of Graphics Controller Registers in Section 6.5

The CL-GD7542 Graphics Controller Registers are summarized in the following table. Note that there are Extension Registers that are accessed using the Graphics Controller Port.

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index Register	–	3CE	173
GR0	Set/Reset Register	0	3CF	174
GR1	Set/Reset Enable Register	1	3CF	175
GR2	Color Compare Register	2	3CF	176
GR3	Data Rotate Register	3	3CF	177
GR4	Read Map Select Register	4	3CF	178
GR5	Mode Register	5	3CF	179
GR6	Miscellaneous Register	6	3CF	183
GR7	Color Don't Care Register	7	3CF	184
GR8	Bit Mask Register	8	3CF	185

6.1.6 Summary of Attribute Controller Registers in Section 6.6

The CL-GD7542 Attribute Controller Registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index Register	–	3C0/3C1	189
AR0-ARF	Attribute Controller Palette Registers	0:F	3C0/3C1	190
AR10	Attribute Controller Mode Register	10	3C0/3C1	191
AR11	Overscan (Border) Color Register	11	3C0/3C1	193
AR12	Color Plane Enable Register	12	3C0/3C1	194
AR13	Pixel Panning Register	13	3C0/3C1	196
AR14	Color Select Register	14	3C0/3C1	197

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6.1.7 Summary of Extension Registers in Section 6.7

The CL-GD7542 Extension Registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
SR6	Unlock All Extensions Register	6	3C5	201
SR7	Extended Sequencer Mode Register	7	3C5	202
SR8	Miscellaneous Control Register	8	3C5	205
SR9	Scratch-Pad 0 Register	9	3C5	206
SRA	Scratch-Pad 1 Register	A	3C5	206
SRB	VCLK0 Numerator Register	B	3C5	207
SRC	VCLK1 Numerator Register	C	3C5	207
SRD	VCLK2 Numerator Register	D	3C5	207
SRE	VCLK3 Numerator Register	E	3C5	207
SRF	DRAM Control Register	F	3C5	209
SR10	Graphics Cursor and Icon Horizontal Position Register	10	3C5	211
SR11	Graphics Cursor and Icon Vertical Position Register	11	3C5	213
SR12	Video Data Path Control Register	12	3C5	214
SR13	Graphics Cursor Pattern Address Offset Register	13	3C5	217
SR14	Scratch-Pad 2 Register	14	3C5	218
SR15	Scratch-Pad 3 Register	15	3C5	218
SR16	Performance Tuning Register	16	3C5	219
SR18	Signature Generator Control Register	18	3C5	221
SR19	Signature Generator Result Low Byte Register	19	3C5	223
SR1A	Signature Generator Result High Byte Register	1A	3C5	224
SR1B	VCLK0 Denominator and Post-Scalar Value Register	1B	3C5	225
SR1C	VCLK1 Denominator and Post-Scalar Value Register	1C	3C5	225
SR1D	VCLK2 Denominator and Post-Scalar Value Register	1D	3C5	225
SR1E	VCLK3 Denominator and Post-Scalar Value Register	1E	3C5	225
SR1F	MCLK Frequency and VCLK Source Select Register	1F	3C5	226
SR20	Miscellaneous Control Register	20	3C5	227
SR21	Dual-scan Color Control Register	21	3C5	228
SR22	Hardware Configuration Register	22	3C5	229
SR23	Software Configuration #1 Register	23	3C5	231
SR24	LCD Type Switch and FC Enable Register	24	3C5	233
SR25	Timer-Software Reset and Hardware Configuration Register	25	3C5	235
SR26	Shader Signature — Least-Significant Byte	26	3C5	237
SR27	Shader Signature — Most-Significant Byte	27	3C5	238
SR2A	Hardware Icon #0 Control	2A	3C5	239
SR2B	Hardware Icon #1 Control	2B	3C5	240
SR2C	Hardware Icon #2 and Miscellaneous PCI Control	2C	3C5	242
SR2D	Hardware Icon #3 and HIMEM Select Control	2D	3C5	247
SR2E	Graphics-Cursor Horizontal-Position Extension	2E	3C5	245
SR2F	Half-Frame-Accelerator Threshold	2F	3C5	247

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6.1.7 Summary of Extension Registers in Section 6.7 (cont.)

The CL-GD7542 Extension Registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
	Graphic-Controller Extension Registers			
GR9	Offset Register 0	9	3CF	248
GRA	Offset Register 1	A	3CF	250
GRB	Graphics Controller Mode Extensions Register	B	3CF	251
GRC	Color Key Compare Register	C	3CF	253
GRD	Color Key Compare Mask Register	D	3CF	254
GRE	PCI-Burst and Green-PC Control Register	E	3CF	256
GR10	16-bit Pixel Background Color High Byte Register	10	3CF	257
GR11	16-bit Pixel Foreground Color High Byte Register	11	3CF	258
GR20	BLT Width Low Register	20	3CF	259
GR21	BLT Width High Register	21	3CF	260
GR22	BLT Height Low Register	22	3CF	261
GR23	BLT Height High Register	23	3CF	262
GR24	BLT Destination Pitch Low Register	24	3CF	263
GR25	BLT Destination Pitch High Register	25	3CF	264
GR26	BLT Source Pitch Low Register	26	3CF	265
GR27	BLT Source Pitch High Register	27	3CF	266
GR28	BLT Destination Start Low Register	28	3CF	267
GR29	BLT Destination Start Mid Register	29	3CF	268
GR2A	BLT Destination Start High Register	2A	3CF	269
GR2C	BLT Source Start Low Register	2C	3CF	270
GR2D	BLT Source Start Mid Register	2D	3CF	271
GR2E	BLT Source Start High Register	2E	3CF	272
GR30	BLT Mode Register	30	3CF	273
GR31	BLT Start/Status Register	31	3CF	276
GR32	BLT Raster Operation Register	32	3CF	277
GR34	BLT Transparent Color Select Low Register	34	3CF	278
GR35	BLT Transparent Color Select High Register	35	3CF	279
GR38	BLT Source Transparent Color Mask Low Register	38	3CF	315
GR39	BLT Source Transparent Color Mask High Register	39	3CF	281

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6.1.7 Summary of Extension Registers in Section 6.7 (cont.)

Abbreviation	Register Name	Index	Port	Page
	Control Extension Registers			
CR19	Interlace End	19	3?5	282
CR1A	Miscellaneous Control	1A	3?5	283
CR1B	Extended Display Controls	1B	3?5	285
CR1D	Overlay Mode Controls	1D	3?5	287
CR1E	LCDShading	1E	3?5	288
CR1F	LCD Modulation Control	1F	3?5	290
CR20	Power Management	20	3?5	292
CR21	Power-down Timers	21	3?5	294
CR23	FPVCC, FPBL, SUSPEND-Debounce Control	23	3?5	296
CR25	MFG Revision Register	25	3?5	298
CR27	ID Register	27	3?5	307
CR29	CL-GD7542 Configuration Status	29	3?5	308
CR2C	LCD Interface	2C	3?5	301
CR2D	LCD Display Control	2D	3?5	304
CR2E	High-resolution LCD Control	2E	3?5	306
CR2F	Drivers and BIOS Revision Register	2F	3?5	307
CR30	TV-OUT Control	30	3?5	308
	MotionVideo™ Window (MVW) Control Registers			
CR33	MVW Horizontal XS and XW Overflow	33	3?5	310
CR34	MVW Horizontal-Start XS	34	3?5	308
CR35	MVW Horizontal-Width XW	35	3?5	312
CR36	MVW Vertical-Position High and YUV to RGB Convert	36	3?5	313
CR37	MVW Vertical Position Start YS	37	3?5	314
CR38	MVW Vertical Position End YE	38	3?5	315
CR39	MVW Surrounding Address Offset	39	3?5	316
CR3A	MVW Memory-Address Start	3A	3?5	317
CR3B	MVW Memory-Address Offset	3B	3?5	318
CR3C	MVW Zoom, Enable and Encoding Format	3C	3?5	319
CR3D	MVW Horizontal Size	3D	3?5	320

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

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6.1.7 Summary of Extension Registers in Section 6.7 (cont.)

Abbreviation	Register Name	Index	Port	Page
	LCD Horizontal-Timing Control Registers			
CR40	LCD Horizontal-Display-Enable Start – No Centering	40	3?5	321
CR41	LCD HDE Start Register to Center 720 Dots	41	3?5	323
CR42	LCD HDE Start Register to Center 640 Dots	42	3?5	324
CR43	LCD Dot-Clock Skew-Control	43	3?5	325
CR44	LCD Horizontal-Width	44	3?5	327
CR47	TFT Horizontal Position	47	3?5	324
CR48	TFT-HSYNC and LCD-Height Overflow	48	3?5	324
CR49	Vertical Size for Upper-half of Dual-scan STN LCDs	49	3?5	324
CR4A	Vertical Size for LCD LCDs	4A	3?5	324
CR4B	Reserved for Scratch Pad	4B	3?5	324
CR4C	Input-Resolution Override for Dithering	4C	3?5	324
CR4D	Output Resolution for Dithering	4D	3?5	324
CR4E	MVA Input-Resolution Override for Dithering	4E	3?5	337
HDR	Hidden DAC Register	–	3C6	339
	LCD Timing Registers			
R2X	LFS Vertical Counter Value Compare (not centered)	2	3?5	343
R3X	LFS Vertical Counter Value Compare (centered)	3	3?5	345
R4X	LFS Vertical Counter Value Compare (centered)	4	3?5	346
R5X	LFS Vertical Counter Value Compare (centered)	5	3?5	347
R6X	Overflow (msb) Bits for LFS Signal Compare	6	3?5	348
R7X	LCD Signal Control for Color TFT LCDs	7	3?5	350
R8X	STN Color LCD Data Format	8	3?5	351
R9X	TFT LCD Data Format	9	3?5	352
RBX	Shade Conversion and Extra Line Clock Insert	B	3?5	357
RCX	LFS Vertical Position for 600-Line Modes	C	3?5	354
RDX	LCD Timing – LFS Vertical Position #6	D	3?5	347
REX	Overflow Bits for RCX and RDX	E	3?5	357
	Horizontal-Timing Shadow Registers			
R0Y	Horizontal Timing Shadow Register	0	3?5	357
R2Y	Horizontal Timing Shadow Register	2	3?5	357
R3Y	Horizontal Timing Shadow Register	3	3?5	357
R4Y	Horizontal Timing Shadow Register	4	3?5	357
R5Y	Horizontal Timing Shadow Register	5	3?5	357
R0Z	Horizontal Timing Shadow Register	0	3?5	357
R2Z	Horizontal Timing Shadow Register	2	3?5	357
R3Z	Horizontal Timing Shadow Register	3	3?5	357
R4Z	Horizontal Timing Shadow Register	4	3?5	357
R5Z	Horizontal Timing Shadow Register	5	3?5	357

NOTES: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.
The RnX register are indexed through settings of CR2D.
The R0Y–R5Y registers and the R0Z–R5Z registers are indexed through settings of CR2C.

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6.2 External / General Registers

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6.2.1 MISC: Miscellaneous Output Register

I/O Port Address: 3C2 (Write) 3CC (Read)

Index: –

Bit	Description	Reset State
7	Vertical Sync Polarity	0
6	Horizontal Sync Polarity	0
5	Page Select	0
4	Reserved	
3	Clock Select [1]	0
2	Clock Select [0]	0
1	Enable Display Memory	0
0	CRTC I/O Address	0

This standard VGA register has an assortment of bits that have nothing in common.

Bit 7 — Vertical Sync Polarity:
When this bit is programmed to:
- 0, Vertical Sync is normally low, and a high indicates beginning sync time.
- 1, Vertical Sync is normally high, and a low indicates beginning sync time.

Bit 6 — Horizontal Sync Polarity:
- When this bit is programmed to:
  - — 0, Horizontal Sync is normally low. A high indicates beginning sync time.
  - — 1, Horizontal Sync is normally high. A low indicates beginning sync time.
- For some monitors, the combined polarity of Vertical and Horizontal Sync is used to indicate the number of scanlines per frame, as shown in the table.
- When Extension Register CR20[5] = 1 and MISC[7:6] = 00, the value of MISC[7:6] is redefined from Reserved to an 800 x 600 LCD.

MISC		Vertical Size	Vertical Overscan	Vertical Total =
[7] Vertical Sync Polarity	[6] Horizontal Sync Polarity	(Scanlines appearing on screen)	(Scanlines appearing off screen)	(Vertical Size + Vertical Overscan)
0 (+)	0 (+)	Reserved	Reserved	Reserved
0 (+)	1 (–)	400	14	414
1 (–)	0 (+)	350	12	362
1 (–)	1 (–)	480	16	496

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6.2.1 MISC: Miscellaneous Output Register *(cont.)*

Bit — **Description**

5 — **Page Select:**
When SR4[2] (the odd/even bit of the Sequencer Memory Mode Register) is 1, MISC[5] affects how display memory addresses are selected.
- When SR4[2] = 1, and this bit = 0, only odd memory locations are selected.
- When SR4[2] = 1, and this bit = 1, only even memory locations are selected.
- This bit takes effect for video modes 6, D, E, 11, and 12.
- This bit is ignored if either of the following are true:
  - — Graphics Controller Register GR6[1] = 1.
  - — Sequencer Register SR4[3] = 1.

4 — **Reserved**

3:2 — **Clock Select:**
As shown in the following table, this field is used with Sequencer Register bits and Extension Register bits to choose a clock source for the CL-GD7542.

SR22 [3]	SR23 [7]	MISC [3]	MISC [2]	SR1F [6]	SR1E [0]	Clock Source to CL-GD7542
0	0	0	0	0	X	SR0B (N) / SR1B (D) [a]
0[b]	X	X	X	0	X	OSC if TV-Out Enabled
X	X	X	X	1	0	MCLK
X	X	X	X	1	1	MCLK ÷ 2 [c]
0	0	0	1	0	X	SR0C (N) / SR1C (D) [a]
0	0	1	0	0	X	SR0D (N) / SR1D (D) [a]
0	0	1	1	0	X	SR0E (N) / SR1E (D) [a]
0	1	0	X	0	X	FCVCLK to only DAC
0	1	1	X	0	X	FCVCLK to both DAC and CRTC
1	1	0	X	0	X	OSC (Pin)

[a] These are Numerator/Denominator Registers. For information on programming alternative frequencies, refer to Appendix A7.
[b] True only if CR30[3] =1 and SR25[4] = 1.
[c] True only if SR12[4] = 1.

1 — **Enable Display Memory:**
When this bit is programmed to:
- 0, the CL-GD7542 will not respond to any accesses to display memory.
- 1, the CL-GD7542 will respond normally to accesses to display memory.

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6.2.1 MISC: Miscellaneous Output Register *(cont.)*

Bit	Description
0	**CRTC I/O Address:** This bit selects either Monochrome or Color I/O addresses.

MISC[0]	Mode	Input Status / Feature Control	CRTC Index	CRTC Data
0	Monochrome	3BA	3B4	3B5
1	Color	3DA	3D4	3D5

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6.2.2 FC: Feature Control Register

I/O Port Address: 3?A (Write) 3CA (Read)

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	CRT VSYNC Control	0
2	Reserved	
1	Reserved	
0	Reserved	

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of the original IBM PC registers. Nearly all the bits are no longer used.

Bit	Description
7:4	Reserved
3	**CRT VSYNC Control:** This bit is normally used for CRTs that have a internal vertical display enable signal pin. Program this bit: • to 0 to keep the CRT VSYNC signal unchanged and to maintain IBM compatibility. • to 1 to logically OR the CRT VSYNC signal with the CL-GD7542 internal vertical display enable signal prior to going to the VSYNC pin.
2.0	Reserved

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6.2.3 FEAT: Input Status Register 0

I/O Port Address: 3C2

Index: –

Bit	Description	Reset State
7	Vertical Interrupt Request Pending	0
6	Reserved	
5	Reserved	
4	DAC Switch Sensing	0
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

The bits in this read-only register are nearly all undefined.

Bit	Description
7	**Vertical Interrupt Request Pending:** When this bit: • = 1, there is a vertical interrupt request pending. • = 0, there is no vertical interrupt request pending. For more information on the CL-GD7542 vertical interrupt system, refer to CRT Controller Register CR11.
5	Reserved
4	**DAC Switch Sensing:** This read-only bit is used to report the on-off status of one of four analog comparator RAMDAC sense switches, as selected by MISC[3:2]. This bit: • = 1 when the selected DAC sense switch is on. • = 0 when the selected DAC sense switch is off.
3:0	Reserved

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6.2.4 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: –

Bit	Description	Reset State
7	Peserved	
6	Reserved	
5	Diagnostic [1]	0
4	Diagnostic [0]	0
3	Vertical Retrace	0
2	Reserved	
1	Reserved	
0	Video Display Enable	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register contains some status bits.

Bit — **Description**

7:6 — Reserved

5:4 — **Diagnostic [1:0]:**
For diagnostic purposes, these bits indicate the state of two of the eight outputs of the Attribute Controller Register AR12[5:4], as indicated in the following table:

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	FP[2] Red	FP[0] Blue
0	1	FP[3] Secondary Blue	FP[1] Green
1	0	FP[5] Secondary Red	FP[4] Secondary Green
1	1	FP[7]	FP[6]

If the Attribute Controller Register AR12[3:2] or Extension Register CR1A[3:2] set the FP[7:0] bits to act as inputs, the STAT[5:4] bits can reflect the input data on FP[7:0]

3 — **Vertical Retrace:**
A 1 on this bit indicates that vertical retrace is in progress.

2 1 — Reserved

0 — **Video Display Enable:**
When this bit:
- = 0, video data bits are being serialized and displayed.
- = 1, vertical or horizontal blanking is active.

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6.2.5 3C3 Sleep Mode Register

I/O Port Address: 3C3

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Sleep Mode Readback	1
0	Sleep Mode Write / Readback	1

The CL-GD7542 may be put into the sleep mode in one of several ways.

1. Sleep Mode Method 1:
   This 3C3 Sleep Mode Register is normally recommended for motherboard applications.
2. Sleep Mode Method 2:
   When the S46 / MD[21] pin has an external pull-up resistor attached, the alternate Sleep Mode Register, 46E8, is selected. (The 3C3 Sleep Mode Register is then inactive.)
3. Sleep Mode Method 3:
   The sleep mode may also be activated when the SLEEP# input pin is low.

Bit	Description
7:2	Reserved
1	**Sleep Mode Readback:** This bit is read-only. When 3C3[0]: • = 1, this bit is also 1. • = 0, this bit is also 0.
0	**Sleep Mode Write / Readback:** This read/write bit is normally 1. When this bit: • = 1, the CL-GD7542 is active and can respond to normal bus and display activity. • = 0, the CL-GD7542 turns off the interface to the display memory, the interface to the CPU I/O, and the displays. • is cleared to 0, no other chip accesses, except those to 3C3, are allowed until this bit is set to a 1.

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6.2.6 3C6 Pixel Mask Register

I/O Port Address: 3C6

Index: –

Bit	Description	Reset State
7	Pixel Mask Register Bit [7]	0
6	Pixel Mask Register Bit [6]	0
5	Pixel Mask Register Bit [5]	0
4	Pixel Mask Register Bit [4]	0
3	Pixel Mask Register Bit [3]	0
2	Pixel Mask Register Bit [2]	0
1	Pixel Mask Register Bit [1]	0
0	Pixel Mask Register Bit [0]	0

The bits in this read-only register form the Pixel Mask for the Palette DAC. Typically, the Cirrus Logic BIOS programs all these bits to 1. This same 3C6 address is used to access the Hidden DAC Register, described in this manual's Extension Registers (Section 6.7).

Bit	Description
7:0	**Pixel Mask [7:0]:** This field is the Pixel Mask for the Palette DAC. When a bit in this field is programmed to 0, the corresponding bit in the pixel data is ignored in looking up an entry in the Color Lookup Table.

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6.2.7 3C7: Pixel Address Read Mode Register (Write Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Reset State
7	Pixel Address Bit (Read Mode) [7]	0
6	Pixel Address Bit (Read Mode) [6]	0
5	Pixel Address Bit (Read Mode) [5]	0
4	Pixel Address Bit (Read Mode) [4]	0
3	Pixel Address Bit (Read Mode) [3]	0
2	Pixel Address Bit (Read Mode) [2]	0
1	Pixel Address Bit (Read Mode) [1]	0
0	Pixel Address Bit (Read Mode) [0]	0

The bits in this write-only register form the Pixel Address (Read Mode) for the Palette DAC. This Pixel Address is then used to specify the Color Lookup Table entry that is to be read.

Bit	Description
7:0	**Pixel Address (Read Mode) [7:0]:** This field is the Pixel Address (Read Mode) for an entry in the Color Lookup Table. At the conclusion of every third read of the Pixel Data Register (3C9), this address is incremented by one.

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6.2.8 3C7: DAC State Register (Read Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	DAC State [1]	0
0	DAC State [0]	0

The bits in this read-only register indicate whether a read or a write to the Color Lookup Table occurred last.

Bit	Description
7:2	Reserved
1:0	**DAC State [1:0]:** This two-bit field indicates which pixel address register was accessed last. • Both bits in this field will always be the same digit. • When the bits: — are 00, a write operation is in progress, meaning that the last accessed register for the Color Lookup Table was the Pixel Address Write Register. — are 11, a read operation is in progress, meaning that the last accessed register for the Color Lookup Table was the Pixel Address Read Register.

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6.2.9 3C8: Pixel Address Write Mode Register

I/O Port Address: 3C8

Index: –

Bit	Description	Reset State
7	Pixel Address Bit (Write Mode) [7]	0
6	Pixel Address Bit (Write Mode) [6]	0
5	Pixel Address Bit (Write Mode) [5]	0
4	Pixel Address Bit (Write Mode) [4]	0
3	Pixel Address Bit (Write Mode) [3]	0
2	Pixel Address Bit (Write Mode) [2]	0
1	Pixel Address Bit (Write Mode) [1]	0
0	Pixel Address Bit (Write Mode) [0]	0

The bits in this registers form the Pixel Address (Write Mode) for the Palette DAC. This Pixel Address is then used to specify the Color Lookup Table entry that is to be written.

Bit	Description
7:0	**Pixel Address (Write Mode) [7:0]:** This field is the Pixel Address (Write Mode) for an entry in the Color Lookup Table. At the conclusion of every third write to the Pixel Data Register (3C9), this address is incremented by one.

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6.2.10 3C9: Pixel Data Register

I/O Port Address: 3C9

Index: –

Bit	Description	Reset State
7	Pixel Data Register Bit [7]	0
6	Pixel Data Register Bit [6]	0
5	Pixel Data Register Bit [5]	0
4	Pixel Data Register Bit [4]	0
3	Pixel Data Register Bit [3]	0
2	Pixel Data Register Bit [2]	0
1	Pixel Data Register Bit [1]	0
0	Pixel Data Register Bit [0]	0

This register contains the Pixel Data for the palette DAC.

Bit	Description
7:0	**Pixel Data [7:0]:** These read/write register bits store the Pixel Data for the Palette DAC. Writing to this register. • Prior to writing to this register, register 3C8 (the Pixel Address Write Mode Register) is written with the first or only pixel address. • Three values, corresponding to the Red, Green, and Blue values for the pixel, are then written to this address. • Following the third write, values are transferred to the Color Lookup Table. • The Pixel Address is incremented, in case new values for the next pixel address are to be written. Reading from this register. • Prior to reading from this register, register 3C7 (the Pixel Address Read Mode Register) is written with the first or only pixel address. • Three values, corresponding to the Red, Green, and Blue values for the pixel, are then read from this address. • Following the third read, the Pixel Address is incremented, in case new values for the next pixel address are to be read.

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6.2.11 PCI00: PCI Device ID / PCI Vendor ID Register

PCI Configuration Address: 00 Index: –

Bit	Description	Reset State
31	PCI Device ID [15]	0
30	PCI Device ID [14]	0
29	PCI Device ID [13]	0
28	PCI Device ID [12]	1
27	PCI Device ID [11]	0
26	PCI Device ID [10]	0
25	PCI Device ID [9]	1
24	PCI Device ID [8]	0
23	PCI Device ID [7]	0
22	PCI Device ID [6]	0
21	PCI Device ID [5]	0
20	PCI Device ID [4]	0
19	PCI Device ID [3]	0
18	PCI Device ID [2]	0
17	PCI Device ID [1]	0
16	PCI Device ID [0]	0
15	PCI Vendor ID [15]	0
14	PCI Vendor ID [14]	0
13	PCI Vendor ID [13]	0
12	PCI Vendor ID [12]	1
11	PCI Vendor ID [11]	0
10	PCI Vendor ID [10]	0
9	PCI Vendor ID [9]	0
8	PCI Vendor ID [8]	0
7	PCI Vendor ID [7]	0
6	PCI Vendor ID [6]	0
5	PCI Vendor ID [5]	0
4	PCI Vendor ID [4]	1
3	PCI Vendor ID [3]	0
2	PCI Vendor ID [2]	0
1	PCI Vendor ID [1]	1
0	PCI Vendor ID [0]	1

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This register is accessible and effective only if the CL-GD7542 is configured for PCI bus. It contains the PCI Device ID and the PCI Vendor ID required for PCI compliance.

Bit	Description
31.16	**PCI Device ID [15:0]:** When the CL-GD7542 is configured for PCI bus, this read-only field returns 1200 hex, the PCI device ID assigned to the CL-GD7542 by Cirrus Logic, Inc.
15.0	**PCI Vendor ID [15:0]:** When the CL-GD7542 is configured for PCI bus, this read-only field returns 1013 hex, the PCI vendor ID assigned to Cirrus Logic, Inc. by the PCI Special Interest Group.

6.2.12 PCI04: PCI Command Register

PCI Configuration Address: 04 Index: –

Bit	Description	Reset State
15	Reserved	
14	Reserved	
13	Reserved	
12	Reserved	
11	Reserved	
10	Reserved	
9	Reserved	
8	Reserved	
7	Reserved	
6	Reserved	
5	Enable PCI DAC Shadowing	0
4	Reserved	
3	Reserved	
2	Reserved	
1	Enable Memory Accesses	0
0	Enable I/O Accesses	0

This 16-bit register is accessible and effective only if the CL-GD7542 is configured for PCI Bus. It consists of the least-significant two bytes of the PCI Status / PCI Command Register.

Bit	Description
15:6	Reserved: These bits are reserved and must be programmed to a 0.
5	**Enable PCI DAC Shadowing:** When the CL-GD7542 is configured for PCI Bus and this bit is programmed to a 1: • PCI DAC shadowing is enabled. • Read accesses are executed normally. • Write accesses to the CL-GD7542 are executed, in that data bits are latched in the appropriate Palette Register. However, the CL-GD7542 will not acknowledge the access.
4.2	Reserved: These bits are reserved and must be programmed to a 0.
1	**Enable Memory Accesses:** When the CL-GD7542 is configured for PCI Bus and this bit is programmed to: • 1, memory accesses are enabled on the CL-GD7542. • 0, memory accesses are not enabled on the CL-GD7542.
0	**Enable I/O Accesses:** When the CL-GD7542 is configured for PCI Bus and this bit is programmed to: • 1, I/O accesses are enabled on the CL-GD7542. • 0, I/O accesses are not enabled on the CL-GD7542. Regardless of state of this bit, I/O accesses to PCI configuration registers (PC100, PC104, PC110, and PC13C) are always enabled.

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6.2.13 PCI04: PCI Status Register

PCI Configuration Address: 04

Index: –

Bit	Description	Reset State
31	Reserved	
30	Reserved	
29	Reserved	
28	Reserved	
27	Reserved	
26	DEVSEL# Timing [1]	0
25	DEVSEL# Timing [0]	0
24	Reserved	
23	Reserved	
22	Reserved	
21	Reserved	
20	Reserved	
19	Reserved	
18	Reserved	
17	Reserved	
16	Reserved	

This 16-bit register, which is accessible and effective only if the CL-GD7542 is configured for PCI Bus, consists of the most-significant two bytes of the PCI Status / PCI Command Register.

Bit	Description
31.27	Reserved
26.25	**DEVSEL# Timing [1:0]:** When the CL-GD7542 is configured for PCI bus, this read-only field always returns the value 00 to indicate fast DEVSEL# timing.
24 16	Reserved

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6.2.14 PCI10: PCI Base Address Register

PCI Configuration Address: 10 Hex

Index: –

Bit	Description	Reset State
31	PCI Base Address for Display Memory [31]	0
30	PCI Base Address for Display Memory [30]	0
29	PCI Base Address for Display Memory [29]	0
28	PCI Base Address for Display Memory [28]	0
27	PCI Base Address for Display Memory [27]	0
26	PCI Base Address for Display Memory [26]	0
25	PCI Base Address for Display Memory [25]	0
24	PCI Base Address for Display Memory [24]	0
23:1	Reserved	
0	Memory / I/O Indicator	0

This 32-bit register, which is accessible and effective only when the CL-GD7542 is configured for PCI bus, contains the PCI Base Address for display memory.

Bit	Description
31:24	**PCI Base Address for Display Memory [31:24]:** When the CL-GD7542 is configured for PCI bus, this field contains the base address of the contiguous 16-Mbyte display memory block reserved for the CL-GD7542.
23:1	Reserved
0	**Memory / I/O Indicator:** When the CL-GD7542 is configured for PCI bus, this bit is used to indicate the type of address space requested, either memory or I/O. • When this bit: — is 0, a memory address space is requested. — is 1, an I/O address space is requested. • For the PCI BIOS, this bit is read/write. • For the VGA BIOS, this bit is read only.

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6.2.15 PCI3C: PCI Interrupt Pin and PCI Interrupt Line Register

PCI Configuration Address: 3C Hex

Index: –

Bit	Description	Reset State
15	PCI Interrupt Pin [7]	0
14	PCI Interrupt Pin [6]	0
13	PCI Interrupt Pin [5]	0
12	PCI Interrupt Pin [4]	0
11	PCI Interrupt Pin [3]	0
10	PCI Interrupt Pin [2]	0
9	PCI Interrupt Pin [1]	0
8	PCI Interrupt Pin [0]	1
7	PCI Interrupt Line [7]	0
6	PCI Interrupt Line [6]	0
5	PCI Interrupt Line [5]	0
4	PCI Interrupt Line [4]	0
3	PCI Interrupt Line [3]	0
2	PCI Interrupt Line [2]	0
1	PCI Interrupt Line [1]	0
0	PCI Interrupt Line [0]	0

This register, which is accessible and effective only when the CL-GD7542 is configured for PCI bus, contains data from the PCI Interrupt Pin and PCI Interrupt Line.

Bit	Description
15:8	**PCI Interrupt Pin [7:0]:** When the CL-GD7542 is configured for PCI bus, this read-only field contains the value 01 hex. This value indicates the CL-GD7542 INTR# interrupt request pin is connected to the PCI Bus INTA# interrupt request pin.
7:0	**PCI Interrupt Line [7:0]:** When the CL-GD7542 is configured for PCI bus, this read/write field contains an 8-bit value that has no direct effect on the CL-GD7542. This field is used to transfer an interrupt pointer from the PCI system BIOS to the CL-GD7542 VGA BIOS.

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6.2.16 46E8 Alternate Sleep Mode Register

I/O Port Address: 46E8

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Alternate Sleep Mode Select	1
2	Reserved	
1	Reserved	
0	Reserved	

This register is active only when the following two conditions are both filled:

1. There is a low-to-high transition of the Reset# signal.
2. There is an external pull-up resistor on the S46 / MD[21] pin, which disables the 3C3 Sleep Mode Register.

Unless both conditions are filled, register 3C3 is the sleep mode register.

Bit	Description
7:4	Reserved
3	**Alternate Sleep Mode Select:** When there is a pull-up resistor on the CL-GD7542 pin S46 / MD[21], and when this bit: • is 1, the CL-GD7542: — is enabled. — can respond to normal bus and video display activity. • is 0, the CL-GD7542: — is disabled and will not affect the video display activity. — will respond normally to BIOS access. — will not respond to accesses to I/O, except to those addressed to 46E8. — will not respond to any accesses to display memory.
2 0	Reserved

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6.3 Sequencer Registers

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6.3.1 SRX: Sequencer Index Register

I/O Port Address: 3C4

Index: –

Bit	Description	Reset State
7	Fine Position HW Cursor and HW Icon [2]	0
6	Fine Position HW Cursor and HW Icon [1]	0
5	Fine Position HW Cursor and HW Icon [0] / Sequencer Index [5]	0
4	Sequencer Index [4]	0
3	Sequencer Index [3]	0
2	Sequencer Index [2]	0
1	Sequencer Index [1]	0
0	Sequencer Index [0]	0

Depending on this register's index value, this register has one of two possible purposes:

1 The primary purpose is to extend the sequencer index from 3 bits to 6 bits. The index specifies which register in the CL-GD7542 sequencer block is to be accessed by the next I/O read or write to Address 3C5. An index number greater than 5 points to registers that are defined in this manual's Extension Registers in section 6.7.

2. The secondary purpose is to specify the fine position of the hardware cursor and the hardware icon, both horizontal and vertical.

Bit	Description
7:5	**Fine Positions for Hardware Cursor and Hardware Icon:** **Vertical Fine Position for Hardware Cursor and Hardware Icon [2:0]:** When Extension Register SR11 is programmed, bits SRX[7:5] define in scan-lines the vertical fine position of the hardware cursor and icon. **Horizontal Fine Position for Hardware Cursor and Hardware Icon [2:0]:** When Extension Register SR10 is programmed, bits SRX[7:5] define in dot clocks (pixels) the horizontal fine position of the hardware cursor and icon. For special modes requiring extra dot clocks for fine position adjustments, a fourth, most-significant bit has been added to Attribute Controller Registers SR2E and SR2A. • Hardware Cursor Bit: Extension Register SR2E[0] — For the horizontal fine position of the hardware cursor, SR2E[0] is an added fourth and most-significant bit. — This bit is used in horizontally expanded graphics modes. • Hardware Icon Bit: Extension Register SR2A[6] — For the horizontal fine position of the hardware icon, SR2A[6] is an added fourth and most-significant bit. — This bit is used in horizontally expanded graphics modes and for text modes with 9-dot and 10-dot fonts, such as 640 x 480 displays that are expanded to 800 x 600.

Continued on next page.

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6.3.1 SRX: Sequencer Index Register *(cont.)*

Bit	Description
5:0	**Sequencer Index [5:0]:** • When writing to any CL-GD7542 sequencer index *except* 10h or 11h: — These bits become a 6-bit sequencer index field, SRX[5:0]. — The SRX[5:0] field selects the register to be accessed with the next I/O read or I/O write to I/O Port Address 3C5. • When writing *to* CL-GD7542 sequencer index 10h or 11h: — These bits become a 5-bit sequencer index field, SRX[4:0]. — The SRX[4:0] field selects the sequencer index, SRX[7:5], used to define the fine position for the hardware cursor and hardware icon. — Extension registers SR2A[6] and SR2E[0]) also define the fine position for the hardware cursor and hardware icon.

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6.3.2 SR0: Reset Register

I/O Port Address: 3C5

Index: 0

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Synchronous Reset	1
0	Asynchronous Reset	1

This register is used to reset the CL-GD7542 sequencer. These bits are for VGA-standard compatibility only, and after reset they need never be used.

Bit	Description
7:2	Reserved
1	**Synchronous Reset:** When this bit is programmed to: • 0, the sequencer is cleared and halted, which disables screen refresh and display memory refresh. • 1, and when SR0[0] = 1, the sequencer will operate normally.
0	**Asynchronous Reset:** When this bit is programmed to: • 0, the sequencer is cleared and halted, and SR3 is cleared. • 1, and when SR0[1] = 1, the sequencer will operate normally.

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6.3.3 SR1: Clocking Mode Register

I/O Port Address: 3C5

Index: 1

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Full Display Memory Bandwidth	0
4	Shift and Load 32 Data Bits	0
3	Dot Clock	0
2	Shift and Load 16 Data Bits	0
1	Reserved	
0	8/9 Dot Clock	0

This register is used to control some miscellaneous functions in the CL-GD7542 sequencer.

Bit	Description
7:6	Reserved
5	**Full Display Memory Bandwidth:** When this bit is programmed to: • 0, the CRT screen is turned on, and the CL-GD7542 operates normally. • 1, the CRT screen is turned off. In addition: — The CPU uses nearly 100% of the display memory bandwidth. — HSYNC and VSYNC continue normally. — The BLANK# signal goes active and stays active. — The refresh for the display memory will continue normally.
4	**Shift and Load 32 Data Bits:** This bit, in conjunction with SR1[2], controls how often 32-bit graphics controller display data shifters are loaded, according to the following table:

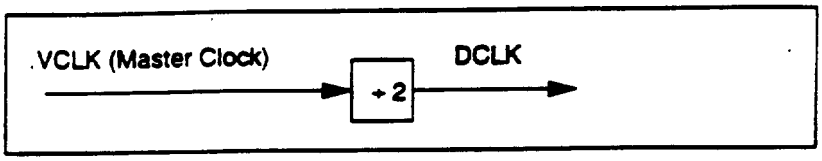
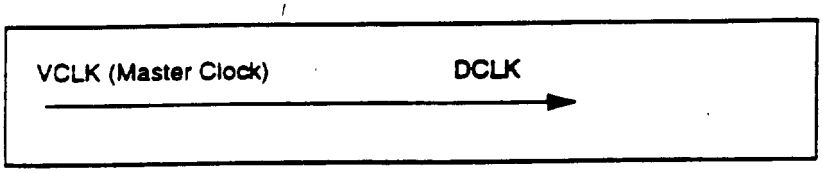
SR1		Data Shifters Loaded
[4]	[2]	
0	0	Every character clock
0	1	Every 2nd character clock
1	x	Every 4th character clock

Continued on next page.

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6.3.3 SR1: Clocking Mode Register *(cont.)*

Bit	Description
3	**Dot Clock:** When this bit is programmed to: • 1, VCLK (the Master Clock) is divided by 2 to generate DCLK, a dot clock that is half the frequency of the Master Clock. This dot clock is used for low-resolution video modes such as 0, 1, 4, 5, and D.  • 0, VCLK (the Master Clock) is not divided by 2. In this case, the clock that is used as the dot clock is the same frequency as the Master Clock. 
2	**Shift and Load 16 Data Bits:** This bit controls how often 16-bit graphics controller display data shifters are loaded. (Refer to the description of bit [4] of this register.)
1	Reserved
0	**8/9 Dot Clock:** When this bit is programmed to: • 0, then character clocks 8 dots wide are generated, used in all modes by mode 7, in which there are 320 or 640 horizontal dots. • 1, then character clocks 9 dots wide are generated, used in the mono-chrome mode 7, in which there are 720 horizontal dots.

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6.3.4 SR2: Plane Mask Register

I/O Port Address: 3C5

Index: 2

Bit	Description	Reset State
7	Enable Writing Pixel 7 / Reserved	0
6	Enable Writing Pixel 6 / Reserved	0
5	Enable Writing Pixel 5 / Reserved	0
4	Enable Writing Pixel 4 / Reserved	0
3	Enable Writing Pixel 3 / Bit-Map Plane 3 Enable	0
2	Enable Writing Pixel 2 / Bit-Map Plane 2 Enable	0
1	Enable Writing Pixel 1 / Bit-Map Plane 1 Enable	0
0	Enable Writing Pixel 0 / Bit-Map Plane 0 Enable	0

This register has two uses.

1. Its first use is to control the writing of up to eight pixels.
2. Its second use is to enable or disable writing to the four bit-map planes of display memory.

Bit	Description
7:0	**Enable Writing Pixel [7:0]:** • These bits can control whether individual pixel data bits [7:0] are written. • To enable an individual pixel, the corresponding Enable Writing Pixel bit must be set to 1, and *one* of the following conditions must be met: — Extended Write Mode 4 or Extended Write Mode 5 is selected with Graphics Controller Register bits GR5[2:0]. — Write Mode 1 is selected with Graphics Controller Register bits GR5[2:0], and Extension Register GRB[2] is set to 1. • This field is also used as a write protect for the BitBLT (bit block transfer) engine.
7 4	**Reserved:** These four bits are reserved when Extended Write Modes 4 and 5 are disabled (that is, Graphics Controller Register bits GR5[2] = 0), which would be the case for VGA-compatibility modes.
3 0	**Bit-Map Plane Enable [3:0]:** These four bits are used to control whether individual display memory bit-map planes [3:0] are written with Write Modes [3:0].

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6.3.5 SR3: Character Map Set Select Register

I/O Port Address: 3C5

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Character Map Set Select [0]	0
4	Primary Character Map Set Select [0]	0
3	Secondary Character Map Set Select [2]	0
2	Secondary Character Map Set Select [1]	0
1	Primary Character Map Set Select [2]	0
0	Primary Character Map Set Select [1]	0

This register is used to specify the primary and the secondary character map sets (fonts). This register applies only to text modes.

Bit	Description
7:6	Reserved
5, 3:2	**Secondary Character Map Set Select:** These three bits select from among the secondary character map sets, according to the following table:

SR3			Secondary Character Map Set	Address Offset (Kbytes)
[5]	[3]	[2]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

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6.3.5 SR3: Character Map Set Select Register *(cont.)*

Bit **Description**

4, 1:0 **Primary Character Map Set Select:**
These three bits select from among the primary character map sets, according to the following table:

SR3			Primary Character Map Set	Address Offset (Kbytes)
[4]	[1]	[0]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

NOTES:

(1) In text video display modes:
1. Character Map Plane 0 stores the ASCII text character code.
2. Character Map Plane 1 stores the attribute byte.
3. Character Map Plane 2 stores the character map set (the font).

(2) Bit 3 of the attribute byte normally controls the intensity of the foreground color.

This bit may be redefined to be a switch between character sets, allowing 512 displayable characters.

This switch is enabled whenever SR4[1] is a 1 *AND* there is a difference between the values of the Primary Character Map Set Select and the values of the Secondary Character Map Set Select.

(3) The format for the Character Map Plane 2 font address bits [15:0] is:
F2 F1 F0 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0
where:
F[2:0] is the character map set select
C[7:0] is the ASCII text character code
R[4:0] is the character row (the scanline in the character cell)

6.3.6 SR4: Memory Mode Register

I/O Port Address: 3C5

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Chain-4	0
2	Odd/Even Mode	0
1	Extended Memory	0
0	Reserved	

This register is used to control some miscellaneous functions in the CL-GD7542 sequencer.

Bit	Description
7:4	Reserved
3	**Chain-4:** When this bit is programmed to 1: • This bit takes priority over SR4[2] (Odd/Even Mode) and Graphics Controller Register GR5[4] (Odd/Even Addressing Mode). • Its effect is similar to SR4[2] (Odd/Even Mode), except both A0 and A1 are used. — Address A0 provides display memory Plane Select Bit [0]. — Address A1 provides display memory Plane Select Bit [1]. • The Graphics Controller Read Map Register (GR4) is ignored.
2	**Odd/Even Mode:** • When this bit is programmed to 0, the sequencer is in Odd/Even Mode. • This bit *must* be programmed to a 0 for text modes. • The value of this bit must track Graphics Controller Register GR5[4] (Odd/Even Addressing Mode), and the values must be opposite. — The even CPU addresses will access display memory planes 0 and 2. — The odd CPU addresses will access display memory planes 1 and 3. • This bit may be overridden by the SR4[3] bit.
1	**Extended Memory:** When this bit is programmed to: • 0, effective memory size is 64K, regardless of actual installed memory. (EGA modes require this to be the case.) • 1, effective memory size equals actual installed memory.
0	Reserved

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6.4 CRT Controller Registers

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6.4.1 CRX: CRT Controller Index Register

I/O Port Address: 3?4

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	CRTC Index [5]	0
4	CRTC Index [4]	0
3	CRTC Index [3]	0
2	CRTC Index [2]	0
1	CRTC Index [1]	0
0	CRTC Index [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This index register is used to specify the register in the CRT Controller block to be accessed by the next I/O read or I/O write to Address 3?5. Registers at indices 19, 1A, 1B, 25, and 27 are described in this manual's section on the CL-GD7542 Extension Registers, in section 6.7.

Bit	Description
7:6	Reserved
5:0	**CRTC Index [5:0]:** The value resulting from these bits point to the register to be accessed in the next I/O read or I/O write to address 3?5. (Note that registers above 18 were never documented by IBM.)

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6.4.2 CR0: Horizontal Total Register

I/O Port Address: 3?5

Index: 0

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to specify the total number of character clocks per horizontal period.

Bit	Description
7:0	**Horizontal Total:** This 8-bit field specifies the total number of character clocks per horizontal period as follows: • The VCLK signal provides the character clock. (The character clock is derived from VCLK, according to the character width.) • The character counter counts the total number of character clocks. • The value in the character counter is then compared with the value in this register to provide the basic horizontal timing. • All horizontal and vertical timing is eventually derived from the basic horizontal timing in this register. The value of the horizontal total for this register may be calculated as follows: FROM: Total number of character clocks (from character counter) SUBTRACT: − 5 character clocks (for standard VGA compatibility) TO GET: = Horizontal total Example: If 80 characters are desired per horizontal scanline, then a value of 75 must be loaded into this register. Figure 6–1 indicates the way the horizontal and vertical timing is defined. • The horizontal timing is calculated in terms of character clock periods. • The vertical timing is calculated in terms of horizontal periods. Table 6–1 indicates how the various CRT Controller timing registers are extended.

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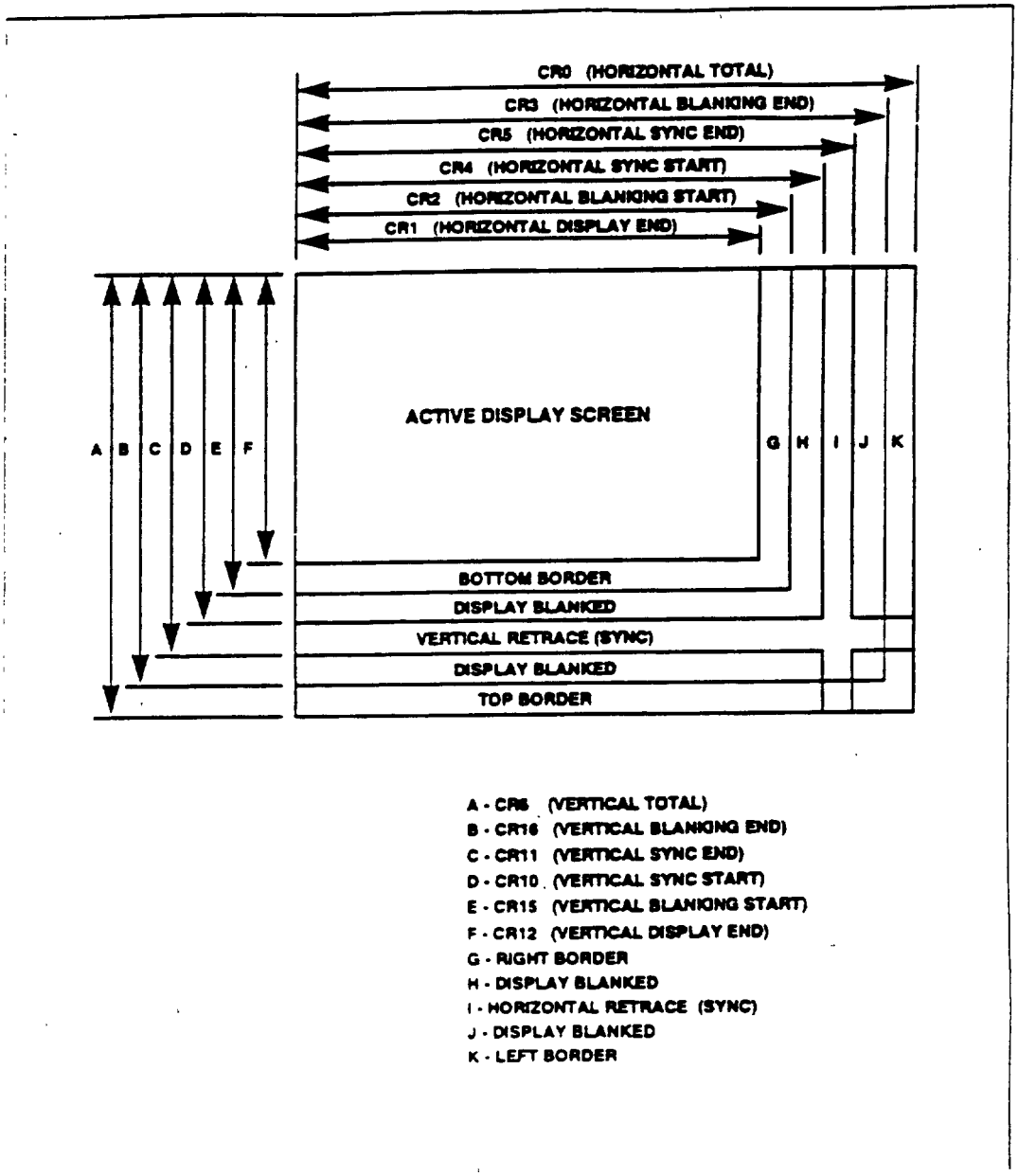


Figure 6–1. CRTC Timing Registers

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The following table is a guide to the location of the CRT controller timing registers and accompanying extension and overflow bits.

- An extension bit is a bit added by Cirrus Logic to the standard VGA controller bits.
- An overflow bit is a standard VGA controller bit that results from using more than eight bits to define a field.

Table 6–1. Summary of CRT Controller Timing Register Bits[a]

Parameter	CRT Controller Register Bit Position					
	[9]	[8]	[7]	[6]	[5]	[4:0]
H Total			**CR0[7]**	**CR0[6]**	**CR0[5]**	**CR0[4:0]**
H Display End			**CR1[7]**	**CR1[6]**	**CR1[5]**	**CR1[4:0]**
H Blanking Start			**CR2[7]**	**CR2[6]**	**CR2[5]**	**CR2[4:0]**
H Blanking End			**CR1A[5]**	**CR1A[4]**	**CR5[7]**	**CR3[4:0]**
H Sync Start			**CR4[7]**	**CR4[6]**	**CR4[5]**	**CR4[4:0]**
H Sync End						**CR5[4:0]**
V Total	**CR7[5]**	**CR7[0]**	**CR6[7]**	**CR6[6]**	**CR6[5]**	**CR6[4:0]**
V Sync Start	**CR7[7]**	**CR7[2]**	**CR10[7]**	**CR10[6]**	**CR10[5]**	**CR10[4:0]**
V Sync End						**CR11[3:0]**
V Display End	**CR7[6]**	**CR7[1]**	**CR12[7]**	**CR12[6]**	**CR12[5]**	**CR12[4:0]**
V Blanking Start	**CR9[5]**	**CR7[3]**	**CR15[7]**	**CR15[6]**	**CR15[5]**	**CR15[4:0]**
V Blanking End	**CR1A[7]**	**CR1A[6]**	**CR16[7]**	**CR16[6]**	**CR16[5]**	**CR16[4:0]**
Line Compare	**CR9[6]**	**CR7[4]**	**CR18[7]**	**CR18[6]**	**CR18[5]**	**CR18[4:0]**
Offset		**CR1B[4]**	**CR13[7]**	**CR13[6]**	**CR13[5]**	**CR13[4:0]**

a Bits shown in **bold text** are extensions.

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6.4.3 CR1: Horizontal Display End Register

I/O Port Address: 3?5

Index: 1

Bit	Description	Reset State
7	Horizontal Display End [7]	0
6	Horizontal Display End [6]	0
5	Horizontal Display End [5]	0
4	Horizontal Display End [4]	0
3	Horizontal Display End [3]	0
2	Horizontal Display End [2]	0
1	Horizontal Display End [1]	0
0	Horizontal Display End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to specify the number of character clocks during horizontal display time.

Bit	Description
7:0	**Horizontal Display End [7:0]:** For the horizontal display time, this register specifies the number of character clocks, *minus 1*, as calculated for both text modes and graphics modes. • For text modes: CR1[7:0] = "Number of character clocks" – 1 Where number of character clocks = Number of characters • For graphics modes: CR1[7:0] = "Number of character clocks" – 1 Where number of character clocks = (Number of pixels/scanline) ÷ (Number of pixels/character clock) For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.4 CR2: Horizontal Blanking Start Register

I/O Port Address: 3?5

Index: 2

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to specify the character count where horizontal blanking starts.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** This register specifies the character count at which horizontal blanking starts. • For text modes: Character count at which horizontal blanking starts = Number of characters • For graphics modes: Character count at which horizontal blanking starts = (Number of pixels/scanline) ÷ (Number of pixels/character clock) • For both text modes and graphics modes: The value programmed into CR2 must always be larger than the value programmed into CRT Controller Register CR1. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.5 CR3: Horizontal Blanking End Register

I/O Port Address: 3?5

Index: 3

Bit	Description	Reset State
7	Compatible Read	0
6	Display Enable Delay [1]	0
5	Display Enable Delay [0]	0
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to determine the horizontal blanking period width. Also, this register controls access to CRT Controller Registers CR10 and CR11 and the display enable delay.

Bit	Description
7	**Compatible Read:** When this bit: • = 0, CRT Controller Registers CR10 and CR11 are write-only registers. • = 1, CRT Controller Registers CR10 and CR11 are read/write registers.
6.5	**Display Enable Delay [1:0]:** This two-bit field is used to specify the number of character clocks that the display enable signal is delayed from the horizontal total. This delay is necessary to compensate for the accesses of the character code, attribute byte, font, etc. The following table indicates programming for the display enable signal delay:

CR3		Delay for Display Enable Signal (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character clock (typical setting)
1	0	2 character clocks
1	1	3 character clocks

NOTE: If the delay is programmed too low, the left-most character will be repeated. If the delay is programmed too high, one or more characters will disappear at the left of each character row.

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6.4.5 CR3: Horizontal Blanking End Register *(cont.)*

Bit	Description
4:0	**Horizontal Blanking End [4:0]:** The horizontal blanking end field consists of these 5 bits (and as needed, a sixth bit in CR5[7]). This field determines the width of the horizontal blanking period. The least-significant five (or six) bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal blanking period ends. The horizontal blanking end value to be programmed into this register may be calculated as follows: FROM: Horizontal blanking start (value programmed into CR2) SUBTRACT: − Horizontal blanking period (as desired) TO GET: = Horizontal blanking end • The horizontal blanking period: — must never be programmed to extend past the horizontal total. — is limited to 63 character-clock times. • The horizontal blanking end field is extended as follows: — CR5[7] is the horizontal blanking end field bit [5], which extends this field to 6 bits. — When either Extension Register CR1B[5] = 1 or Extension Register CR1B[7] = 1, Extension Register bits CR1A[5:4] further extend the horizontal blanking end field to eight bits with bits [7:6]. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.6 CR4: Horizontal Sync Start Register

I/O Port Address: 3?5

Index: 4

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the time at which horizontal sync becomes active.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** This field specifies the character count at which the horizontal sync signal becomes active. Adjusting the value in this field moves the display horizontally on the screen. • The horizontal sync start must be programmed to a value either equal to or greater than horizontal display end. • The time from horizontal sync start to horizontal total must be either equal to or greater than four character-clock times. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.7 CR5: Horizontal Sync End Register

I/O Port Address: 3?5

Index: 5

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Horizontal Sync Delay [1]	0
5	Horizontal Sync Delay [0]	0
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the position at which the horizontal sync pulse ends, effectively specifying the width of the pulse. In addition, this register contains an overflow bit and a field for the horizontal sync delay.

Bit	Description
7	**Horizontal Blanking End [5]:** This overflow bit increases by one bit the horizontal blanking end value of CR3[4:0].
6:5	**Horizontal Sync Delay [1:0]:** This two-bit field is used to specify the number of character clocks that the external horizontal sync pulse is delayed from the horizontal sync start position implied in CR4. In some video modes, this horizontal sync delay is necessary to allow internal timing signals that are triggered from horizontal sync start to begin, prior to display enable. The following table summarizes programming for the horizontal sync delay:

CR5		Delay for Horizontal Sync Pulse (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character clock
1	0	2 character clocks
1	1	3 character clocks

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6.4.7 CR5: Horizontal Sync End Register *(cont.)*

Bit	Description
4:0	**Horizontal Sync End [4:0]:** This 5-bit field determines the width of the horizontal sync pulse. The least-significant five bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal sync pulse ends. The horizontal sync end value to be programmed into this register may be calculated as follows: FROM: Horizontal sync start (value programmed in CR4) SUBTRACT: − Horizontal sync pulse width (as desired) TO GET: = Horizontal sync end The horizontal sync pulse: • has a width limited to 31 character-clock times. • must never be programmed to extend past the horizontal total of CR0. • must always end during the horizontal blanking period. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.8 CR6: Vertical Total Register

I/O Port Address: 3?5

Index: 6

Bit	Description	Reset State
7	Vertical Total [7]	0
6	Vertical Total [6]	0
5	Vertical Total [5]	0
4	Vertical Total [4]	0
3	Vertical Total [3]	0
2	Vertical Total [2]	0
1	Vertical Total [1]	0
0	Vertical Total [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the total number of scanlines per frame.

Bit	Description
7:0	**Vertical Total [7:0]:** This field is the least-significant eight bits of a ten-bit field that defines the total number of scanlines per frame. This field is extended with CR7[5] and CR7[0]. The value of the Vertical Total field to be programmed may be calculated as follows: FROM: Total number of horizontal scanlines SUBTRACT: − 2 scanlines TO GET: = Vertical Total field (total number of scanlines per frame) When the value in the scanline counter equals the value of the Vertical Total field, a vertical retrace period begins. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.9 CR7: Overflow Register

I/O Port Address: 3?5

Index: 7

Bit	Description	Reset State
7	Vertical Sync Start [9]	0
6	Vertical Display End [9]	0
5	Vertical Total [9]	0
4	Line Compare [8]	0
3	Vertical Blanking Start [8]	0
2	Vertical Sync Start [8]	0
1	Vertical Display End [8]	0
0	Vertical Total [8]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains bits that extend various vertical count fields. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

Bit	Description
7	**Vertical Sync Start [9]:** With CR7[2], this bit extends the vertical sync start field (CR10) to ten bits.
6	**Vertical Display End [9]:** With CR7[1], this bit extends the vertical display end field (CR12) to ten bits.
5	**Vertical Total [9]:** With CR7[0], this bit extends the vertical total field (CR6) to ten bits.
4	**Line Compare [8]:** With CR9[6], this bit extends the line compare field (CR18) to ten bits. This bit can always be written.
3	**Vertical Blanking Start [8]:** With CR9[5], this bit extends the vertical blanking start field (CR15) to ten bits.
2	**Vertical Sync Start [8]:** With CR7[7], this bit extends the vertical sync start field (CR10) to ten bits.
1	**Vertical Display End [8]:** With CR7[6], this bit extends the vertical display end field (CR12) to ten bits.
0	**Vertical Total [8]:** With CR7[5], this bit extends the vertical total field (CR6) to ten bits.

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6.4.10 CR8: Screen A Preset Row Scan Register

I/O Port Address: 3?5

Index: 8

Bit	Description	Reset State
7	Reserved	
6	Byte (Coarse) Panning [1]	0
5	Byte (Coarse) Panning [0]	0
4	Screen A Preset Row Scan [4]	0
3	Screen A Preset Row Scan [3]	0
2	Screen A Preset Row Scan [2]	0
1	Screen A Preset Row Scan [1]	0
0	Screen A Preset Row Scan [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the row scanline at which Screen A starts. This register also allows two types of scrolling:

- scrolling on a character row (scanline) basis (also called coarse panning)
- scanline (row) basis, also called fine scroll.
- In addition, this register specifies byte (coarse) panning.

Bit 7 — Reserved

Bit 6:5 — **Byte (Coarse) Panning [1:0]:**
This two-bit field controls coarse panning. (For fine panning on a pixel-by-pixel basis, refer to Attribute Controller Register AR13.)

- This field can specify a coarse pan of up to 24 pixels, with 8-pixel resolution.
- Values for CR8[6:5] are interpreted as indicated in the following table:

CR8 [6]	CR8 [5]	Resulting Pan (in bytes)	Resulting Pan (in pixels)
0	0	0	0
0	1	1	8
1	0	2	16
1	1	3	24

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Bit 4:0 — **Screen A Preset Row Scan [4:0]:**
This field specifies the scanline at which the first character row will begin.

- This specification provides scrolling on a scanline basis (soft scrolling).
- The contents of this field should be changed only during vertical retrace.

6.4.11 CR9: Character Cell Height Register

I/O Port Address: 3?5

Index: 9

Bit	Description	Reset State
7	Control Scanline Double	0
6	Line Compare [9]	0
5	Vertical Blanking Start [9]	0
4	Character Cell Height [4]	0
3	Character Cell Height [3]	0
2	Character Cell Height [2]	0
1	Character Cell Height [1]	0
0	Character Cell Height [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the number of scanlines in the character cell. In addition, it contains two overflow bits and one control bit.

Bit	Description
7	**Control Scanline Double:** When this bit is 1, every scanline is displayed twice in succession. • Scanlines double for those specifications based on scanline counter addressing, such as Character Height, Cursor Start, Cursor End, and Cursor Underline location. • Typically, this bit is used to double a 200-scanline display to 400 scanlines. • The scanline doubling function is not available in interlaced video modes.
6	**Line Compare [9]:** With CR7[4], this bit extends the line compare field (CR18) to ten bits.
5	**Vertical Blanking Start [9]:** With CR7[3], this bit extends the vertical blanking start field (CR15) to ten bits.
4 0	**Character Cell Height [4:0]:** This field specifies the vertical size of the character cell in terms of scanlines. The value programmed into this field equals the actual size of the character cell (in scanlines), minus 1.

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6.4.12 CRA: Text Cursor Start Register

I/O Port Address: 3?5

Index: A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Disable Text Cursor	0
4	Text Cursor Start [4]	0
3	Text Cursor Start [3]	0
2	Text Cursor Start [2]	0
1	Text Cursor Start [1]	0
0	Text Cursor Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains a bit that will disable the text cursor. In addition, this register specifies the scanline at which the text cursor is to start.

Bit	Description
7:6	Reserved
5	**Disable Text Cursor:** When this bit: • = 1, the text cursor will be disabled (that is, it will be removed). • = 0, the text cursor will function normally.
4:0	**Text Cursor Start [4:0]:** This field specifies the scanline within the character cell at which the text cursor is to start. When the Text Cursor Start value is: • less than the Text Cursor End value, no text cursor will display. • greater than the Text Cursor End value, no text cursor will display. • equal to the Text Cursor End value, the text cursor will display on a single scanline.

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6.4.13 CRB: Text Cursor End Register

I/O Port Address: 3?5

Index: B

Bit	Description	Reset State
7	Reserved	
6	Text Cursor Delay [1]	0
5	Text Cursor Delay [0]	0
4	Text Cursor End [4]	0
3	Text Cursor End [4]	0
2	Text Cursor End [4]	0
1	Text Cursor End [4]	0
0	Text Cursor End [4]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the scanline at which the text cursor is to end. It also contains a field that allows the text cursor display to be delayed from the location specified in CRE and CRF.

Bit	Description
7	Reserved
6:5	**Text Cursor Delay [1:0]:** This two-bit field specifies a delay, given in character clocks, from the text cursor location specified in CRE and CRF to the actual display of the text cursor.
4:0	**Text Cursor End [4:0]:** This field specifies the scanline within the character cell at which the text cursor is to end. When the Text Cursor End value is: • less than or equal to the character cell height, no text cursor will display. • greater than the character cell height, the effective text cursor end value will be equal to the character cell height.

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6.4.14 CRC: Screen A Start Address High Register

I/O Port Address: 3?5

Index: C

Bit	Description	Reset State
7	Screen A Start Address [15]	0
6	Screen A Start Address [14]	0
5	Screen A Start Address [13]	0
4	Screen A Start Address [12]	0
3	Screen A Start Address [11]	0
2	Screen A Start Address [10]	0
1	Screen A Start Address [9]	0
0	Screen A Start Address [8]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, along with CRD and Extension Register CR1B[3:2, 0], specify the display memory location at which data to be displayed on the screen starts.

Bit	Description
7:0	**Screen A Start Address [15:8]:** The 19-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the screen. • Bits [18:16] are in Extension Register CR1B[3:2,0]. • Bits [15:8] are in this register. • Bits [7:0] are in CRT Controller Register CRD.

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6.4.15 CRD: Screen A Start Address Low Register

I/O Port Address: 3?5

Index: D

Bit	Description	Reset State
7	Screen A Start Address [7]	0
6	Screen A Start Address [6]	0
5	Screen A Start Address [5]	0
4	Screen A Start Address [4]	0
3	Screen A Start Address [3]	0
2	Screen A Start Address [2]	0
1	Screen A Start Address [1]	0
0	Screen A Start Address [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, along with CRC and Extension Register CR1B[3:2, 0], specify the display memory location at which data to be displayed on the screen starts.

Bit	Description
7:0	**Screen A Start Address [7:0]:** The 19-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the screen. • Bits [18:16] are in Extension Register CR1B[3:2,0]. • Bits [15:8] are in CRT Controller Register CRC. • Bits [7:0] are in this register.

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6.4.16 CRE: Text Cursor Location High Register

I/O Port Address: 3?5

Index: E

Bit	Description	Reset State
7	Text Cursor Location [15]	0
6	Text Cursor Location [14]	0
5	Text Cursor Location [13]	0
4	Text Cursor Location [12]	0
3	Text Cursor Location [11]	0
2	Text Cursor Location [10]	0
1	Text Cursor Location [9]	0
0	Text Cursor Location [8]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, along with CRF, specifies the display memory location at which the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [15:8]:** The Text Cursor Location is a 16-bit field that specifies the display memory location at which the text cursor is to be displayed. • Bits [15:8] are in this register. • Bits [7:0] are in CRT Controller Register CRF. • The value contained in this field specifies an address in display memory, not an offset from the beginning of the screen. When the value of the Screen A Start is changed without a compensating change in the Text Cursor Location field, the text cursor will move on the screen.

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6.4.17 CRF: Text Cursor Location Low Register

I/O Port Address: 3?5

Index: F

Bit	Description	Reset State
7	Text Cursor Location [7]	0
6	Text Cursor Location [6]	0
5	Text Cursor Location [5]	0
4	Text Cursor Location [4]	0
3	Text Cursor Location [3]	0
2	Text Cursor Location [2]	0
1	Text Cursor Location [1]	0
0	Text Cursor Location [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, with CRE, specifies the display memory location at which the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [7:0]:** The Text Cursor Location is a 16-bit field that specifies the display memory location at which the text cursor is to be displayed. • Bits [15:8] are in CRT Controller Register CRE. • Bits [7:0] are in this register.

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6.4.18 CR10: Vertical Sync Start Register

I/O Port Address: 3?5

Index: 10

Bit	Description	Reset State
7	Vertical Sync Start [7]	0
6	Vertical Sync Start [6]	0
5	Vertical Sync Start [5]	0
4	Vertical Sync Start [4]	0
3	Vertical Sync Start [3]	0
2	Vertical Sync Start [2]	0
1	Vertical Sync Start [1]	0
0	Vertical Sync Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

The Vertical Sync Start field specifies the scanline at which the Vertical Sync pulse is to become active.

Access to this register is controlled by CRT Controller Register CR3[7].

- When CR3[7] = 1, this register is read/write.
- When CR3[7] = 0, this register is write-only.

Bit	Description
7:0	**Vertical Sync Start [7:0]:** The Vertical Sync field specifies the scanline at which the Vertical Sync pulse will become active. • This register contains the least-significant eight bits [7:0] of that field. • Bits [9:8] in CRT Controller Register CR7[7,2] extend this field to ten bits. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

6.4.19 CR11: Vertical Sync End Register

I/O Port Address: 3?5

Index: 11

Bit	Description	Reset State
7	Write Protect CR7 through CR0	0
6	Refresh Cycle Control	0
5	Disable Vertical Interrupt	0
4	Clear Vertical Interrupt	0
3	Vertical Sync End [3]	0
2	Vertical Sync End [2]	0
1	Vertical Sync End [1]	0
0	Vertical Sync End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the scanline at which the Vertical Sync pulse is to become inactive, thereby effectively specifying the Vertical Sync pulse width. In addition, this register contains controls for the vertical interrupt and two miscellaneous control bits, CR11[7:6].

Access to this register is controlled by CR3[7].

- When CR3[7] = 1, this register is read/write.
- When CR3[7] = 0, this register is write-only.

Bit	Description
7	**Write Protect CR7 through CR0:** When this bit: • = 0, CR0 through CR7 can be written normally. • = 1, CR0 through CR7 cannot be written, except for CR7[4], which can always be written.
6	**Refresh Cycle Control:** When this bit: • = 0, three refresh cycles will be executed per scanline. • = 1, five refresh cycles will be executed per scanline.
5	**Disable Vertical Interrupt:** When this bit: • = 0, vertical interrupt is enabled and functions normally. • = 1, vertical interrupt is disabled, and the INTR pin cannot go active.
4	**Clear Vertical Interrupt:** When this bit: • = 0, the Interrupt Pending Bit (FEAT[7]) will be cleared to 0, and the INTR pin will be forced inactive. • = 1, it has no effect

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6.4.19 CR11: Vertical Sync End Register *(cont.)*

Bit	Description
3:0	**Vertical Sync End [3:0]:** • This field determines the width of the Vertical Sync pulse. • The value of this field is compared with the least-significant four bits of the Scanline Counter. When a match occurs, the Vertical Sync pulse is ended. • The Vertical Sync pulse is limited to 15 scanlines. • The vertical sync end value to be programmed into this register may be calculated as follows: FROM: Vertical sync start (value programmed in CR10 and CR7[7,2]) SUBTRACT: – Vertical sync width (as desired) TO GET: = Vertical sync end The vertical sync pulse must never be programmed to extend past the Vertical Total. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

6.4.20 CR12: Vertical Display End Register

I/O Port Address: 3?5

Index: 12

Bit	Description	Reset State
7	Vertical Display End [7]	0
6	Vertical Display End [6]	0
5	Vertical Display End [5]	0
4	Vertical Display End [4]	0
3	Vertical Display End [3]	0
2	Vertical Display End [2]	0
1	Vertical Display End [1]	0
0	Vertical Display End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

The Vertical Display End field is used to specify the scanline at which the display is to end.

Bit	Description
7:0	**Vertical Display End [7:0]:** The Vertical Display End field is used to specify the scanline at which the display is to end. • The least-significant eight bits [7:0] of this field are in this register. • The most-significant two bits [9:8] are in register CR7[6,1]. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.21 CR13: Offset Register

I/O Port Address: 3?5

Index: 13

Bit	Description	Reset State
7	Offset [7]	0
6	Offset [6]	0
5	Offset [5]	0
4	Offset [4]	0
3	Offset [3]	0
2	Offset [2]	0
1	Offset [1]	0
0	Offset [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the display 'pitch,' which is the distance in the display memory between the beginnings of adjacent character rows or scanlines.

Bit	Description
7:0	**Offset [7:0]:** This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This field is extended to nine bits with Extension Register CR1B[4]. Except for the first scanline, to calculate the address from which to begin fetching data, add the contents of this register CR13 to the beginning address of the previous scanline or character row. Depending on the value of CR17[6], the offset will shift left either no or one bit positions.

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6.4.22 CR14: Underline Row Scanline Register

I/O Port Address: 3?5

Index: 14

Bit	Description	Reset State
7	Reserved	0
6	Double-Word Mode	0
5	Count by Four	0
4	Underline Scanline [4]	0
3	Underline Scanline [3]	0
2	Underline Scanline [2]	0
1	Underline Scanline [1]	0
0	Underline Scanline [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to enable or disable access to the Extension Registers.

Bit	Description
7	Reserved
6	**Double-Word Mode:** When this bit: • is 1, double-word addressing is selected. — The CRTC Memory Address Counter is rotated left for two bit positions. — As a result, display memory address bits MA[1] and MA[0] are sourced from CRTC Address Counter bits [13] and [12], respectively. • is 0, CR17[6] controls whether the CL-GD7542 uses the byte-address mode or the word-address mode.
5	**Count by Four:** When Double-Word mode: • is not enabled (CR14[6] = 0), this bit must be cleared to 0. • is enabled (CR14[6] = 1), this bit must be set to 1 to clock the Memory Address Counter with Character Clock divided by four.
4 0	**Underline Scanline [4:0]:** Within a character cell, this field specifies the scanline where the underline occurs

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6.4.23 CR15: Vertical Blanking Start Register

I/O Port Address: 3?5

Index: 15

Bit	Description	Reset State
7	Vertical Blanking Start [7]	0
6	Vertical Blanking Start [6]	0
5	Vertical Blanking Start [5]	0
4	Vertical Blanking Start [4]	0
3	Vertical Blanking Start [3]	0
2	Vertical Blanking Start [2]	0
1	Vertical Blanking Start [1]	0
0	Vertical Blanking Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the scanline at which blanking is to become active.

Bit	Description
7:0	**Vertical Blanking Start [7:0]:** This 10-bit field specifies the scanline on which vertical blanking is to start. • The least-significant eight bits [7:0] of this field are in this register. • The most-significant two bits [9:8] of this field are in CRT Controller Registers CR9[5] and CR7[3]. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.24 CR16: Vertical Blanking End Register

I/O Port Address: 3?5

Index: 16

Bit	Description	Reset State
7	Vertical Blanking End [7]	0
6	Vertical Blanking End [6]	0
5	Vertical Blanking End [5]	0
4	Vertical Blanking End [4]	0
3	Vertical Blanking End [3]	0
2	Vertical Blanking End [2]	0
1	Vertical Blanking End [1]	0
0	Vertical Blanking End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

The Vertical Blanking End field specifies the scanline at which vertical blanking is to end.

Bit	Description
7:0	**Vertical Blanking End [7:0]:** The Vertical Blanking End field specifies the scanline at which vertical blanking is to end. When Extension Register CR1B[5] • = 0, the entire field is the eight bits of CRT Controller Register CR16[7:0]. • = 1, the field is extended to ten bits with Extension Register CR1A[7:6]. The contents of the Vertical Blanking End field are compared to the scanline counter to determine when to terminate vertical blanking. • If CR1B[5] is 0, this comparison limits the duration of vertical blanking to 255 scanlines. • If CR1B[5] is, this comparison does not limit the duration of vertical blanking to 255 scanlines. (That is, the duration of vertical blanking may be more than 255 scanlines.) For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.25 CR17: Mode Control Register

I/O Port Address: 3?5

Index: 17

Bit	Description	Reset State
7	CRTC Timing Logic Enable	0
6	Byte/Word Address Mode	0
5	Address Rotation	0
4	Reserved	
3	Count by Two	0
2	Multiply Vertical Registers by Two	0
1	Compatibility-Mode (Hercules™) Support	0
0	Compatibility-Mode (CGA) Support	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains a number of miscellaneous control bits.

Bit	Description
7	**CRTC Timing Logic Enable:** When this bit: • = 1, CRTC timing logic is enabled and functions normally. • = 0, CRTC timing logic is disabled, forcing a reset condition.
6	**Byte/Word Address Mode:** • When this bit = 1: — The Byte-Address mode is enabled. — Before the contents of the CRTC Address Counter are sent to display memory, they are not rotated. • When this bit = 0: — The Word-Address mode is enabled. — Before the contents of the CRTC Address Counter are sent to display memory, they are rotated left one bit position.
5	**Address Rotation:** • When CR17[6] = 1, this bit is ignored. • When CR17[6] = 0. — and this bit is 1, the left rotation described in CR17[6] above involves 16 bits of the CRTC Address Counter. — and this bit is 0, the left rotation described in CR17[6] above involves 14 bits of the CRTC Address Counter.
4	Reserved.

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6.4.25 CR17: Mode Control Register *(cont.)*

Bit	Description
3	**Count by Two:** When this bit: • = 1, the CL-GD7542 clocks the Memory Address Counter with the Character Clock, divided by two. • = 0, the CL-GD7542 clocks the Memory Address Counter with the Character Clock.
2	**Multiply Vertical Registers by Two:** When this bit: • is 1, the Scanline Counter is clocked with Horizontal Sync, divided by two. (In effect, the Vertical Registers are multiplied by two.) — This division allows the number of scanlines to be doubled to 2048. — All periods will be even multiples of two scanlines. • is 0, the Scanline Counter is clocked with Horizontal Sync. — As a result, the number of scanlines is 1024.
1	**Compatibility-Mode (Hercules™) Support:** When this bit: • = 0, Scanline Counter bit [1] is substituted for CRTC Address Counter [14]. This substitution provides for Hercules™ compatibility. • = 1, the substitution described above does not occur.
0	**Compatibility-Mode (CGA) Support:** When this bit: • = 0, Scanline Counter bit [0] is substituted for CRTC Address Counter [14]. This substitution provides for CGA compatibility. • = 1, the substitution described above does not occur.

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6.4.26 CR18: Line Compare Register

I/O Port Address: 3?5

Index: 18

Bit	Description	Reset State
7	Line Compare [7]	0
6	Line Compare [6]	0
5	Line Compare [5]	0
4	Line Compare [4]	0
3	Line Compare [3]	0
2	Line Compare [2]	0
1	Line Compare [1]	0
0	Line Compare [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

The Line Compare field is used to specify where Screen A ends and Screen B starts for a vertically split screen.

Bit	Description
7:0	**Line Compare [7:0]:** The Line Compare field is used to implement a vertically split screen by specifying where Screen A ends and Screen B starts. • This register contains the eight least-significant bits [7:0] of this field. • The two most-significant bits [9:8] are in CR9[6] and CR7[4]. The top portion of the split screen is called Screen A. • Screen A may start anywhere in display memory. • Screen A can be panned and scrolled on a pixel-by-pixel basis. The bottom portion of the split screen is called Screen B. • Screen B always starts at location 0 in display memory. • Screen B cannot be panned or scrolled.

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6.4.27 CR22: Graphics Controller Data Latches Readback Register

I/O Port Address: 3?5

Index: 22

Bit	Description	Reset State
7	Graphics Controller Data Latch n Readback [7]	0
6	Graphics Controller Data Latch n Readback [6]	0
5	Graphics Controller Data Latch n Readback [5]	0
4	Graphics Controller Data Latch n Readback [4]	0
3	Graphics Controller Data Latch n Readback [3]	0
2	Graphics Controller Data Latch n Readback [2]	0
1	Graphics Controller Data Latch n Readback [1]	0
0	Graphics Controller Data Latch n Readback [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register address is used to read the Graphics Controller Data Latches.

Bit	Description
7:0	**Graphics Controller Data Latch n Readback [7:0]:** This read-only register may be used to read back the contents of one of the four VGA graphics controller display memory data latches. • The number of the display memory data latch that is read back is selected with Graphics Controller Register GR4[1:0]. • The graphics controller data latches are loaded whenever display memory is read by the CPU.

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6.4.28 CR24: Attribute Controller Toggle Readback Register

I/O Port Address: 3?5

Index: 24

Bit	Description	Reset State
7	Attribute Controller Data-Index Toggle Readback	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register provides access to the Attribute Controller Toggle.

Bit	Description
7	**Attribute Controller Data-Index Toggle Readback:** When this bit: • = 1, on the next access, the Attribute Controller reads or writes a data value. • = 0, on the next access, the Attribute Controller reads or writes an index value.
6:0	Reserved

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6.4.29 CR26: Attribute Controller Index Readback Register

I/O Port Address: 3?5

Index: 26

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Video Enable Status	0
4	Attribute Controller Index [4]	0
3	Attribute Controller Index [3]	0
2	Attribute Controller Index [2]	0
1	Attribute Controller Index [1]	0
0	Attribute Controller Index [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register provides access to the current Attribute Controller Index.

Bit	Description
7:6	Reserved
5	**Video Enable Status:** This bit provides the status of the Video Enable bit in Attribute Controller Index Register ARX[5].
4:0	**Attribute Controller Index [4:0]:** This field reads back the value that is in Attribute Controller Index ARX[4:0].

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6.5 Graphics Controller Registers

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6.5.1 GRX: Graphics Controller Index Register

I/O Port Address: 3CE

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Graphics Controller Index [5]	0
4	Graphics Controller Index [4]	0
3	Graphics Controller Index [3]	0
2	Graphics Controller Index [2]	0
1	Graphics Controller Index [1]	0
0	Graphics Controller Index [0]	0

This register is used to specify a graphics controller register.

Bit	Description
7:6	Reserved
5:0	**Graphics Controller Index [5:0]:** This field specifies one of the following: • a register in the Graphics Controller group • an Extension Register that is accessed by the next I/O read or I/O write to I/O Port Address 3CF.

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6.5.2 GR0: Set / Reset Register

I/O Port Address: 3CF

Index: 0

Bit	Description	Reset State
7	Write Mode 5 Background [7] / Reserved	0
6	Write Mode 5 Background [6] / Reserved	0
5	Write Mode 5 Background [5] / Reserved	0
4	Write Mode 5 Background [4] / Reserved	0
3	Write Mode 5 Background [3] / Set/Reset Plane 3	0
2	Write Mode 5 Background [2] / Set/Reset Plane 2	0
1	Write Mode 5 Background [1] / Set/Reset Plane 1	0
0	Write Mode 5 Background [0] / Set/Reset Plane 0	0

This register specifies:

- the background color, when Extended Write Mode 5 is selected.
- values to be written into the respective display memory planes when the processor executes a Write Mode 0 or Write Mode 3 operation.

For an overview of Write Modes, refer to the description in Graphics Controller Register GR5.

Bit	Description
7:0	**Write Mode 5 Background [7:0]:** When Graphics Controller Register GR5[2:0] selects Extended Write Mode 5, these bits [7:0] specify the background color for Extended Write Mode 5.
7:4	**Reserved:** • When Graphics Controller Register GR5[2:0] does not select Extended Write Mode 5, these bits are reserved. • When Extension Register GRB[2]: — is 0, writes to these bits are ignored, and reads return zeroes. — is 1, these bits are read/write, but bit contents are not used.
3:0	**Set/Reset Plane [3:0]:** When Graphics Controller Register GR5[2:0] does not select Extended Write Mode 5, these bits [3:0] control the values written into the respective display memory planes for Write Mode 3 and Write Mode 0.

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6.5.3 GR1: Set / Reset Enable Register

I/O Port Address: 3CF

Index: 1

Bit	Description	Reset State
7	Write Mode 4, 5 Foreground [7] / Reserved	0
6	Write Mode 4, 5 Foreground [6] / Reserved	0
5	Write Mode 4, 5 Foreground [5] / Reserved	0
4	Write Mode 4, 5 Foreground [4] / Reserved	0
3	Write Mode 4, 5 Foreground [3] / Enable Set/Reset Plane 3	0
2	Write Mode 4, 5 Foreground [2] / Enable Set/Reset Plane 2	0
1	Write Mode 4, 5 Foreground [1] / Enable Set/Reset Plane 1	0
0	Write Mode 4, 5 Foreground [0] / Enable Set/Reset Plane 0	0

This register:

- defines the foreground color when Extended Write Mode 4 or 5 is selected.
- is used with Graphics Controller Register GR0 to determine values to be written into the respective display memory planes when Write Mode 0 is selected.

For an overview of Write Modes, refer to the description in Graphics Controller Register GR5.

Bit	Description
7:0	**Write Mode 4, 5 Foreground [7:0]:** These bits specify the foreground color for an Extended Write Mode when: • Extended Write Mode 4 is selected. (Graphics Controller Register GR5[2:0] is 100). • Extended Write Mode 5 is selected. (Graphics Controller Register GR5[2:0] is 101).
7 4	**Reserved:** • When Graphics Controller Register GR5[2:0] selects Extended Write Mode 4 or 5, these bits are reserved. • When Extension Register GRB[2]: — is 0, writes to these bits are ignored, and reads return zeroes. — is 1, these bits are read/write, but bit contents are not used.
3 0	**Enable Set / Reset Plane [3:0]:** When Write Mode 0 is selected (Graphics Controller Register GR5[2:0] is 000) and when a bit in this field: • = 1, the corresponding value in Graphics Controller Register GR0[3:0] is written into the corresponding display memory plane. • = 0, the corresponding value from the CPU data bus is written into the corresponding display memory plane.

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6.5.4 GR2: Color Compare Register

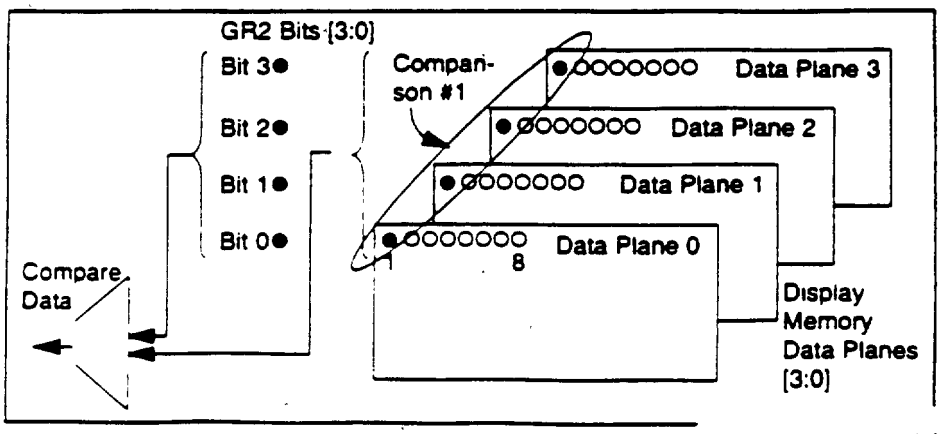
I/O Port Address: 3CF

Index: 2

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Compare Plane [3]	0
2	Color Compare Plane [2]	0
1	Color Compare Plane [1]	0
0	Color Compare Plane [0]	0

This register specifies the color compare plane(s) for Read Mode 1.

Bit	Description
7:4	Reserved
3:0	**Color Compare Plane [3:0]:** This field represents a color comparison value consisting of 1 to 4 bits. • GR5[3] must be set to 1 (Read Mode 1 is selected) to enable this field. • GR7[3:0] bits select display memory data planes for the comparison below. • For each selected display memory data plane, the color value of the corresponding bit in this field is compared to the color of the eight neighboring horizontal pixels in the corresponding display memory data plane. (For display memory data planes that are not chosen, their data is forced to match the values of the other data planes, becoming a "don't care" in the process.) • The eight bits from the comparison are read into the CPU.



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6.5.5 GR3: Data Rotate Register

I/O Port Address: 3CF

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Logical Function Select [1]	0
3	Logical Function Select [0]	0
2	Data Rotate Count [2]	0
1	Data Rotate Count [1]	0
0	Data Rotate Count [0]	0

This register contains two fields that are used with Write Modes 0 and 3.

Bit	Description
7:5	Reserved
4:3	**Logical Function Select [1:0]:** This two-bit field: • is used for Write Mode 0 only (Graphics Controller Register GR5[2:0] is 000). • selects the logical function operation that takes place between the data in the CPU data latches and the data from the CPU or Set/Reset Logic. The result of the functional operation is written into display memory. The logical function operations are summarized in the following table:

GR3		Logical Function Operation
[4]	[3]	
0	0	None. The data in the latches are ignored.
0	1	Data in latches is logically ANDed with data from CPU or Set/Reset Logic
1	0	Data in latches is logically ORed with data from CPU or Set/Reset Logic
1	1	Data in latches is logically XORed with data from CPU or Set/Reset Logic

2 0	**Data Rotate Count [2:0]:** This field allows data from the CPU bus to be rotated up to seven bit positions prior to being altered by the Set/Reset logic.

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6.5.6 GR4: Read Map Plane Select Register

I/O Port Address: 3CF

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Display Memory Data Plane Select [1]	0
0	Display Memory Data Plane Select [0]	0

This register is used to select a display memory data plane for Read Mode 0. (For an overview of the Write Modes, refer to the description in GR5.)

Bit	Description
7:2	Reserved
1:0	**Display Memory Data Plane Select [1:0]:** This field: • is used only when Read Mode 0 is selected (Graphics Controller Register GR5[3] = 1). • specifies the display memory data plane selected for a read by Read Mode 0, as shown in the following table:

GR4		Display Memory Data Plane Selected for Read by Read Mode 0
[1]	[0]	
0	0	Display Memory Data Plane 0
0	1	Display Memory Data Plane 1
1	0	Display Memory Data Plane 2
1	1	Display Memory Data Plane 3

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6.5.7 GR5: Mode Register

I/O Port Address: 3CF

Index: 5

Bit	Description	Reset State
7	Reserved	
6	256-Color Mode	0
5	Video Data Shift Register Mode	0
4	Odd/Even Addressing Mode	0
3	Read Mode	0
2	Write Mode [2]	0
1	Write Mode [1]	0
0	Write Mode [0]	0

This register specifies the Write Mode and Read Mode. In addition, it controls the configuration of the video data shift registers.

Bit	Description
7	Reserved
6	**256-Color Mode:** When this bit: • = 1, video data shift registers are configured for 256-color video modes, and Graphics Controller Register GR5[5] is ignored. • = 0, video data shift registers are configured for 16-, 4-, or 2-color video modes.
5	**Video Data Shift Register Mode:** When this bit: • = 0, video data shift registers are configured for EGA compatibility. • = 1, video data shift registers are configured for CGA compatibility, which is used for video modes 4 and 5.
4	**Odd/Even Addressing Mode:** • When this bit is 1, the CL-GD7542 is configured for odd/even addressing. • This bit should always be programmed to the opposite value as Sequencer Register SR4[2].

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6.5.7 GR5: Mode Register *(cont.)*

Bit **Description**

3 **Read Mode:**

This bit specifies whether the CL-GD7542 is in Read Mode 0 or Read Mode 1.

GR5 [3]	Read Mode	CPU Read Source
0	Read Mode 0	CPU reads data directly from display memory
1	Read Mode 1	CPU reads data that results from the color-compare logic of GR2

Read Mode 0:

- During Read Mode 0, the CPU reads data directly from display memory.
- Read Mode 0 returns eight adjacent bits of the display memory data plane specified in GR4[1:0].
- Read Mode 0 does not use the color-compare logic of register Graphics Controller Register GR2.
- A Read Mode 0 operation can be forced with an I/O read of CRT Controller Register CR22, the Graphics Controller Data Latches Readback Register.

Read Mode 1:

- During Read Mode 1, the CPU reads data that results from the color-compare logic of Graphics Controller Register GR2.
- Read Mode 1 allows eight adjacent pixels (16-color modes) to be compared to a specified color value in a single operation. Each of the eight bits returned to the CPU indicates the result of a comparison between the four bits of the Color Compare (Graphics Controller Register GR2[3:0]) and the bits from the four display memory planes.
- When the four bits of the Color Compare operation match the four bits from the display memory data planes, a 1 is returned for the corresponding bit position.
- When any bits in the Color Don't Care Plane (Graphics Controller Register GR7[3:0]) are zeroes, the value in the corresponding display memory data plane is forced to match the values of the other data planes, becoming a "don't care" in the process.

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6.5.7 GR5: Mode Register *(cont.)*

Bit **Description**

2:0 **Write Mode [2:0]:**

These bits specify if the CL-GD7542 is in Write or Extended Write Mode.

- When Extension Register GRB[2]=0, GR5[2] is forced to 0.

GR5			Write Mode Selected	
[2]	[1]	[0]		
0	0	0	GRB[2] = 0 forces GR5[2] = 0	Write Mode 0
0	0	1		Write Mode 1
0	1	0		Write Mode 2
0	1	1		Write Mode 3
1	0	0	Extended Write Mode 4	
1	0	1	Extended Write Mode 5	
1	1	0	Reserved	
1	1	1	Reserved	

Write Mode 0:

- Each of the four display memory data planes is written with the CPU data rotated by the number of counts in Graphics Controller Register GR3[2:0].
- When a bit in Graphics Controller Register GR1[3:0] is 1:
  - — the corresponding display memory data plane is written with the contents of the corresponding bit in GR0[3:0].
  - — under the control of GR3[4:3], the contents of CPU data latches may be logically combined with data from the set/reset logic.
- Bit planes are enabled with Sequencer Register SR2[3:0].
- Bit positions are enabled with Graphics Controller Register GR8.

Write Mode 1:

- Each of the four display memory data planes is written with data in CPU data latches, loaded from display memory by a previous read.
- Write Mode 1 ignores Graphics Controller Register GR8.

Write Mode 2:

- Display memory data planes [3:0] are written with CPU data bit values [3:0].
- Bit planes are enabled with Sequencer Register SR2[3:0].
- Bit positions are enabled with Graphics Controller Register GR8.
- Write Mode 2 ignores the data rotator, set/reset, and function-select fields.

Write Mode 3:

- Display memory plane data comes from corresponding bits of GR0[3:0].
- The bit-position-enable field is formed with the logical AND of Graphics Controller Register GR8 and the rotated CPU data.
- Write Mode 3 ignores the set/reset and function-select fields.

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6.5.7 GR5: Mode Register *(cont.)*

Bit **Description**

2:0(cont.)

Extended Write Mode 4:

- The contents of GR1[7:0] are written into up to eight adjacent pixels.
- The CPU data bits are used to control whether a pixel is written.
  - — When a CPU data bit is a 1, the corresponding pixel is written.
  - — When a CPU data bit is a 0, the corresponding pixel is not changed.
- This mode can be used for 256-color text expansion for which the background is to be preserved.
- This mode can also be used for 64K-color text expansion for which the background is to be preserved.

Extended Write Mode 5:

- The contents of either GR1[7:0] or GR0[7:0] are written into each of eight adjacent pixels.
- For each of the eight pixels, the choice between GR1 and GR0 is made according to the value of the corresponding bit of the CPU data, summarized in the following table.

CPU Data	GR0 / GR1	Note
0	GR0	Background
1	GR1	Foreground

- This mode is intended for 256-color text expansion, for which both the foreground and background are to be written.
- This mode can also be used for 64K-color text expansion for which both the foreground and background are to be written.

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6.5.8 GR6: Miscellaneous Register

I/O Port Address: 3CF

Index: 6

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Display Memory Map [1]	0
2	Display Memory Map [0]	0
1	Chain Odd Maps to Even	0
0	Graphics Mode	0

This register contains miscellaneous control bits.

Bit 7:4 — Reserved

Bit 3:2 — **Display Memory Map [1:0]:**
This field specifies the beginning address and size of the display memory in the CPU host address space. This field is summarized in the following table:

GR6 [3]	GR6 [2]	Display Memory Map Plane	Display Memory Address in CPU Host Address Space	Display Memory Size (Kbytes)	Affected Mode(s)
0	0	0	A000:0 to BFFF:F	128	Extended
0	1	1	A000:0 to AFFF:F	64	EGA / VGA
1	0	2	B000:0 to BFFF:F	32	Hercules
1	1	3	B800:0 to BFFF:F	32	CGA

Bit 1 — **Chain Odd Maps to Even:**
- When this bit is 1, CPU Address Bit[0] is replaced with a higher-order address bit. This replacement causes the even host addresses to access Planes 0 and 2, and the odd host addresses to access Planes 1 and 3.
- This mode is useful for MDA emulation.

Bit 0 — **Graphics Mode:**
When this bit:
- = 0, the CL-GD7542 functions in text (alphanumeric) modes.
- = 1, the CL-GD7542 functions in graphics (all-points-addressable) modes.

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6.5.9 GR7: Color Don't-Care Plane Register

I/O Port Address: 3CF

Index: 7

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Don't-Care Plane [3]	0
2	Color Don't-Care Plane [2]	0
1	Color Don't-Care Plane [1]	0
0	Color Don't-Care Plane [0]	0

This register is used with Graphics Controller Register GR2 for Read Mode 1 accesses. (For an overview of the Read Modes, refer to the description of Graphics Controller Register GR5.)

Bit	Description
7:4	Reserved
3:0	**Color Don't-Care Plane [3:0]:** These four bits are used to control color compare logic for the four Color Don't-Care Planes. If a bit: • = 1, the corresponding plane is involved in color compares. • = 0, the corresponding plane is not involved in color compares.

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6.5.10 GR8: Display Memory Bit Mask Register

I/O Port Address: 3CF

Index: 8

Bit	Description	Reset State
7	Display Memory Bit Write Enable [7]	0
6	Display Memory Bit Write Enable [6]	0
5	Display Memory Bit Write Enable [5]	0
4	Display Memory Bit Write Enable [4]	0
3	Display Memory Bit Write Enable [3]	0
2	Display Memory Bit Write Enable [2]	0
1	Display Memory Bit Write Enable [1]	0
0	Display Memory Bit Write Enable [0]	0

This register is used to control writing to display memory on a bit basis in Write Modes 0, 2, and 3.

Bit	Description
7:0	**Display Memory Bit Write Enable [7:0]:** Each bit in this register controls whether the corresponding bit in display memory is written in Write Modes 0, 2, or 3. When a bit: • = 1, the corresponding bit in display memory is written. • = 0, the corresponding bit in display memory is not written.

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6.6 Attribute Controller Registers

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6.6.1 ARX: Attribute Controller Index Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Video Enable	0
4	Attribute Controller Index [4]	0
3	Attribute Controller Index [3]	0
2	Attribute Controller Index [2]	0
1	Attribute Controller Index [1]	0
0	Attribute Controller Index [0]	0

This register is used to specify the register in the Attribute Controller block that is accessed with the next I/O write to 3C0 or I/O read to 3C1.

For the Attribute Controller block, both the index and data registers are at the same port addresses, unlike other blocks, for which index and data registers are at different port addresses.

Alternate writes to ARX toggle between index and data. The CRT Controller Register CR24 provides access to the Attribute Controller Toggle, which reads or writes either a data value or an index value.

Bit	Description
7:6	Reserved
5	**Video Enable:** When this bit: • = 0, the screen displays the color indicated by AR11. • = 1, the screen displays normal video.
4 0	**Attribute Controller Index [4:0]:** This field is the index to the Attribute Controller data registers. The CRT Controller Register CR24 provides access to the current Attribute Controller index value.

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6.6.2 AR0 to ARF: Attribute Controller Palette Registers

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 0:F

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Red	0
4	Secondary Green / Intensity	0
3	Secondary Blue / Monochrome	0
2	Red	0
1	Green	0
0	Blue	0

These bits act as pointers to palette entries.

Bit	Description
7:6	Reserved
5:0	**Palette Entries:** In 16-color text and graphics modes, the digital attribute controller palette entries in this register are chosen by the four bits of pixel data, and they point to palette memory entries. • The palette memory entries are normally programmed, and so the DAC outputs reflect these values. • As a result, the palette memory is programmed to simulate standard EGA colors.

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6.6.3 AR10: Attribute Controller Mode Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 10

Bit	Description	Reset State
7	AR14 Video Source Enable	0
6	Pixel Double-Clock Select	0
5	Pixel Panning Compatibility	0
4	Reserved	
3	Character Blink Enable	0
2	Line Graphics Enable	0
1	Display Type	0
0	Graphics Mode	0

This register contains some miscellaneous control bits for the Attribute Controller.

Bit	Description
7	**AR14 Video Source Enable:** • When an 8-, 16-, or 24-bit pixel mode is chosen, this bit is ignored. • When this bit: — = 1, AR14[1:0] are used as the source for the Color Lookup Table address bits [5:4], which allows rapid selection of four 16-color palettes. — = 0, palette registers AR0 to ARF[5:4] are used as the source for the Color Lookup Table address bits [5:4].
6	**Pixel Double-Clock Select:** • When this bit is 0, pixels are clocked on every cycle. • When this bit is 1, pixels are clocked on every other clock cycle. Also: — Registers AR0 to ARF are bypassed. — This bit setting is used with Mode 13. — The CL-GD7542 sequencer logic operates at twice the pixel clock rate.
5	**Pixel Panning Compatibility:** When this bit: • = 0, the two parts of a split screen pan together. • = 1, a line compare match in the CRTC forces the output of the AR13 Pixel Panning Register to a 0 until the next VSYNC occurs. This action allows the panning of Screen A without Screen B.
4	Reserved
3	**Character Blink Enable:** When this bit: • = 0, character blinking is disabled • = 1, character blinking is enabled at the frequency rate of vertical refresh, divided by 32.

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6.6.3 AR10: Attribute Controller Mode Register *(cont.)*

Bit **Description**

2 **Line Graphics Enable:**
When this bit:
- = 0, bit 9 of a 9-bit-wide character cell is the same as the background.
- = 1, bit 9 of a 9-bit-wide character cell is made the same value as bit 8. This value is used for those character sets that have special characters associated with line graphics, for characters codes in the range C0 through DF.

1 **Display Type:**
This bit is used only if the CL-GD7542 is in alphanumeric modes When this bit:
- = 0, the Attribute Byte contents are treated as color attributes.
- = 1, the Attribute Byte contents are treated as MDA-compatible attributes.

The following table shows examples of monochrome attributes.

Bit Definitions for Attribute Byte								Hex Code Of Attribute Byte	Monochrome Attribute Byte
Blink Bit [7]	Background Bits			Intensity Bit [3]	Foreground Bits				
	[6]	[5]	[4]		[2]	[1]	[0]		
0	0	0	0	0	1	1	1	07h	Normal
0	0	0	0	1	1	1	1	0Fh	Intense
0	0	0	0	0	0	0	1	01h	Underline
0	0	0	0	1	0	0	1	09h	Underline Intense
0	1	1	1	0	0	0	0	70h	Reverse
1	1	1	1	0	0	0	0	F0h	Blinking Reverse

0 **Graphics Mode:**
When this bit:
- = 0, the Attribute Controller functions in text (alphanumeric) modes.
- = 1, the Attribute Controller functions in graphics (all-points-addressable) modes.

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6.6.4 AR11: Overscan (Border) Color Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 11

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	(Border Color Bit) Secondary Red	0
4	(Border Color Bit) Secondary Green	0
3	(Border Color Bit) Secondary Blue	0
2	(Border Color Bit) Red	0
1	(Border Color Bit) Green	0
0	(Border Color Bit) Blue	0

This register points to the entry in the Color Lookup Table that defines the Border Color.

- As shown in Figure 6–1 at CRT Controller Register CR0, the border is defined as that portion of the raster between blanking and active video, on all four sides of the screen.
- Typically, the Color Lookup Table entries are programmed, and so the color defined by the bits above is the color that results.

Bit	Description
7:6	Reserved
5.0	**Border Color Bits [5:0]:** Depending on if the CGA or EGA mode is in use, either four of these bits (for CGA) or six of these bits (for EGA) are used to select the Color Lookup Table entry for the Border Color in CGA and EGA Modes.

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6.6.5 AR12: Color Plane Enable Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 12

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Video Status Mux [1]	0
4	Video Status Mux [0]	0
3	Color Plane Enable [3]	0
2	Color Plane Enable [2]	0
1	Color Plane Enable [1]	0
0	Color Plane Enable [0]	0

This register contains:

- a field that chooses the inputs for diagnostic bits in STAT[5:4].
- a field that enables the four color planes in the Attribute Controller Palette Registers.

Bit	Description
7:6	Reserved
5:4	**Video Status Mux [1:0]:** This field chooses the inputs for the diagnostic status bits in STAT[5:4] as indicated in the following table:

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	FP[2] Red	FP[0] Blue
0	1	FP[3] Secondary Blue	FP[1] Green
1	0	FP[5] Secondary Red	FP[4] Secondary Green
1	1	FP[7]	FP[6]

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6.6.5 AR12: Color Plane Enable Register *(cont.)*

Bit	Description
3:0	**Color Plane Enable [3:0]:** This field controls which display memory data plane will send data to a corresponding attribute controller color palette register, as shown in the following table:

AR12 Bit / State	Display Memory Data Plane	Result
AR12[3] = 0	Plane 3	Plane 3 disabled.
AR12[3] = 1		Plane 3 data selected for Color Palette Register 3.
AR12[2] = 0	Plane 2	Plane 2 disabled.
AR12[2] = 1		Plane 2 data selected for Color Palette Register 2.
AR12[1] = 0	Plane 1	Plane 1 disabled.
AR12[1] = 1		Plane 1 data selected for Color Palette Register 1.
AR12[0] = 0	Plane 0	Plane 0 disabled.
AR12[0] = 1		Plane 0 data selected for Color Palette Register 0.

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6.6.6 AR13: Pixel Panning Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 13

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Pixel Panning [3]	0
2	Pixel Panning [2]	0
1	Pixel Panning [1]	0
0	Pixel Panning [0]	0

This register:

- specifies the number of pixels the display data are shifted to the left.
- functions both in the graphics (all-points-addressable) and text (alphanumeric) modes.

Bit	Description
7:4	Reserved
3:0	**Pixel Panning [3:0]:** This field controls fine panning on a pixel-by-pixel basis by specifying the number of pixels the display data are shifted to the left. The values programmed into AR13[3:0] are interpreted as indicated in the following table:

AR13 [3]	AR13 [2]	AR13 [1]	AR13 [0]	Hex Code	Shift for 9-Bit Characters	Shift for 8-Bit Characters	Shift for Mode 13
0	0	0	0	0h	1 bit left	(none)	(none)
0	0	0	1	1h	2 bits left	1 bit left	–
0	0	1	0	2h	3 bits left	2 bits left	1 bit left
0	0	1	1	3h	4 bits left	3 bits left	–
0	1	0	0	4h	5 bits left	4 bits left	2 bits left
0	1	0	1	5h	6 bits left	5 bits left	–
0	1	1	0	6h	7 bits left	6 bits left	3 bits left
0	1	1	1	7h	8 bits left	7 bits left	–
1000 to 1111				8h - Fh	no shift	1 bit right	–

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6.6.7 AR14: Color Select Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 14

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Bit C [7]	0
2	Color Bit C [6]	0
1	Color Bit C [5]	0
0	Color Bit C [4]	0

This register contains two fields that are involved in the selection of addresses into the Color Lookup Table.

Bit	Description
7:4	Reserved
3:2	**Color Bits C [7:6]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • These two bits are concatenated with the six bits from the Attribute Controller Palette Registers AR0 to ARF to form the address into the Color Lookup Table and to drive flat-panel interface pins FP[7:6].
1:0	**Color Bits C [5:4]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • When AR10[7]: — is 0, these two bits are ignored. — is 1, these two bits replace the corresponding two bits from the Attribute Controller Palette Registers AR0 to ARF to form the address into the Color Lookup Table and to drive flat-panel interface pins FP[5:4].

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6.7 Extension Registers

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6.7.1 SR6: Unlock All Extensions Registers

I/O Port Address: 3C5

Index: 6

Bit	Description	Reset State
7	Not Used	x
6	Not Used	x
5	Not Used	x
4	Unlock All Extension Registers	1
3	Not Used	x
2	Unlock All Extension Registers	0
1	Unlock All Extension Registers	1
0	Unlock All Extension Registers	0

This register is used to enable or disable access to all Extension Registers.

Bit	Description
7:0	**Unlock All Extensions Registers (Access Value):** When the value of this field: • is xxx1x010: — The field will be read as 00010010. — Extension Registers will be unlocked (enabled) for read/write access. • is any other value: — The field will be read as 00001111. — Extension Registers will be disabled for read/write access.

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6.7.2 SR7: Extended Sequencer Mode Register

I/O Port Address: 3C5

Index: 7

Bit	Description	Reset State
7	Memory Segment Select [3]	0
6	Memory Segment Select [2]	0
5	Memory Segment Select [1]	0
4	Memory Segment Select [0]	0
3	Reserved	
2	Select CRTC Character Clock Divider [1]	0
1	Select CRTC Character Clock Divider [0]	0
0	Select High-Resolution Packed-Pixel Mode	0

This register has several purposes which are described in the following bit descriptions.

Bit	Description
7:4	**Memory Segment Select [3:0]:** • When this programmed field value is 0000: — the CL-GD7542 will be configured for standard VGA display memory addressing, responding to memory accesses at Axxx:x, or Bxxx:x, or both, as specified by GR6[3:2]. • When this programmed field value is other than 0000: — the CL-GD7542 will be configured for 1-Mbyte linear memory addressing. — the CL-GD7542 will respond to any memory access for which CPU address bits[23:20] match this field value. • When this programmed field value is other than 0000 *and*: — when there is a full one Mbyte of display memory installed, *and* the CL-GD7542 is configured for extended 256-color chain-4, then the 1-Mbyte address range will have one-to-one mapping to the one Mbyte of installed display memory. — when the CL-GD7542 is configured for unchained, x8, or x16 addressing, then it will respond to the entire 1-Mbyte range, but address wrapping will take place. — GR8[5] is programmed to a 1, then SR7[4] becomes a don't-care bit, and the CL-GD7542 will respond to a 2-Mbyte address.
3	Reserved

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6.7.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit **Description**

2:1 **Select CRTC Character Clock Divider [1:0]:**
This field selects how the CRTC Character Clock is divided down, as indicated in the following table:

SR7		CRTC Character Clock Divider Mode
[2]	[1]	
0	0	Normal operation
0	1	CRTC Character Clock ÷ 2 for 16 bit/pixel data
1	0	CRTC Character Clock ÷ 3 for 24 bit/pixel data
1	1	16 bit/pixel data at pixel rate (only)

CRTC Character Clock ÷ 2 for 16-Bit/Pixel Data:
When this mode is selected:
- the DAC and Video Shift Register are clocked at the VCLK data byte rate
- the CRTC is clocked with a character clock of 8 pixels (16 VCLKs)

The above clocking allows:
- the CRTC timing value for 640 x 480 modes and 800 x 600 modes with 16-bit pixels to be programmed in units of an 8-pixel character clock.
- Offset Register CR13 to be set to:
  - A0h for 640 x 480 mode
  - C8h for 800 x 600 mode
- The hardware cursor x-position to be set in pixel units.
- The Cursor Data Invert function to operate on 15-, 16-, or 18-bit RGB data presented to the DAC.

CRTC Character Clock ÷ 3 for 24-Bit/Pixel Data:
When this mode is selected:
- the DAC and Video Shift Register is clocked at the VCLK data byte rate
- the CRTC is clocked with a character clock of 8 pixels (24 VCLKs)

The above clocking allows:
- the CRTC timing value for 640 x 480 modes with 24-bit pixels to be programmed in units of an 8-pixel character clock.
- Offset Register CR13 Offset Register to be set to F0h.

The hardware cursor is not supported in this configuration.

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6.7.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit	Description
2:1 *(cont.)*	**Select CRTC Character Clock Divider [1:0]:** **16-Bit/Pixel Data at Pixel Rate:** When this mode is selected: • the sequencer will provide 16-bit data to the palette DAC at the displayed pixel rate. This action allows 5-5-5 or 5-6-5 color modes to be selected with a 1x VCLK. • The data at P[7:0] will be only the low-byte of the pixel data. (The high-byte of the pixel data is not available externally.) • This mode also provides for 1024 x 768 display modes, with 5-5-5 or 5-6-5 color, and with VCLK equal to the pixel rate.
0	**Select High-Resolution Packed-Pixel Mode:** When this bit is 1: • Video shift registers are configured so one character clock equals 8 pixels. • True packed-pixel memory addressing is enabled. • This mode may also be used with 16- and 24-bit pixel modes. (Refer to SR7[2:1].) • This mode may not be used with video mode 13, which is packed pixel, but not high resolution. For video mode 13, set AR10[6] = 1. Notes: *In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses.* *In contrast, with chain-4 addressing, consecutive pixels are stored at every fourth address in display memory.*

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6.7.3 SR8: Miscellaneous Control

I/O Port Address: 3C5

Index: 8

Bit	Description	Access	Reset State
7(MSB)	Not Used	-	
6	Reserved	-	
5	Latch FCESYNC# and FCEVIDEO#	R/W	0
4	Reserved	-	
3	Reserved	-	
2	Reserved	-	
1	Reserved	-	
0(LSB)	Reserved	-	

Bit	Description
7	Not Used
6	Reserved
5	**Latch FCESYNC# and FCEVIDEO#:** When this bit is 1, the values on the FCESYNC# and FCEVIDEO# inputs are latched, so that the pins can be used for other functions.
4:0	Reserved

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6.7.4 SR9, SRA: Scratch Pad 0 and 1 Registers

I/O Port Address: 3C5

Index: 9, A

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD7542 BIOS and must never be written by any application program. They are listed here only for completeness.

Bit	Description
7:0	These bits are reserved for the Cirrus Logic, Inc., BIOS.

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6.7.5 SRB, SRC, SRD, SRE: VCLK0, 1, 2, 3 Numerator Registers

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description	Reset State
7	Reserved	
6	VCLK Numerator [6]	0
5	VCLK Numerator [5]	0
4	VCLK Numerator [4]	0
3	VCLK Numerator [3]	0
2	VCLK Numerator [2]	0
1	VCLK Numerator [1]	0
0	VCLK Numerator [0]	0

These registers, in conjunction with Extension Registers SR1B to SR1E, are used to determine the frequency of video clocks VCLKs. (For more information, refer to Appendix A7.)

Bit	Description
7	Reserved
6:0	**VCLK Numerator [6:0]:** The following table shows VCLK-related default values loaded at system reset. The default values are determined by the expression explained on the following page. (For more information on the VCLK denominator and post-scalar, refer to Extension Registers SR1B to SR1E.)

Table 6–2. VCLK Numerator, Denominator, and Post-scalar Values

VCLKi and Frequency		VCLK Numerator Values			DCLK Numerator Values			
VCLKi	VCLKi Frequency	Numerator Register and Hex Value in Register		*NB* = Value Used in Equation Numerator	Denominator Register and Hex Value in Register		*DB* = Value Used in Equation Denominator, Resulting from Post-Scalar	*P* = Post-Scalar Value Used in Equation Denominator
	MHz	Register	Hex	Decimal Equivalent of Hex Value	Register	Hex	Decimal	Decimal
VCLK0	25.180	SRB	66h	102	SR1B	3Bh	29	1
VCLK1	28.325	SRC	5Bh	91	SR1C	2Fh	23	1
VCLK2	41.165	SRD	45h	69	SR1D	30h	24	0
VCLK3	36.082	SRE	7Eh	126	SR1E	19h	25	1

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6.7.5 SRB, SRC, SRD, SRE: VCLK0, 1, 2, 3 Numerator Registers *(cont.)*

Bit	Description
6:0 *(cont.)*	**VCLK Numerator [6:0]:**

Each Video Clock frequency is determined by the following expression:

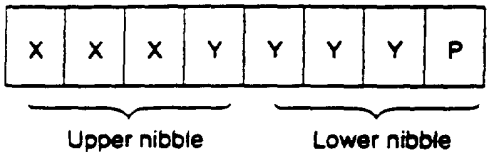
$$\text{VCLK i (MHz)} = \frac{\text{OSC} \times \text{NR}}{\text{DR} \times [\text{P} + 1]}$$

Where:

VCLK i	= Video Clock i, where i = 0, 1, 2, 3
OSC	= Input Clock, 14.31818 MHz
Numerator Register	= Value of Register SRi [6:0], where i = B, C, D, E
Denominator Register	= Value of Register SR1i [5:1], where i = B, C, D, E
Post-scalar	= Value of Register SR1i [0], where i = B, C, D, E

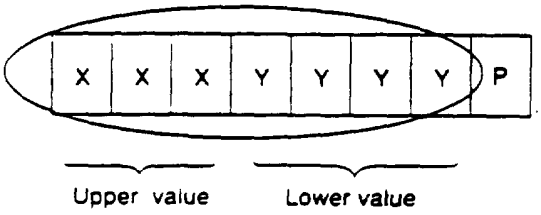
The DR denominator value is determined as follows:

1. The hex value programmed in the appropriate denominator register is read.



Hex number read:
Upper nibble = Values in XXXY.
Lower nibble = Values in YYY, plus post-scalar P = YYYP.

2. To extract a value to be used in the equation, the post-scalar value is ignored, which has the effect of shifting all values in the register to the right.



Circled area is what is actually used in the equation.
Upper value = Values in XXX. Lower value = Values in YYYY.

3. The value that is extracted is converted to decimal and plugged into the equation, along with P, the post-scalar value, which is obtained from Table 6–2

6.7.6 SRF: DRAM Control Register

I/O Port Address: 3C5

Index: F

Bit	Description	Reset State
7	DRAM Bank Select	0
6	Disable CPU-Write FIFO Fast-Page-Detection Mode	0
5	CRT FIFO Depth Control	0
4	Display Memory Data Bus Width [1]	0
3	Display Memory Data Bus Width [0]	0
2	DRAM RAS Timing	0
1	Reserved	0
0	Multiple-CAS# / Multiple-WE# DRAM Select	1

This register is used to control the display memory.

Bit	Description
7	**DRAM Bank Select:** • This bit is used with SRF[4:3] to specify the display memory data bus width according to the number of banks of display memory used. • When this bit: — is 1, the CL-GD7542 is configured for two banks of display memory (four 256K x 16 DRAMs). — is 0, the CL-GD7542 is configured for one bank of display memory (four 512K x 8 DRAMS, or two 256K x 16 DRAMs).
6	**Disable CPU-Write FIFO Fast-Page-Detection Mode:** • To avoid CPU write buffer under-runs, this bit *must* be programmed to 1, either when loading font data for page-mode font access, or when performing multiple color-expand writes in 16-bit pixel modes. • When this bit: — is 1, CPU writes to display memory will take place as random cycles. — is 0, consecutive CPU writes to display memory are executed as Fast-page Mode writes, whenever possible.
5	**CRT FIFO Depth Control:** When this bit is 0 (the default): • The CRT write buffer depth is set to 8 levels (32 bits/level). • This setting is typically used for standard video modes and for extended 16-color modes When this bit is 1: • The CRT write buffer depth is set to 16 levels (64 bytes). • This setting is typically used for any 16-bit or 24-bit pixel modes and for extended 8-bit pixel modes. This setting should never be used for any text mode.

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6.7.6 SRF: DRAM Control Register *(cont.)*

Bit **Description**

4:3 **Display Memory Data Bus Width [1:0]:**
This two-bit field is used with SRF[7] to specify the display memory data bus width according to the following table:

SRF			Display Memory Data Bus Width	Memory Organization	Total Memory
[7]	[4]	[3]			
0	0	0	—	Reserved	Reserved
0	0	1	—	Reserved	Reserved
0	1	0	32 Bit	Two 256K x 16 DRAMs	1 MByte
				Four 512K x 8 (symmetric) DRAMs	2 MBytes
0	1	1	—	Reserved	Reserved
1	1	0	32 Bit	Four 256K x 16 DRAMs (two banks)	2 MBytes
111			—	Reserved	Reserved

These bits have one level of buffering. At the end of each horizontal scanline refresh interval, when horizontal blanking begins, the state of each of these bits is transferred to the timing logic. This transfer avoids changing the timing logic in mid-scanline.

2 **DRAM RAS Timing:**
This bit indicates the DRAM row-address strobe timing as summarized in the following table.

SRF[2]	Timing for RAS high	Timing for RAS low	Note
0	3 MCLK	4 MCLK	Extended RAS (default)
1	2.5 MCLK	3.5 MCLK	Standard RAS

The default is extended RAS timing, which fits all DRAMs. However, in order to achieve optimal performance, the timing selected should match the MCLK.

1 Reserved

0 **Multiple-CAS# / Multiple-WE# DRAM Select:**
- A 0 selects multiple-WE# 256 x 16-bit DRAM support.
- A 1 selects multiple-CAS# DRAM support, which is the default.

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6.7.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Reset State
7	HW Cursor and HW Icon Coarse Horizontal Position [10]	0
6	HW Cursor and HW Icon Coarse Horizontal Position [9]	0
5	HW Cursor and HW Icon Coarse Horizontal Position [8]	0
4	HW Cursor and HW Icon Coarse Horizontal Position [7]	0
3	HW Cursor and HW Icon Coarse Horizontal Position [6]	0
2	HW Cursor and HW Icon Coarse Horizontal Position [5]	0
1	HW Cursor and HW Icon Coarse Horizontal Position [4]	0
0	HW Cursor and HW Icon Coarse Horizontal Position [3]	0

This register, and bits SRX[7:5] of the index that is used to access it, is used to define in character clocks the coarse horizontal (X) pixel offset of the graphics hardware cursor and icon. For more information on the hardware cursor and icon, refer to Appendices A2 and A3.

For all 8-bit text modes and non-expanded graphics modes and text modes which do not require the fourth expansion bit, the entire 12-bit cursor or icon horizontal position can be written in a single 16-bit I/O write as follows:

- The expansion bits in SR2A[6] and SR2E[0], which are cleared to 0, are ignored.
- The offset must be placed in AX[15:5].
- AX[4:0] must be 10000.
- DX must be 3C4h.

When 10, 30, 50...F0 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the previously stored three bits of the cursor or icon position.

Note: Changes programmed in SR10 do not take effect until SR11 has been written.

Bit	Description
7 0	**Cursor and Icon Horizontal Position [10:3]:** SR12[3] selects whether the value in this register refers to the hardware cursor or the hardware icon. Cursor 12-bit Horizontal Position • When SR12[3] = 0, the hardware cursor is selected. • SR10[7:0] are the upper 8 coarse-position bits. • SRX[7:5] are the lower 3 fine-position bits, defined in dot clocks. • SR2E[0] extends the cursor fine position by one msb for horizontally expanded graphics modes. This extra bit is valid only with a 10-dot character clock. • The hardware cursor is not available in text modes and mode 13.

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6.7.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position *(cont.)*

Bit	Description
7:0*(cont.)*	**Cursor and Icon Horizontal Position [10:3]:**

Icon 12-bit Horizontal Position

- When SR12[3] = 1, the hardware icon is selected.
- SR10[7:0] form the upper-eight bits of the 11-bit icon horizontal offset.
- SRX[7:5] form the lower-three bits of the 11-bit icon horizontal offset.
- SR2A[6] is the fourth bit of a dot-clock-level delay in expanded-graphics modes and in text modes with 9-dot or 10-dot fonts.
- The icon is supported in all modes, except interlaced, 24 bpp with 3X clock, and 16 bpp with 2X clock. (The latter does not support horizontal doubling.)

To program the horizontal position of the hardware icon:

- Place the icon hot point (top left) at pixel n (with 0 as the first pixel).
- Program the coarse position as: Integer [(n ÷ (k-1)) ÷ k].
  (k = the number of dots in a character clock.)
- Program the fine position as: Remainder [(n ÷ (k-1)) ÷ k].

For example, to place the icon:

- at pixel 10, which is 11 pixels from the left (n = 10)
- with an 8-dot character clock, as in graphics mode 12 (k = 8)

Program:

- the coarse position as = Integer [(10 ÷ (8 - 1)) ÷ 8] = Integer [17 ÷ 8] = 2h
- the fine position as = Remainder [17 ÷ 8] = 1h

An example of programming for an 8-dot character clock is given in the table below.

Pixel Position	Position Programmed	
	Coarse.	Fine
0	0	7
1	1	0
2	1	1
3	1	2
4	1	3
5	1	4
6	1	5
7	31	6
8	1	7
9		0
10	2	1

There are only three cases of character clock width.

- 10 dots – used for text and graphics expansion on 800 x 600 LCD
- 9 dots – used for text on 800 x 600 LCDs, when 720 dots are displayed
- 8 dots – used in all other cases

6.7.8 SR11: Hardware Cursor and Hardware Icon Coarse Vertical Position

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Reset State
7	HW Cursor and HW Icon Coarse Vertical Position [10]	0
6	HW Cursor and HW Icon Coarse Vertical Position [9]	0
5	HW Cursor and HW Icon Coarse Vertical Position [8]	0
4	HW Cursor and HW Icon Coarse Vertical Position [7]	0
3	HW Cursor and HW Icon Coarse Vertical Position [6]	0
2	HW Cursor and HW Icon Coarse Vertical Position [5]	0
1	HW Cursor and HW Icon Coarse Vertical Position [4]	0
0	HW Cursor and HW Icon Coarse Vertical Position [3]	0

This register, and bits SRX[7:5] of the index that is used to access it, is used to define in scanlines the coarse vertical (Y) scanline offset of the graphics hardware cursor and icon. For more information on the hardware cursor and icon, refer to Appendices A2 and A3.

The entire 11-bit cursor or icon vertical position can be written in a single 16-bit I/O write as follows:

- The offset must be placed in AX[15:5].
- AX[4:0] must be 10001.
- DX must be 03C4.

When 10, 30, 50...F1 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the previously stored three bits of the cursor or icon position.

Bit	Description
7:0	**Cursor and Icon Vertical Position [10:3]:** SR12[3] selects whether the value in this register refers to the hardware cursor or the hardware icon. Cursor and Icon 11-bit Vertical Position • When SR12[3]: — is 0, the hardware cursor is selected. — is 1, the hardware icon is selected. • SR11[7:0] are the upper 8 coarse-position bits. • SRX[7:5] are the lower 3 fine-position bits, defined in scanlines

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6.7.9 SR12: Video Data Path Control Register

I/O Port Address: 3C5

Index: 12

Bit	Description	Reset State
7	Overscan Color Protect	0
6	Tri-State All Display Memory Pins	0
5	VCLK = VCO ÷ 4	0
4	MCLK = MVCO ÷ 2	0
3	Hardware Icon and Hardware Cursor Position Modification	0
2	Cursor Pixel Size Select	0
1	CPU Access to DAC Extended Colors	0
0	Graphics Hardware Cursor Enable	0

This register is used to enable or disable 4-bit packed-pixel addressing on the CL-GD7542.

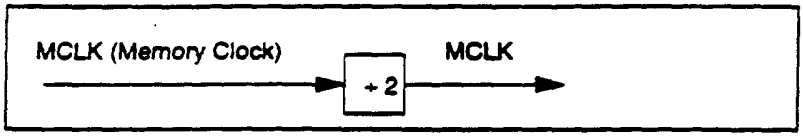
Bit	Description
7	**Overscan Color Protect:** When this bit: • is 1, the overscan color comes from the hidden DAC register (the 16-cell RAMDAC RAM extension.) As a result, the border color is locked to a value dictated by the enviromental requirements, and it cannot be changed by the application. • is 0, the overscan color comes from AR11[5:0].
6	**Tri-State All Display Memory Pins:** • When this bit is 0, all display memory pins operate normally. • When this bit is 1, all display memory pins are forced to a tri-stated high-impedance off state. The display memory pins can then be multiplexed for use with another graphics controller.
5	**VCLK = VCO ÷ 4:** When this bit is 1, the video clock (VCLK) signal is derived from the voltage-controlled oscillator (VCO) frequency divided by four. • This bit must be used to get VCLK frequencies of 20MHz or less. For example, to get 20 MHz: — Program VCO for 80 MHz. — Set SR12[5] = 1, which divides the VCO signal by four. — As a result, VCLK = 20 MHz. • This bit is useful in 5V Core-VDD systems where at low frequencies, the VCO frequency range is not good enough. (Note that SR1B through SR1E[0] is VCLK divided by two). While the VCO is within its operating range, as appropriate for the desired VCLK frequency, divide by 2 or by 4.

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6.7.9 SR12: Video Data Path Control Register *(cont.)*

Bit	Description
4	**MCLK = MCLK ÷ 2:** When this bit: • is 1, the memory clock (MCLK) signal is derived by dividing by two the original memory clock signal (which is the MVCO, the memory voltage-controlled oscillator).  • is 0, the memory clock is not divided by 2. In this case, the clock that is used as the memory clock is the same frequency as the MVCO.  • This bit may is used to get MCLK frequencies outside the memory VCO frequency range for a given Core VDD value and frequency.
3	**Hardware Icon and Hardware Cursor Position Modification:** This bit selects whether the CPU can modify the position (both horizontal and vertical) of either the hardware icon or the hardware cursor. The same registers are used to modify both hardware icon and hardware cursor position. • When this bit is 0, the CPU can modify the hardware cursor position. • When this bit is 1, the CPU can modify the hardware icon position. • This bit does not affect SR2A[6] or SR2E[0], which are always accessible by the CPU.
2	**Cursor Pixel Size Select:** • When this bit is 0, the 32 x 32 pixel hardware cursor is selected. • When this bit is 1, the 64 x 64 pixel hardware cursor is selected.
1	**CPU Access to DAC Extended Colors:** • When this bit is 0, the CPU accesses the standard VGA 256 x 18 Color Lookup Table. • When this bit is 1, the CPU accesses the DAC extended colors, which are 16 additional 18-bit wide RAMDAC RAM locations. — Some locations have a specific purpose, such as hardware cursor colors (2 locations), hardware icon colors (4 locations), and border color (1 location). — Other locations are not used, or can be used as scratch registers by the BIOS and drivers.

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6.7.9 SR12: Video Data Path Control Register *(cont.)*

Bit **Description**

1 *(cont.)* **CPU Access to DAC Extended Colors (cont.):**
The address map for the DAC extended colors is given in the following table:

I/O Address	Physical RAM Location	Function
X0h	256	Hardware cursor back-ground color
XFh	257	Hardware cursor foreground color
X2h	258	Fix color of overscan (the border)
X3h	259	Hardware icon color #0. (This function is not used, if in 3 colors + transparent mode.)
X4h	260	Hardware icon color #1
X5h	261	Hardware icon color #2
X6h	262	Hardware icon color #3
XD, XE	269, 270	Used by Video BIOS

0 **Graphics Hardware Cursor Enable:**
When this bit is 1, the graphics hardware cursor is enabled.

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6.7.10 SR13: Graphics Cursor Pattern Address Offset Register

I/O Port Address: 3C5

Index: 13

Bit	Description	Reset State
7	Not Used	
6	Not Used	
5	Reserved	
4	Cursor Pattern Select [4]	0
3	Cursor Pattern Select [3]	0
2	Cursor Pattern Select [2]	0
1	Cursor Pattern Select [1] / Reserved	0
0	Cursor Pattern Select [0] / Reserved	0

This register is used to select:

- one of 32 possible cursor patterns for the 32 x 32 cursor
- one of 8 possible cursor patterns for the 64 x 64 cursor

For a complete programming guide for the graphics hardware cursor, refer to Appendix A2.

Bit	Description
7.6	Not Used
5	Reserved
4.0	**Cursor Pattern Select (32 x 32 Cursor):** When SR12[2] is 0 • This 5-bit field can select 1 of 32 cursor patterns for the 32 x 32 cursor. • The patterns are stored in 8 Kbytes of the top 32 Kbytes of display memory.
4.2	**Cursor Pattern Select (64 x 64 Cursor):** When SR12[2] is 1 • This 3-bit field can select 1 of 8 cursor patterns for the 64 x 64 cursor. • The patterns are stored in 8 Kbytes of the top 32 Kbytes of display memory.
1.0	Reserved, when SR12[2] = 1.

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6.7.11 SR14, SR15: Scratch Pad 2, 3 Registers

I/O Port Address: 3C5

Index:14, 15

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD7542 BIOS and must never be written by any application program. They are listed here only for completeness.

Bit	Description
7:0	These bits are reserved for the Cirrus Logic, Inc., BIOS.

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CL 28642

6.7.12 SR16: Performance Tuning Register

I/O Port Address: 3C5

Index:16

Bit	Description	Reset State
7	Extra Wait State for Fast VL Bus	1
6	RDY# Delay for I/O	1
5	RDY# Delay for Memory Write [1]	1
4	RDY# Delay for Memory Write [0]	1
3	FIFO Demand Threshold [3]	0
2	FIFO Demand Threshold [2]	0
1	FIFO Demand Threshold [1]	0
0	FIFO Demand Threshold [0]	0

This register is used to control the delay from ADS# to RDY#, and to control the threshold at which the CRT FIFO will be refilled. This register must never be written by an application program. It is listed here for completeness only.

Bit **Description**

7 **Extra Wait State for Fast VL Bus:**

- When this bit is 1, and when the CL-GD7542 is configured for the VL bus, one extra wait state is added to both I/O and memory accesses.
- This bit must be 1 if the bus clock is fast, compared to the memory clock.
- In conjunction with the state of SR16[6], this bit controls the CPU1X clock delay from ADS# to RDY# for I/O cycles.
- For further explanation, refer to the tables in SR16[6] and SR16[5:4].

6 **RDY# Delay for I/O:**

- This field applies only when the CL-GD7542 is configured for local bus.
- In conjunction with the state of SR16[7], this bit controls the CPU1X clock delay from ADS# to RDY# for read/write I/O cycles.
- The following table summarizes the values:

SR16		CPU1X Clock Delay
[7]	[6]	
0	0	1
0	1	2
1	0	2
1	1	3 (Default)

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6.7.12 SR16: Performance Tuning Register *(cont.)*

Bit **Description**

5:4 **RDY# Delay for Memory Write [1:0]:**

- This field is used to control the delay from ADS# to RDY# for memory write cycles.
- This field applies only when the CL-GD7542 is configured for local bus.
- The table below summarizes values that may be programmed into this field. The value programmed must satisfy the following inequality:
  [(2 + value of bits 7,5,4) x CPU Clock Period] ≥ [(3 x MCLK Period) + 2 ns]

SR16			CPU1X Clock Delay
[7]	[5]	[4]	
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	3
1	0	1	4
1	1	0	5
1	1	1	6 (Default)

3.0 **FIFO Demand Threshold [3:0]:**

- The value written to this field will select the level at which the CL-GD7542 sequencer will begin cycles to refill the CRT FIFO (and thereby hold off CPU cycles).
- For each video mode and MCLK frequency, there will be an optimum value that will use the DRAM most efficiently.

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CL 28644

6.7.13 SR18: Signature Generator Control Register

I/O Port Address: 3C5

Index:18

Bit	Description	Reset State
7	LCD Signature Generator Enable	0
6	Reserved	
5	Reserved	
4	Pixel Bus Bit Select [2]	0
3	Pixel Bus Bit Select [1]	0
2	Pixel Bus Bit Select [0]	0
1	Reset Signature Generator	0
0	Signature Generator Enable / Status	0

This register is used to control and monitor the status of the CL-GD7542 signature generator, which is used for board-level testing of the video sub-system. For a complete description of the signature generator, refer to Appendix A10.

Bit	Description
7	**LCD Signature Generator Enable:** When this bit is 1, the LCD signature generator is enabled.
6	Reserved
5	Reserved
4:2	**Pixel Bus Bit Select [2:0]:** This field is used to select the Feature Connector Pixel Bus bit that will be used as the input for the signature generator according to the following table:

SR18			Feature Connector Pixel Bus Bit
[4]	[3]	[2]	
0	0	0	FCP[0]
0	0	1	FCP[1]
0	1	0	FCP[2]
0	1	1	FCP[3]
1	0	0	FCP[4]
1	0	1	FCP[5]
1	1	0	FCP[6]
1	1	1	FCP[7]

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6.7.13 SR18: Signature Generator Control Register *(cont.)*

Bit	Description
1	**Reset Signature Generator:** • When this bit is 1, the signature generator is reset to an initial, defined condition. • When this bit is 0, the signature generator is allowed to run under the control of SR18[0].
0	**Signature Generator Enable / Status:** • When this bit is 1, the signature generator is enabled and begins operation on the next VSYNC. From the Feature Connector Pixel Bus bit chosen by SR18[4:2], the signature generator accumulates a signature for one video frame and then stops, forcing this bit to 0. • By monitoring the status of this bit, the program can determine when the signature is complete.

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6.7.14 SR19: Signature Generator Result Low Byte Register

I/O Port Address: 3C5

Index: 19

Bit	Description	Reset State
7	Signature Generator Result [7]	0
6	Signature Generator Result [6]	0
5	Signature Generator Result [5]	0
4	Signature Generator Result [4]	0
3	Signature Generator Result [3]	0
2	Signature Generator Result [2]	0
1	Signature Generator Result [1]	0
0	Signature Generator Result [0]	1

For a complete description of the signature generator, refer to Appendix A10.

Bit	Description
7:0	**Signature Generator Result [7:0]:** This register is used to read the low-order byte of the CL-GD7542 signature generator result.

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6.7.15 SR1A: Signature Generator Result High Byte Register

I/O Port Address: 3C5

Index: 1A

Bit	Description	Reset State
7	Signature Generator Result [15]	0
6	Signature Generator Result [14]	0
5	Signature Generator Result [13]	0
4	Signature Generator Result [12]	0
3	Signature Generator Result [11]	0
2	Signature Generator Result [10]	0
1	Signature Generator Result [9]	0
0	Signature Generator Result [8]	0

For a complete description of the signature generator, refer to Appendix A10.

Bit	Description
7:0	**Signature Generator Result [15:8]:** This register is used to read the high-order byte of the CL-GD7542 signature generator result.

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6.7.16 SR1B,SR1C,SR1D,SR1E: Denominator/Post-scalar for VCLK 0,1,2,3

I/O Port Address: 3C5

Index: 1B, 1C, 1D, 1E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	VCLK Denominator [4]	Note a
4	VCLK Denominator [3]	Note a
3	VCLK Denominator [2]	Note a
2	VCLK Denominator [1]	Note a
1	VCLK Denominator [0]	Note a
0	VCLK Post-Scalar	Note a

Note a. The reset values for the VCLK Numerator for these four registers are shown in Table 6–2, "VCLK Numerator, Denominator, and Post-scalar Values," on page 207.

These registers, in conjunction with SRB, SRC, SRD, and SRE, are used to determine the frequency of video clock 0 (VCLK0), etc. For complete programming information for the synthesizers, refer to Appendix A7.

Bit	Description
7:6	Reserved
5.1	**VCLK Denominator (D) [4:0]:** Refer to Table 6–2, "VCLK Numerator, Denominator, and Post-scalar Values," on page 207 for detailed explanation of the VCLK derivation.
0	**VCLK Post-Scalar (P):** Refer to Table 6–2, "VCLK Numerator, Denominator, and Post-scalar Values," on page 207 for detailed explanation of the VCLK derivation.

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6.7.17 SR1F: MCLK Frequency and VCLK Source Select Register

I/O Port Address: 3C5

Index: 1F

Bit	Description	Reset State
7	Not Used	
6	VCLK Source Select	0
5	MCLK Frequency [5]	(Refer to MCLK Table below)
4	MCLK Frequency [4]	(Refer to MCLK Table below)
3	MCLK Frequency [3]	(Refer to MCLK Table below)
2	MCLK Frequency [2]	(Refer to MCLK Table below)
1	MCLK Frequency [1]	(Refer to MCLK Table below)
0	MCLK Frequency [0]	(Refer to MCLK Table below)

This register is used to program the MCLK frequency. This register should never be programmed by an applications program. It is listed here only for completeness.

Bit 7 — Not Used.

Bit 6 — **VCLK Source Select:**

- When this bit is 0, the VCLK synthesizer operates normally.
- When this bit is 1, VCLK is derived from MCLK as follows:

SR1F[6]	SR1E[0]	VCLK Source
0	X	VLCK (Normal Operation)
1	0	VCLK = MCLK
1	1	VCLK = MCLK ÷ 2

Bits 5 0 — **MCLK Frequency [5:0]:**

- To directly program the MCLK frequency, use the following equation: MCLK = (Reference Frequency ÷ 8) x SR1F[5:0]
- This field may be programmed with values from 21 to 38 (decimal).
- The following table assumes a reference frequency of 14.31818 MHz.

SR1F[5:0] (Decimal)	SR1F[5:0] (Hex)	Resulting MCLK Frequency
21	15h	37.585 MHz
23	17h	41.165 MHz
24	**18h (default, at-reset value)**	**42.955 MHz**
25	19h	44.744 MHz
26	1Ah	46.534 MHz
28	1Ch	50.114 MHz

- For information on DRAM requirements for MCLK frequencies, refer to Appendix A6

6.7.18 SR20: Miscellaneous Control 2

I/O Port Address: 3C5

Index: 20

Bit	Description	Reset State
7(MSB)	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	DRAM Interface-Input Threshold Select	0
0(LSB)	CPU Bus Interface-Input Threshold Select	0

This register is reserved exclusively for the CL-GD7542 BIOS and must never be written by an application program. It is listed here only for completeness.

Bit	Description
7:2	Reserved
1	**DRAM Interface-Input Threshold Select:** • When this bit is 0, DRAM interface-input thresholds are at TTL levels. • When this bit is 1, DRAM interface-input thresholds are at CMOS levels.
0	**CPU Bus Interface-Input Threshold Select:** • When this bit is 0, CPU bus interface-input thresholds are at TTL levels. • When this bit is 1, CPU bus interface-input thresholds are at CMOS levels.

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6.7.19 SR21: Dual-Scan Color Control

I/O Port Address: 3C5

Index: 21

Bit	Description	Reset State
7(MSB)	Refresh Per Line Select	0
6	Dual-Scan STN Color STN Select	0
5	Reserved	
4	Graphics Hardware Cursor-Size Select	0
3	Reserved	
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

The SR21[7,6,4] bits are user programmable for the CL-GD7542. The SR21[3:0] bits are reserved for manufacturing testing and must never be written by an application program.

Bit	Description
7	**Refresh Per Line Select:** • When this bit is 1, one refresh cycle per scanline is selected. • When this bit is 0 (the default), CR11[6] selects either three or five refresh cycles per scanline.
6	**Dual-Scan STN Color Select:** CR2C[7:6] must be programmed to 10 to select STN color LCDs. When CR2C[7:6] = 10 and this bit: • = 1, dual-scan STN color mode is selected. • = 0, single-scan STN color mode is selected.
5	Reserved
4	**Graphics Hardware Cursor-Size Select:** When SR12[0] is 1 and: • this bit is 1, the 64 x 64-bit hardware cursor is selected. • this bit is 0, the 32 x 32-bit hardware cursor is selected. For hardware cursor pattern choices, refer to SR13[4:0].
3 0	Reserved for testing only.

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6.7.20 SR22: Hardware Configuration Read Register 1

I/O Port Address: 3C5

Index: 22

Bit	Description	Access	Reset State
7	PCI Minimum Grant	R	= MD[23]
6	Reserved	R	
5	Sleep Address Select	R	= MD[21]
4	Reserved		
3	External Clock Select	R	= MD[19]
2	Select VESA Local Bus > 33MHz	R	= MD[18]
1	Reserved		
0	Select 32-Bit PCI Bus	R	= MD[16]

This register contains a read-only field that allows the BIOS to determine configuration information for bus type, sleep address, and external clock by reading the level on the indicated MD pins during the low-to-high transition of the Reset pulse.

- All these MD pins have pull-down resistors internally, and so the default readings are all 0.
- An external 60 k-ohm pull-up resistor is needed to establish a high (1) on these pins.

Bus-select bits SR22[7,2,0] are mutually exclusive. Only *one* can be high at any time.

- If there are no external pull-ups on SR22 bus-select bits 7, 2, and 0, the CL-GD7542 will be configured for VESA local bus operation ≤ 33MHz.
- If there are no external pull-ups on *any* of the SR22 bus-select bits, the CL-GD7542 will be configured for VESA local bus operation ≤ 33MHz. In addition, the CL-GD7542 will be configured with internal clock synthesizers and a sleep address of 3C3h.

Bit	Description
7	**PCI Minimum Grant:** • An external pull-up on PCI-MGE / MD[23] reads back a 1. In this case: — The PCI burst cycle to the CL-GD7542 must be a minimum of 16 CPU clock cycles — PCI Configuration Register 3Ch, offset 2 will read back a 1, allowing the PCI core logic to detect the presence of the pull-up resistor. — The CL-GD7542 expects a default minimum grant value of 8 bus clocks. — A pull-up should not be used on PCI / MD[16], as only one PCI bus external configuration pull-up should be used (either PCI-MGE or PCI). • No external pull-up on PCI-MGE / MD[23] reads back a 0. In this case: — The PCI burst cycle to the CL-GD7542 will be 8 CPU clock cycles. — PCI Configuration Register 3Ch, offset 2 will read back a 0. • Normally no pull-up is required on PCI-MGE / MD[23] .

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6.7.20 SR22: Hardware Configuration Read Register 1 *(cont.)*

Bit	Description
6	Reserved
5	**Sleep Address Select:** • An external pull-up on S46 / MD[21] reads back a 1, which selects I/O address 46E8h as the sleep address. • No external pull-up on S46 / MD[21] reads back a 0, indicating the selection of sleep address 3C3h, the default.
4	Reserved
3	**External Clock Select:** • An external pull-up on XCLK/ MD[19] reads back a 1, powering down the internal clock for MCLK and VCLK, and enabling the external XMCLK and XVCLK clock inputs. (This external pull-up is used for manufacturing test and for logic simulations by Cirrus Logic.) • No external pull-up on XCLK/ MD[19] reads back a 0, so that the internal clock MCLK and VCLK are used by default.
2	**Select VESA Local Bus > 33MHz:** • An external pull-up on FVL / MD[18] reads back a 1, selecting a fast VESA local bus operation at > 33MHz. • No external pull-up on FVL / MD[18] reads back a 0, selecting a VESA local bus operation ≤ 33MHz.
1	Reserved
0	**Select 32-bit PCI Bus:** • An external pull-up on PCI / MD[16] reads back a 1, configuring the CL-GD7542 for 32-bit PCI bus operation. • No external pull-up on PCI / MD[16] reads back a 0, configuring the CL-GD7542 for VESA local bus operation ≤ 33MHz.

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6.7.21 SR23: Software Configuration Register 1

I/O Port Address: 3C5

Index:23

Bit	Description	Reset State
7	Enable FCVCLK	0
6	ACTI / FCEVIDEO# / SBYI Select	0
5	BLI / SUSPI Select	0
4	VCLK Output Enable	0
3	Reserved	0
2	48-KByte BIOS Decode Select	0
1	Reserved	
0	Reserved	

This register contains a read-only field that allows for miscellaneous configurations.

Bit	Description
7	**Enable FCVCLK:** A 1 in this bit enables the FCVCLK input to drive either the RAMDAC or the video clock (VCLK), depending on the state of External/General Register MISC[3]. When SR23[7] = 1: • *and* MISC[3] = 0, FCVCLK is sent only to the RAMDAC, enabling only that part of the CL-GD7542. • *and* MISC[3] = 1, FCVCLK is used for to drive VCLK, which clocks the entire CL-GD7542. • *and* there is a high on TVON, the TVON high signal forces MISC[3] to 1. In this case also, FCVCLK is used to drive VCLK, which clocks the entire CL-GD7542.
6	**ACTI / FCEVIDEO# / SBYI Select:** When SR24[7] = 0: • *and* this bit is 0, the ACTI / FCEVIDEO# / SBYI pin is configured as the hardware-controlled Standby input. • *and* this bit is 1, the ACTI / FCEVIDEO# / SBYI pin is configured as the Activity sense input to reset the power-down timers. When SR24[7] = 1: • the ACTI / FCEVIDEO# / SBYI pin is always FCEVIDEO#, independent of the SR23[6] value.
5	**BLI / SUSPI Select:** When this bit: • is 0, the BLI / SUSPI pin is configured for hardware-controlled Suspend input. • is 1, and SR24[7] = 0, the BLI / SUSPI pin is configured for Backlight input control.

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6.7.21 SR23: Software Configuration Register 1 *(cont.)*

Bit	Description
4	**VCLK Output Enable:** • When this bit is 0 (the default), the VCLK output is low. • When this bit is 1, the internal VCLK is available for testing on the VCLK / FCDCLK pin, independent of SR22[3] (the external/internal clock selection). Note: When SR24[7] = 1, the internal VCLK is also available on the FCDCLK output.
3	Reserved
2	**48-KByte BIOS Decode Select:** When BIOS is enabled: • A 0 in this bit selects 32-KByte BIOS decode. • A 1 in this bit selects 48-KByte BIOS decode.
1:0	Reserved

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6.7.22 SR24: LCD Type Switches and FC Enable

I/O Port Address: 3C5

Index:24

Bit	Description	Reset State
7	Feature Connector External Pull-up Video Port Enable	FC Pull-up
6	Reserved	
5	Fast 16-Bit CPU Bus Access Enable	0
4	FCDCLK Output Select	0
3	External Pull-Up Read under Software Control	0
2	SW2 Pin Read	Switch Value
1	SW1 Pin Read	Switch Value
0	SW0 Pin Read	Switch Value

Bit	Description
7	**Feature Connector External Pull-up Video Port Enable:** • An external pull-up resistor on FC / MD25 configures all appropriate pins for the Feature Connector Video Port. (Refer to pin descriptions in Chapter 2.) • When no pull-up is used, these pins revert to their other functions or are disabled (that is, inputs are ignored and outputs are high impedance).
6	Reserved
5	**Fast 16-Bit CPU Bus Access Enable:** • When this bit is 0, the RDY# / TRDY# output is delayed for 16-bit accesses by one bus-clock cycle to minimize bus contention problems. • When this bit is 1, the clock delay is removed, which allows faster bus access. This bit works with both the VESA local bus and the PCI bus.
4	**FCDCLK Output Select:** This bit is used to select the clock that appears on the FCDCLK pin. • When this bit is 1: — The selection is the VCLK VCO output clock. — Even if SR23[7] = 1, the internal VCLK clock synthesizer outputs the internal clock to the VCLK output pin. This configuration is used with the Feature Connector for video overlay. • When this bit is 0, the selection is PCLKO, which is a dot clock that SR1[3] does *not* divide by 2.
3	**External Pull-Up Read Under Software Control:** • This bit is used to restore operation: — when total graphics controller power-off is used. — when the Reset pulse is too short to read the switches which have large pull-up or pull-down resistance. • This bit is programmed first to a 1 then to a 0. Configuration inputs are read on the 1-to-0 transition of this bit. By toggling this bit, configuration pins can be read and latched at any time, not just at Reset.

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6.7.22 SR24: LCD Type Switches and FC Enable *(cont.)*

Bit	Description
2:0	**SW2 to SW0 Pin Read:** These read-only bits reflect the active level of switch inputs SW2 to SW0. • These bits are read continuously during normal operation, and are not affected by SR24[3]. • These bits are normally for BIOS use.

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6.7.23 SR25: Timer-Software Reset and Hardware Configuration #2

I/O Port Address: 3C5

Index:25

Bit	Description	Reset State
7	Reserved	
6	External RAMDAC Address / Chip Select	0
5	Enable 1-bit/pixel Packed-Pixel Mode	0
4	Enable External XVCLK Input	0
3	Enable 4-bit/pixel Packed-Pixel Mode	0
2	Reserved	
1	Reset Standby Timer	0
0	Reset Backlight Timer	0

Bit	Description
7	Reserved
6	**External RAMDAC Address / Chip Select:** • When this bit is 0, the TVON pin is controlled by Extension Register CR30[3]. • When this bit is 1: — The TVON output becomes the external RAMDAC Chip Select. At system reset, both the TVON and RAMDAC Select functions are inactive low. As a result, no matter how the chip comes up, external RAMDAC is not affected. — It disables the internal DAC and RAMDAC RAM I/O readback. The RAM continues to be updated by RAMDAC writes, but it does not respond to any RAMDAC read except 3C7. — In VL bus mode, the CL-GD7542 does not assert LDEV# and RDY. — In PCI bus mode, the CL-GD7542 does not support external RAMDAC related to I/O select or shadowing. • This bit must be set to 1, *before* TV-OUT feature is enabled (CR30[3] = 1), to ensure that the TVON pin becomes the external RAMDAC Chip Select.
5	**Enable 1-bit/pixel Packed-Pixel Mode:** When this bit is 1, the 1-bit-per-pixel packed-pixel mode is enabled.
4	**Enable External XVCLK Input:** When this bit is 1, and when SR22[3] is 0, an external 14.31818 input must be connected to the OSC / XVCLK input pin. (However, MCLK will not use this input. Instead, it will still use the internal MVCO source.) • On VCLK generation, this bit is OR'ed with SR22[3]. • This bit is to be used for NTSC-Out.
3	**Enable 4-bit/pixel Packed-Pixel Mode:** When this bit is 1, 4-bit-per-pixel packed-pixel mode is enabled.

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6.7.23 SR25: Timer-Software Reset and Hardware Configuration #2 *(cont.)*

Bit	Description
2	Reserved
1	**Reset Standby Timer:** This bit is used to reset the internal Standby Mode Timer, when there is an I/O read to the keyboard controller (port 60h).
0	**Reset Backlight Timer:** This bit is used to reset the internal Backlight Timer, when there is an I/O read to the keyboard controller (port 60h).

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6.7.24 SR26: Shader Signature — Least-Significant Byte

I/O Port Address: 3C5

Index:26

Bit	Description	Reset State
7	Shader Signature [7]	0
6	Shader Signature [6]	0
5	Shader Signature [5]	0
4	Shader Signature [4]	0
3	Shader Signature [3]	0
2	Shader Signature [2]	0
1	Shader Signature [1]	0
0	Shader Signature [0]	0

The Shader Signature field is used for factory testing only. Application programs should not use the Shader Signature registers, which are listed here only for completeness.

Bit	Description
7:0	**Shader Signature [7:0]:** This register contains the least-significant byte for the Shader Signature. For the most-significant byte, refer to SR27. The Shader Signature field is used for testing the CL-GD7542 shader logic.

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6.7.25 SR27: Shader Signature — Most-Significant Byte

I/O Port Address: 3C5

Index:27

Bit	Description	Reset State
7	Shader Signature [15]	0
6	Shader Signature [14]	0
5	Shader Signature [13]	0
4	Shader Signature [12]	0
3	Shader Signature [11]	0
2	Shader Signature [10]	0
1	Shader Signature [9]	0
0	Shader Signature [8]	0

The Shader Signature field is used for factory testing only. Application programs should not use the Shader Signature registers, which are listed here only for completeness.

Bit	Description
7:0	**Shader Signature [15:8]:** This register contains the most-significant byte for the Shader Signature. For the most-significant byte, refer to SR26. The Shader Signature field is used for testing the CL-GD7542 shader logic.

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6.7.26 SR2A: Hardware Icon #0 Control Register

I/O Port Address: 3C5

Index:2A

Bit	Description	Reset State
7	Reserved	
6	Icon Horizontal Fine-Position msb[3]	0
5	Memory Map Selection for Hardware Icon #0	0
4	Vertical Scanline Doubling for Hardware Icon #0	0
3	Horizontal Pixel Doubling for Hardware Icon #0	0
2	Blink Enable for Hardware Icon #0	0
1	Display Mode Select for Hardware Icon #0	0
0	Display Enable for Hardware Icon #0	0

Bit	Description
7	Reserved
6	**Icon Horizontal Fine-Position msb[3]:** The least-significant bits[2:0] are in register SRX[7:5]. This 4-bit word is used with 9-dot and 10-dot fonts (character clocks), when in text or horizontally-expanded graphics. The coarse horizontal position is SR10. Note: When horizontal expansion from 640 to 800 is enabled, the hardware cursor must be positioned within 10 dots.
5	**Memory Map Selection for Icon #0:** • A 0 in this bit selects map 0. • A 1 in this bit selects map 1.
4	**Vertical Scanline Doubling for Icon #0:** When this bit is 1: • Icon #0 displays 128 scanlines, but each scanline is replicated vertically. • Icon #0 extends down and forces all other icons down.
3	**Horizontal Pixel Doubling for Icon #0:** When this bit is 1: • Icon #0 displays 128 pixels, but each pixel is replicated horizontally. • Icon #0 expands to the right on the display.
2	**Blink Enable for Icon #0:** • When this bit is 1, icon #0 blinks at one-half the text-cursor blink rate. • When this bit is 0, icon #0 is steady state.
1	**Display Mode Select for Icon #0:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • A 0 in this bit selects the four-color display mode for icon #0. • A 1 in this bit selects the three-colors-and-transparent display mode.
0	**Display Enable for Icon #0:** When this bit is 1, it enables icon #0 to display.

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6.7.27 SR2B: Hardware Icon #1 Control Register

I/O Port Address: 3C5

Index:2B

Bit	Description	Reset State
7	High Drive on FPVDCLK and LLCLK	0
6	Monitor Sense Assist Bit	0
5	Memory Map Selection for Hardware Icon #1	0
4	Vertical Scanline Doubling for Hardware Icon #1	0
3	Horizontal Pixel Doubling for Hardware Icon #1	0
2	Blink Enable for Hardware Icon #1	0
1	Display Mode Select for Hardware Icon #1	0
0	Display Enable for Hardware Icon #1	0

Bit	Description
7	**High Drive on FPVDCLK and LLCLK:** When this bit is 1, FPVDCLK and LLCLK have double the normal output drive to support high-load LCDs.
6	**Monitor Sense Assist Bit:** When this bit is 1: • It disables the internal BLANK# signal to the DAC, thus allowing border color during the entire non-display time. • *and* ARX[5] = 0, this bit can be used to force a monitor display for accurate monitor sense, independent of the following: — CPU speed — CPU interrupts — the video mode
5	**Memory Map Selection for Icon #1:** • A 0 in this bit selects map 0. • A 1 in this bit selects map 1.
4	**Vertical Scanline Doubling for Icon #1:** When this bit is 1: • Icon #1 displays 128 scanlines, but each scanline is replicated vertically. • Icon #1 extends down and forces all other icons down.
3	**Horizontal Pixel Doubling for Icon #1:** When this bit is 1: • Icon #1 displays 128 pixels, but each pixel is replicated horizontally. • Icon #1 expands to the right on the display.

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6.7.27 SR2B: Hardware Icon #1 Control Register *(cont.)*

Bit	Description
2	**Blink Enable for Icon #1:** • When this bit is 1, the icon blinks at one-half the text-cursor blink rate. • When this bit is 0, the icon is steady state.
1	**Display Mode Select for Icon #1:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • A 0 in this bit selects the four-color display mode for icon #1. • A 1 in this bit selects the three-colors-and-transparent display mode.
0	**Display Enable for Icon #1:** When this bit is 1, it enables icon #1 to display.

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6.7.28 SR2C: Hardware Icon #2 Control and Miscellaneous PCI Register

I/O Port Address: 3C5

Index:2C

Bit	Description	Reset State
7	Enable PCI Base Register 14h [31:24]	0
6	Byte-swap for PCI Base Register 14h [31:24]	0
5	Memory Map Selection for Icon #2	0
4	Vertical Scanline Doubling for Icon #2	0
3	Horizontal Pixel Doubling for Icon #2	0
2	Blink Enable for Icon #2	0
1	Display Mode Select for Icon #2	0
0	Display Enable for Icon #2	0

Bit	Description
7	**Enable PCI Base Register 14h:** • When this bit is 1, and the CL-GD7542 is in PCI bus mode, base register 14h [31:24] is decoded as a valid address range. • When this bit is 0, this address range is ignored.
6	**Byte-swap for PCI Base Register 14h:** When this bit is 1, and the CL-GD7542 is in PCI bus mode: • Byte swapping is enabled for the base register 14h[31:24] address range. • Byte[0] is swapped with byte[1], and byte[2] is swapped with byte[3].
5	**Memory Map Selection for Icon #2:** • A 0 in this bit selects map 0. • A 1 in this bit selects map 1.
4	**Vertical Scanline Doubling for Icon #2:** When this bit is 1: • Icon #2 displays 128 scanlines, but each scanline is replicated vertically. • Icon #2 extends down and forces all other icons down.
3	**Horizontal Pixel Doubling for Icon #2:** When this bit is 1 • Icon #2 displays 128 pixels, but each pixel is replicated horizontally. • Icon #2 expands to the right on the display.
2	**Blink Enable for Icon #2:** • When this bit is 1, icon #2 blinks at one-half the text-cursor blink rate. • When this bit is 0, icon #2 is steady state.
1	**Display Mode Select for Icon #2:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • A 0 in this bit selects the four-color display mode for icon #2. • A 1 in this bit selects the three-colors-and-transparent display mode.
0	**Display Enable for Icon #2:** When this bit is 1, it enables icon #2 to display.

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6.7.29 SR2D: Hardware Icon #3 Control and HIMEM Select Register

I/O Port Address: 3C5

Index:2D

Bit	Description	Reset State
7	HIMEM[1] Reference Bit	0
6	HIMEM[0] Reference Bit	0
5	Memory Map Selection for Icon #3	0
4	Vertical Scanline Doubling for Icon #3	0
3	Horizontal Pixel Doubling for Icon #3	0
2	Blink Enable for Icon #3	0
1	Display Mode Select for Icon #3	0
0	Display Enable for Icon #3	0

Bit	Description
7:6	**HIMEM[1:0] Reference Bits:** These bits are extensions of memory segment select bits in register SR7[7:4]. The CL-GD7542 compares the value in these bits with the levels on the HIMEM[1:0] pins to define the valid upper-address space. • In VESA local bus operations, when HIMEM[1:0] = SR2D[7:6] and A[23:20] = SR7[7:4], the CL-GD7542 identifies the upper address as its CPU address-mapped area. • In PCI bus operations, when these two bits are non-zero, the chip is in linear memory mode. When SR2D[7:6] or SR7[7:4] are not zero, the PCI memory map is defined by base registers 10 or 14 (upper bytes). • For segmented addressing mode, these bits must be 0.
5	**Memory Map Selection for Icon #3:** • A 0 in this bit selects map 0. • A 1 in this bit selects map 1.
4	**Vertical Scanline Doubling for Icon #3:** When this bit is 1: • Icon #3 displays 128 scanlines, but each scanline is replicated vertically. • Icon #3 extends down and forces all other icons down.
3	**Horizontal Pixel Doubling for Icon #3:** When this bit is 1: • Icon #3 displays 128 pixels, but each pixel is replicated horizontally. • Icon #3 expands to the right on the display.
2	**Blink Enable for Icon #3:** • When this bit is 1, icon #3 blinks at one-half the text-cursor blink rate. • When this bit is 0, icon #3 is steady state.

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6.7.29 SR2D: Hardware Icon #3 Control and HIMEM Select Register *(cont.)*

Bit	Description
1	**Display Mode Select for Icon #3:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • A 0 in this bit selects the four-color display mode for icon #3. • A 1 in this bit selects the three-colors-and-transparent display mode.
0	**Display Enable for Icon #3:** When this bit is 1, it enables icon #3 to display.

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6.7.30 SR2E: Graphics-Cursor Horizontal-Position Extension Register

I/O Port Address: 3C5

Index:2E

Bit	Description	Reset State
7	Early OVRW# Signal Delay [2]	0
6	Early OVRW# Signal Delay [1]	0
5	Early OVRW# Signal Delay [0]	0
4	Memory-Write Cycle Delay [1]	0
3	Memory-Write Cycle Delay [0]	0
2	Hardware Icon #0 Address Map Select [1]	0
1	Hardware Icon #0 Address Map Select [0]	0
0	Hardware Cursor Horizontal Fine-Position msb[3]	0

Bit **Description**

7:5 **Early OVRW# Signal Delay [2:0]:**
These three bits are used to define the time interval between the Overlay Window output from the CL-GD7542 and the data input from the external TV decoder.

- This time interval is used for a time differential adjustment that is intended to compensate for the Feature Connector system delay:
  - — *from* the time the OVRW# output is generated
  - — *to* the time the Feature Connector data is presented to the CL-GD7542
- The FCEVIDEO input must be externally synchronized to the data input from the OVRW# output.
- The table that follows shows early clock cycles for either 1x or 2x DCLKs.
  - — The programmed number of early clock cycles defines the delay between the assertion and de-assertion of OVRW# and the corresponding start and end of the overlay window.
  - — The 1x DCLKs are typically 25-MHz clocks that are used for 8-bit pixels.
  - — The 2x DCLKs are typically 50-MHz clocks that are used for 16-bit pixels.

SR2E			Total Early Clock Cycles	
[7]	[6]	[5]	1x DCLK	2x DCLKs
0	0	0	0	3
0	0	1	don't use	4
0	1	0	don't use	5
0	1	1	0	6
1	0	0	1	7
1	0	1	2	8
1	1	0	3	9
1	1	1	11	25

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6.7.30 SR2E: Graphics-Cursor Horizontal-Position Extension Register *(Cont.)*

Bit **Description**

4:3 **Memory-Write Cycle Delay [1:0]:**
These two bits are used to delay the start of a memory-write cycle in units of MCLKs, as explained in the table below:

SR2E [4]	SR2E [3]	Delay Start of Memory-Write Cycle By:	Conditions Under Which to Use:
0	0	3 MCLKs	Use for worst-case timing conditions.
0	1	2 MCLKs	Optimized for 33-MHz PCI bus. Optimized for 50-MHz VESA VL bus.
1	0	1 MCLKs	Optimized for 33-MHz VL bus.
1	1	0 MCLKs	Optimized for 20-MHz VL bus.

2:1 **Hardware Icon #0 Address Map Select [1:0]:**
- When this field is zero, each icon has two memory maps assigned to it.
- When this field is non-zero, only icon #0 can be used.
  - Hardware icon #0 can have up to eight memory maps.
  - The other hardware icons #1:#3 should be disabled.
  - The number in SR2E[2:1] points to the pair of two icon maps selected by SR2A[5], but in this case, all maps will go to icon #0 for display.
  - In this order of significance, SR2E[2:1] and SR2A[5] select the eight memory maps for icon #0.

0 **Hardware Cursor Horizontal Fine Position msb[3]:**
- When SR12[3] = 0, the CPU can modify the hardware cursor position.
- The hardware cursor horizontal fine position is a 4-bit word consisting of this bit and three least-significant bits [2:0], in SRX[7:5].
- The hardware cursor horizontal fine position is used with 10-dot character clocks, when in horizontally expanded graphics modes.
- The hardware cursor horizontal coarse position is in register SR10.
- In non-expanded graphics modes, this bit is always 0.

Note: The hardware cursor must be positioned within 10 dots when horizontal expansion from 640 to 800 is enabled.

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6.7.31 SR2F: Half-Frame-Accelerator FIFO Threshold

I/O Port Address: 3C5

Index:2F

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Half-Frame Accelerator FIFO Threshold [3]	0
2	Half-Frame Accelerator FIFO Threshold [2]	0
1	Half-Frame Accelerator FIFO Threshold [1]	0
0	Half-Frame Accelerator FIFO Threshold [0]	0

Note: These register bits affect only dual-scan panels.

Bit	Description
7:4	Reserved
3:0	**Half-Frame Accelerator FIFO Threshold [3:0]:** The half-frame accelerator FIFO is 16 data stages deep and 32 bits wide. Before a new request can be made for a refill of the half-frame-accelerator read FIFO, SRF[3:0] controls how many 32-bit data stages are empty in the half-frame-accelerator read FIFO. (At the same time that the half-frame-accelerator read FIFO is emptied, it is refilled.) Note: A color LCD has a higher FIFO threshold than a monochrome LCD. (To minimize CRT-FIFO latency, in 16-bit and 24-bit per pixel modes, program a low threshold of 3h for a monochrome LCD. Program 6h for a dual-scan color STN LCD.) Example: If SR2F[3:0] = 4, after only four half-frame-accelerator FIFO stages are empty, a new request, programmed in hex, will be made for new half-frame-accelerator cycles. For this example, program a FIFO threshold that is: • low (2h to 4h) for 2 to 4 data stages for dual-scan monochrome STN panels. • higher (4h to 7h) for 4 to 7 data stages for dual-scan color STN panels. • less than Ah for all other cases.

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6.7.32 GR9: Offset Register 0

I/O Port Address: 3CF

Index:9

Bit	Description	Reset State
7	Offset 0 [7]	0
6	Offset 0 [6]	0
5	Offset 0 [5]	0
4	Offset 0 [4]	0
3	Offset 0 [3]	0
2	Offset 0 [2]	0
1	Offset 0 [1]	0
0	Offset 0 [0]	0

This register is used to access up to 2 Mbytes of display memory with up to 16-Kbyte granularity.

Bit	Description
7:0	**Offset Register 0 [7:0]:** • This offset register is used when one of the following conditions is true: — GRB[0] = 0 — GRB[0] = 1 *and* address bit A[15] = 0 • When one of the above conditions is true *and* GRB[5] = 0: — The register's offset value is added to the contents of XA (bus addresses A[19:12]) to provide XMA, an address into display memory. — Access is for 1 Mbyte of display memory with 4-Kbyte granularity. • When one of the above conditions is true *and* GRB[5] = 1: — The register's offset value is added to the contents of XA (bus addresses A[20:14]) to provide XMA, an address into display memory. — Access is for up to 2 Mbytes of display memory with 16-Kbyte granularity. **XMA.** XMA is the display memory address, prior to modification by address wrap controls. XMA = (Bus Address XA) + (value from Offset Register GR9 or GRA). **XA.** XA is the address on the bus, with bits [16] and [15] possibly forced to a 0 as indicated in the following table.

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6.7.32 GR9: Offset Register 0 *(cont.)*

Configuration		Bus Address XA		
If Display Memory is:	And Register Setting:	[16]	[15]	[14:0]
128 Kbytes	GR6[3:2] = 00	A[16]	A[15]	A[14:0]
64 Kbytes	GR6[3:2] = 01 *AND* GRB[0] = 0 (Offset 1 Disabled)	0	A[15]	A[14:0]
64 Kbytes	GR6[3:2] = 01 *OR* GRB[0] = 1 (Offset 1 Enabled)	0	0	A[14:0]

The XA bus address is summed with the contents of an Offset Register with one of three relative alignments, according to the configuration indicated in the three tables that follow:

Table 6–3. One MByte of Memory, 4 KBytes of Granularity, VGA Mapping

Bus Address (XA)	0	0	0	XA[16]	XA[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[7]	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]
= Display Memory Address (XMA)	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Table 6–4. Two MBytes of Memory, 16 KBytes of Granularity, VGA Mapping

Bus Address	0	0	0	0	XA[16]	XA[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Table 6–5. One MByte or Two MBytes of Memory, 16 KBytes of Granularity, Linear Addressing

Bus Address	LA[20]	LA[19]	LA[18]	LA[17]	A[16]	A[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

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6.7.33 GRA: Offset Register 1

I/O Port Address: 3CF

Index: A

Bit	Description	Reset State
7	Offset 1 [7]	0
6	Offset 1 [6]	0
5	Offset 1 [5]	0
4	Offset 1 [4]	0
3	Offset 1 [3]	0
2	Offset 1 [2]	0
1	Offset 1 [1]	0
0	Offset 1 [0]	0

This register is used to provide access for up to 2 Mbytes of display memory with 16-Kbyte granularity.

Bit	Description
7:0	**Offset 1 [7:0]:** • When GRB[0] = 0, this register is disabled. • When GRB[0] = 1: — *and* A[15] = 1, the contents of GRA[7:0] are added to the contents of A[19:12] to provide access to up to 1 Mbyte of address into display memory, with 4-Kbyte granularity. — *and* GRB[5] = 1, the contents of GRA[6:0] are added to the contents of A[20:14] to provide access to up to 2 Mbytes of address into display memory, with 16-Kbyte granularity.

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6.7.34 GRB: Graphics Controller Mode Extensions Register

I/O Port Address: 3CF

Index: B

Bit	Description	Reset State
7	Reserved	0
6	Reserved	0
5	Offset Granularity	0
4	Enhanced Writes for 16-bit Pixels Enable	0
3	8-Byte-Wide Display Memory Data Latches Enable	0
2	Extended Write Modes Enable	0
1	By-8 Addressing Enable	0
0	Offset Register 1 Enable	0

This register is used to enable or disable extended write modes which provide enhanced performance.

Bit	Description
7:6	Reserved
5	**Offset Granularity:** When this bit is programmed to 1, Offset Registers GR9 and GRA are redefined as containing bits [6:0]. In this case: • These bits are added to address bits [20:14] to provide access to 2 Mbytes of display memory with 16-Kbyte granularity. • SR7[4] (the low-order bit of a 1-Mbyte address page) becomes a don't care. • Linear address memory mapping becomes 2 Mbytes on any 2-Mbyte boundary.
4	**Enhanced Writes for 16-bit Pixels Enable:** GRB[2] must be 1 in order to enable this bit. When both GRB[2] and GRB[4] are programmed to 1, the CL-GD7542 will execute the following enhanced write modes when Extended Write Modes 4 and 5 are enabled and executed: • **By-16 Addressing Enabled:** The system address is shifted by 4, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (16-byte) block in display memory. • **16-Byte Transfer Enabled:** Up to 16 bytes (8 pixels) can be written into display memory for each CPU byte transfer. • **GR10 and GR11 Enabled:** GR10 and GR11 are enabled as foreground and background color extensions • **SR2 Doubling Enabled:** Each bit of SR2 is used as a pixel write mask for two bytes (one pixel).

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6.7.34 GRB: Graphics Controller Mode Extensions Register *(cont.)*

Bit	Description
3	**8-Byte-Wide Display Memory Data Latches Enable:** When this bit is 1, display memory data latches are 8 bytes wide rather than the normal 4 bytes.
2	**Extended Write Modes Enable:** When this bit is 1, the CL-GD7542 will enable and execute the following extended write modes: • **8-Byte Transfer Enabled:** — When GRB[2] = 1, up to 8 bytes (8 pixels) can be written into display memory for each CPU byte transferred. — When GRB[2] = 1 *and* GRB[4] = 1, up to 16 bytes can be written into display memory for color expansion. • **GR5[2] Enabled:** When GRB[2] = 1, Extended Write Modes 4 and 5 can be enabled. • **GR0 Extended:** When GRB[2] = 1, Register GR0 is extended from 4 bits to 8 bits. • **GR1 Extended:** When GRB[2] = 1, Register GR1 is extended from 4 bits to 8 bits. • **SR2 Extended:** When GRB[2] = 1, Register SR2 is extended from 4 bits to 8 bits. • **GRB[4] Enabled:** When GRB[2] = 1, GRB[4] is enabled.
1	**By-8 Addressing Enable:** • When this bit is 1, the system address is shifted by 3, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (8-byte) block in display memory. • When GRB[4] = 1, this bit is a don't care.
0	**Offset Register 1 Enable:** • When this bit is programmed to 1, the value in system address [15] will be used to choose between Offset Register 0 and Offset Register 1. • When this bit is programmed to 0, the value in system address [15] will be ignored, and Offset Register 0 will always be chosen. • This bit must always be programmed to a 0 for 1 Mbyte of linear addressing.

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CL 28676

6.7.35 GRC: Color Key Compare Register

I/O Port Address: 3CF

Index: C

Bit	Description	Reset State
7	Color Key Compare [7]	1
6	Color Key Compare [6]	1
5	Color Key Compare [5]	1
4	Color Key Compare [4]	1
3	Color Key Compare [3]	1
2	Color Key Compare [2]	1
1	Color Key Compare [1]	1
0	Color Key Compare [0]	1

This register contains an 8-bit value that is compared to video data. For more information, refer to Appendix A8.

Bit	Description
7:0	**Color Key Compare [7:0]:** *This register contains an 8-bit value that is compared to the video data. When Mode Switching 10 or 11 is chosen, a match between this value in GRC[7:0] and the video data value will cause the video data pixel to be replaced with data from the feature connector.*

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CL 28677

6.7.36 GRD: Color Key Compare Mask Register

I/O Port Address: 3CF

Index: D

Bit	Description	Reset State
7	Color Key Compare Mask [7]	0
6	Color Key Compare Mask [6]	0
5	Color Key Compare Mask [5]	0
4	Color Key Compare Mask [4]	0
3	Color Key Compare Mask [3]	0
2	Color Key Compare Mask [2]	0
1	Color Key Compare Mask [1]	0
0	Color Key Compare Mask [0]	0

This register contains an 8-bit mask under which the color key comparison of GRC is made. For more information, refer to Appendix A8.

Bit	Description
7:0	**Color Key Compare Mask [7:0]:** A bit value of 1 for a GRD bit will cause the corresponding video data bit to be masked out and not participate in the color comparison.

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CL 28678

6.7.37 GRE: PCI-Burst and Green-PC Control Register

I/O Port Address: 3CF

Index: E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Enable PCI-Bus Burst-Write Mode	0
3	Enable Extensive PCI-Bus Burst-Write Mode	0
2	DPMS (Green PC) Control [1]	0
1	DPMS (Green PC) Control [0]	0
0	DCLK Output Divided By Two	0

This register contains miscellaneous control bits.

Bit 7:5 — Reserved

Bit 4 — Enable PCI-Bus Burst-Write Mode:

- When the PCI bus is selected (SR22[7] = 1 or SR22[0] = 1), and this bit is 1, the CPU may execute burst writes during vertical non-display time.
- When the system BitBLT (bit block transfer) is enabled, the CL-GD7542 automatically disables this burst-write function.
- The CL-GD7542 does not support PCI-burst-read cycles.

Bit 3 — Enable Extensive PCI-Bus Burst-Write Mode:

When the PCI bus is selected (SR22[7] = 1 or SR22[0] = 1), and this bit is 1, the CPU may execute burst writes anytime during a frame.

Bit 2:1 — DPMS (Green PC) Control [1:0]:

These two bits control the CRT monitor power as specified in the Display Power Management Signalling (DPMS) specification, as shown in the following table:

GRE [2]	GRE [1]	CRT Monitor Power Mode	VSYNC Activity	HSYNC Activity	DAC Power	CL-GD7542 Power Management Mode
0	0	On	Pulsing	Pulsing	On	Active
0	1	Standby	Pulsing	Static at MISC[6] inactive level	Off	Active, Standby, or Suspend
1	0	Suspend	Static at MISC[7] inactive level	Pulsing	Off	Active, Standby, or Suspend
1	1	Off	Static at MISC[7] inactive level	Static at MISC[6] inactive level	Off	Active, Standby, or Suspend

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6.7.37 GRE: PCI-Burst and Green-PC Control Register *(Cont.)*

Bit	Description
2:1(*cont.*)	Because the DPMS CRT power-management modes are not related to the CL-GD7542 controller power-management modes, they can be independently programmed, except for the following restrictions: • Prior to placing the CL-GD7542 in Suspend mode, the BIOS may program any DPMS power-saving mode for the CRT. — The 32-kHz input to the CL-GD7542 is used to provide any sync pulse required by the DPMS. • When the CL-GD7542 timer-driven (that is, hardware-controlled) Standby mode is used, the DPMS STANDBY signal is forced by the hardware. — Because the CL-GD7542 Standby mode is timer-driven, software control is not allowed. • When the CL-GD7542 is in LCD-only mode, the BIOS must set GRE[2:1] = 11 to power off any CRT that may be connected to the notebook computer. • The inactive static VSYNC and HSYNC signal levels are determined by the polarity selection in External/General Register MISC[7:6]. — When MISC[7] = 1, the inactive level is low for the VSYNC signal. — When MISC[6] = 1, the inactive level is low for the HSYNC signal.
0	**DCLK Output, Divided By Two:** • When this bit is 0, the CL-GD7542 operates normally. • When this bit is 1, the CL-GD7542 emulates external DAC clocking mode 1. — The DCLK rising edge can be used to clock a 16-bit data pixel low byte. — The DCLK falling edge can be used to clock a 16-bit data pixel high byte. • In the CL-GD7542, the option of setting this bit to 1: — works only for the CRT-only mode. — does not work for the LCD or SimulSCAN mode. When this bit is 1, the clock to the LCD section is also divided by two, which prevents the LCD from working properly.

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CL 28680

6.7.38 GR10: 16-bit Pixel Background Color High Byte Register

I/O Port Address: 3CF

Index: 10

Bit	Description	Reset State
7	Background Color [15]	0
6	Background Color [14]	0
5	Background Color [13]	0
4	Background Color [12]	0
3	Background Color [11]	0
2	Background Color [10]	0
1	Background Color [9]	0
0	Background Color [8]	0

This register contains the high-order eight bits of the background color for Extended Write Mode 5.

Bit	Description
7:0	**Background Color [15:8]:** • The contents of this register: — are the high-order eight bits of the background color for Extended Write Mode 5. — are sent to display memory map planes 1 and 3. • The contents of Graphics Controller Register GR0: — are the low-order eight bits of the background color for Extended Write Mode 5. — are sent to display memory map planes 0 and 2.

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CL 28681

6.7.39 GR11: 16-bit Pixel Foreground Color High Byte Register

I/O Port Address: 3CF

Index: 11

Bit	Description	Reset State
7	Foreground Color [15]	0
6	Foreground Color [14]	0
5	Foreground Color [13]	0
4	Foreground Color [12]	0
3	Foreground Color [11]	0
2	Foreground Color [10]	0
1	Foreground Color [9]	0
0	Foreground Color [8]	0

This register contains the high-order eight bits of the foreground color for Extended Write Modes 5 and 4.

Bit	Description
7:0	**Foreground Color [15:8]:** • The contents of this register: — are the high-order eight bits of the foreground color for Extended Write Modes 5 and 4. — are sent to display memory map planes 1 and 3. • The contents of Graphics Controller Register GR1: — are the low-order eight bits of the foreground color for Extended Write Modes 5 and 4. — are sent to display memory map planes 0 and 2.

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6.7.40 GR20: BLT Width Low Register

I/O Port Address: 3CF

Index: 20

Bit	Description	Reset State
7	BLT Width [7]	0
6	BLT Width [6]	0
5	BLT Width [5]	0
4	BLT Width [4]	0
3	BLT Width [3]	0
2	BLT Width [2]	0
1	BLT Width [1]	0
0	BLT Width [0]	0

This register contains the low-order eight bits of the BitBLT (bit block transfer) width. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Width [7:0]:** This field is the low-order eight bits of the 11-bit value specifying the width-1, in bytes, of the areas involved in a BitBLT.

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CL 28683

6.7.41 GR21: BLT Width High Register

I/O Port Address: 3CF

Index: 21

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	BLT Width [10]	0
1	BLT Width [9]	0
0	BLT Width [8]	0

This register contains the high-order three bits of the BLT width.

Bit	Description
7:3	Reserved
2:0	**BLT Width [10:8]:** This field is the high-order three bits of the 11-bit value specifying the width-1, in bytes, of the areas involved in a BitBLT.

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CL 28684

6.7.42 GR22: BLT Height Low Register

I/O Port Address: 3CF

Index: 22

Bit	Description	Reset State
7	BLT Height [7]	0
6	BLT Height [6]	0
5	BLT Height [5]	0
4	BLT Height [4]	0
3	BLT Height [3]	0
2	BLT Height [2]	0
1	BLT Height [1]	0
0	BLT Height [0]	0

This register contains the low-order eight bits of the BLT height. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Height [7:0]:** This field is the low-order eight bits of the 10-bit value specifying the height-1, in scanlines, of the areas involved in a BitBLT.

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CL 28685

6.7.43 GR23: BLT Height High Register

I/O Port Address: 3CF

Index: 23

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	BLT Height [9]	0
0	BLT Height [8]	0

This register contains the high-order two bits of the BLT height.

Bit	Description
7:2	Reserved
1:0	**BLT Height [9:8]:** This field is the high-order two bits of the 10-bit value specifying the height-1, in scanlines, of the areas involved in a BitBLT.

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CL 28686

6.7.44 GR24: BLT Destination Pitch Low Register

I/O Port Address: 3CF

Index: 24

Bit	Description	Reset State
7	BLT Destination Pitch [7]	0
6	BLT Destination Pitch [6]	0
5	BLT Destination Pitch [5]	0
4	BLT Destination Pitch [4]	0
3	BLT Destination Pitch [3]	0
2	BLT Destination Pitch [2]	0
1	BLT Destination Pitch [1]	0
0	BLT Destination Pitch [0]	0

This register contains the low-order eight bits of the BLT destination pitch. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Destination Pitch [7:0]:** This field is the low-order eight bits of the 12-bit value specifying the destination pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

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CL 28687

6.7.45 GR25: BLT Destination Pitch High Register

I/O Port Address: 3CF

Index: 25

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BLT Destination Pitch [11]	0
2	BLT Destination Pitch [10]	0
1	BLT Destination Pitch [9]	0
0	BLT Destination Pitch [8]	0

This register contains the high-order four bits of the BLT destination pitch. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:4	Reserved
3:0	**BLT Destination Pitch [11:8]:** This field is the high-order four bits of the 12-bit value specifying the destination pitch of the areas involved in a BitBLT.

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6.7.46 GR26: BLT Source Pitch Low Register

I/O Port Address: 3CF

Index: 26

Bit	Description	Reset State
7	BLT Source Pitch [7]	0
6	BLT Source Pitch [6]	0
5	BLT Source Pitch [5]	0
4	BLT Source Pitch [4]	0
3	BLT Source Pitch [3]	0
2	BLT Source Pitch [2]	0
1	BLT Source Pitch [1]	0
0	BLT Source Pitch [0]	0

This register contains the low-order eight bits of the BLT source pitch. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Source Pitch [7:0]:** This field is the low-order eight bits of the 12-bit value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

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6.7.47 GR27: BLT Source Pitch High Register

I/O Port Address: 3CF

Index: 27

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BLT Source Pitch [11]	0
2	BLT Source Pitch [10]	0
1	BLT Source Pitch [9]	0
0	BLT Source Pitch [8]	0

This register contains the high-order four bits of the BLT source pitch.

Bit	Description
7:4	Reserved
3:0	**BLT Source Pitch [11:8]:** This field is the high-order four bits of the 12-bit value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

6.7.48 GR28: BLT Destination Start Low Register

I/O Port Address: 3CF

Index: 28

Bit	Description	Reset State
7	BLT Destination Start [7]	0
6	BLT Destination Start [6]	0
5	BLT Destination Start [5]	0
4	BLT Destination Start [4]	0
3	BLT Destination Start [3]	0
2	BLT Destination Start [2]	0
1	BLT Destination Start [1]	0
0	BLT Destination Start [0]	0

This register contains the low-order eight bits of the BLT destination start. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Destination Start [7:0]:** This field is the low-order eight bits of the 21-bit BLT destination start value that specifies the byte address of the beginning destination pixel for a BitBLT.

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6.7.49 GR29: BLT Destination Start Mid Register

I/O Port Address: 3CF

Index: 29

Bit	Description	Reset State
7	BLT Destination Start [15]	0
6	BLT Destination Start [14]	0
5	BLT Destination Start [13]	0
4	BLT Destination Start [12]	0
3	BLT Destination Start [11]	0
2	BLT Destination Start [10]	0
1	BLT Destination Start [9]	0
0	BLT Destination Start [8]	0

This register contains the middle eight bits of the BLT destination start.

Bit	Description
7:0	**BLT Destination Start [15:8]:** This field is the middle eight bits of the 21-bit BLT destination start value that specifies the byte address of the beginning destination pixel for a BitBLT.

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CL 28692

6.7.50 GR2A: BLT Destination Start High Register

I/O Port Address: 3CF

Index: 2A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BLT Destination Start [20]	0
3	BLT Destination Start [19]	0
2	BLT Destination Start [18]	0
1	BLT Destination Start [17]	0
0	BLT Destination Start [16]	0

This register contains the high-order five bits of the BLT destination start.

Bit	Description
7:0	**BLT Destination Start [20:16]:** This field is the high-order five bits of the 21-bit BLT destination start value that specifies the byte address of the beginning destination pixel for a BitBLT.

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CL 28693

6.7.51 GR2C: BLT Source Start Low Register

I/O Port Address: 3CF

Index: 2C

Bit	Description	Reset State
7	BLT Source Start [7]	0
6	BLT Source Start [6]	0
5	BLT Source Start [5]	0
4	BLT Source Start [4]	0
3	BLT Source Start [3]	0
2	BLT Source Start [2]	0
1	BLT Source Start [1]	0
0	BLT Source Start [0]	0

This register contains the low-order eight bits of the BLT source start. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Source Start [7:0]:** This field is the low-order eight bits of the 21-bit BLT source start value that specifies the byte address of the beginning source pixel for a BitBLT.

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6.7.52 GR2D: BLT Source Start Mid Register

I/O Port Address: 3CF

Index: 2D

Bit	Description	Reset State
7	BLT Source Start [15]	0
6	BLT Source Start [14]	0
5	BLT Source Start [13]	0
4	BLT Source Start [12]	0
3	BLT Source Start [11]	0
2	BLT Source Start [10]	0
1	BLT Source Start [9]	0
0	BLT Source Start [8]	0

This register contains the middle eight bits of the BLT source start.

Bit	Description
7:0	**BLT Source Start [15:8]:** This field is the middle eight bits of the 21-bit BLT source start value that specifies the byte address of the beginning source pixel for a BitBLT.

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6.7.53 GR2E: BLT Source Start High Register

I/O Port Address: 3CF

Index: 2E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BLT Source Start [20]	0
3	BLT Source Start [19]	0
2	BLT Source Start [18]	0
1	BLT Source Start [17]	0
0	BLT Source Start [16]	0

This register contains the high-order five bits of the BLT source start.

Bit	Description
7:5	Reserved
4:0	**BLT Source Start [20:16]:** This field is the high-order five bits of the 21-bit BLT source start value that specifies the byte address of the beginning source pixel for a BitBLT.

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6.7.54 GR30: BLT Mode Register

I/O Port Address: 3CF

Index: 30

Bit	Description	Reset State
7	Enable Color Expand	0
6	Enable 8 x 8 Pattern Copy	0
5	Reserved	
4	Color Expand / Transparency Width	0
3	Enable Transparency Compare	0
2	BLT Source Display Memory / System Memory	0
1	BLT Destination Display Memory / System Memory	0
0	BLT Direction	0

This register contains the bits that specify the BitBLT (bit block transfer) details, but not the BLT raster operation. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7	**Enable Color Expand:** • When this bit is programmed to 1, the raster operation source will be the expanded result from the bit-mapped source. — The destination must be screen memory. — The direction must be incremental. — Raster operations are available for all block moves. — Graphics Controller Registers GR0 and GR1 and Extension Registers GR10 and GR11 are used for bit-map color-expanded BLT operations. — When the source data is expanded, the most-significant bit of the first source byte will become the first pixel in the screen memory destination. — For color-expanded BLTs (the source is system memory or display memory), each logical line must be an even byte. — Source bytes must be completely used. As a result, when a logical line is not an even multiple of eight pixels, 'dummy' bits are used to fill it out to an even byte. — 'Dummy' bits will be ignored under control of the BLT width setting. — When the source of color-expanded data is display memory, the source starting address must be on a 4-byte boundary, and the addressing will always be linear. (The source pitch will be ignored.) — Fo. information regarding color expansion, refer to Appendix A4. • When this bit is programmed to 0, the raster operation source will be the pixel data read from the source.

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6.7.54 GR30: BLT Mode Register *(cont.)*

Bit	Description
6	**Enable 8 x 8 Pattern Copy:** When this bit is 1, the source pattern will be copied repeatedly to the destination rectangular area. • The pattern source must be aligned on a four-byte boundary. • The pattern source will be linear-addressed data in one of three arrangements as shown in the following table:

Operating Mode	Pattern Source Arrangement
Color Expansion Enabled	8 bytes of monochrome bitmap for the 8 x 8 pattern
8-bit Pixels	64 bytes of color data for 64 pixels
16-bit Pixels	128 bytes of color data for 64 pixels

5	Reserved
4	**Color Expand / Transparency Width:** • When GR30[7] is 1: — *and* this bit is 1, the bit-mapped source will be expanded to 16 bits/pixel. — *and* this bit is 0, the bit-mapped source will be expanded to 8 bits/pixel. • When GR30[3] is 1: — *and* this bit is 1, the transparency compare will be on 16-bit pixels. — *and* this bit is 0, the transparency compare will be on 8-bit pixels.
3	**Enable Transparency Compare:** • When this bit is 1, then for each pixel, the result of the raster operation is compared to the Transparent Color Registers (Extension Registers GR34 and GR35). — When the compare is a match, data are not written to the destination. — When the color-expand BLT is to be used with an opaque foreground and a transparent background (similar to Extended Write Mode 4), the transparency feature must be used, and the transparent color must be set to the background color. • When this bit is 0, the data are written to the destination without regard to Transparent Color Registers GR34 and GR35.

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6.7.54 GR30: BLT Mode Register *(cont.)*

Bit	Description
2	**BLT Source Display Memory / System Memory:** • When this bit is 1, the BLT source will be system memory. — The CPU will perform the system bus transfers, but the CL-GD7542 will ignore the address provided with such transfers. — The CPU is required to transfer data in increments of four bytes. When the total number of bytes moved for a BLT is not a multiple of four, the CPU must write 'extra' bytes. — System-memory-to-system-memory BLTs are not allowed. • When this bit is 0, the BLT source will be display memory. • When system-to-screen BitBLTs are being executed: — that involve color expansion, the BLT Source Start Registers GR2C, GR2D, and GR2E must be cleared to 0. — that do not involve color expansion, 16-bit host transfers must be used, or the system will become non-operative.
1	**BLT Destination Display Memory / System Memory:** • When this bit is 1, the BLT destination will be system memory. — The CPU will perform the system bus transfers, but the CL-GD7542 will ignore the address provided with such transfers. — The CPU is required to transfer data in increments of four bytes. When the total number of bytes moved for a BLT is not a multiple of four, the CPU must read 'extra' bytes. — System-memory-to-system-memory BLTs are not allowed. • When this bit is 0, the BLT destination will be display memory. • When system-to-screen BitBLTs are being executed, 16-bit host transfers must be used, or the system will become non-operative.
0	**BLT Direction:** When this bit: • is 1: — the source and destination addresses will be decremented. — The BLT will proceed from higher addresses to lower addresses. — The starting address will be the highest addressed byte in each area. • is 0: — the source and destination addresses will be incremented. — The BLT will proceed from lower addresses to higher addresses.

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CL 28699

6.7.55 GR31: BLT Start / Status Register

I/O Port Address: 3CF

Index: 31

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BLT Progress Status (Read Only)	0
2	BLT Reset	0
1	BLT Start / Suspend	0
0	BLT Status (Read Only)	0

This register contains the bit that begins a BLT and a bit that indicates whether the BLT has completed. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:4	Reserved
3	**BLT Progress Status (Read Only):** This bit will be set to 1 at the start of a BLT. • When the BLT operation resets (refer to GR32[2]), this bit clears to 0. • When the BLT operation suspends (refer to GR31[1]), this bit remains a 1.
2	**BLT Reset:** • When this bit is set to 1: — The entire BLT engine is immediately reset and any operation in progress will be terminated. The operation cannot be restarted. — GR31[3] clears to 0. • This bit must be cleared to 0 before any BitBLT operations are attempted.
1	**BLT Start / Suspend:** • When this bit is set to 1, the BLT starts with the next available display memory cycle. • GR31[0] must be monitored to determine when the BLT is complete. • This bit will clear to 0 when the BLT completes. • When this bit is cleared to 0, the BLT suspends at the current scanline end. — When the BLT is suspended, the BLT Height Registers reflect the line count for the last completed transfer. — When the BLT is suspended, GR31[3] remains a 1. — A suspended BLT may resume by setting this bit to 1.
0	**BLT Status (Read Only):** • When this bit is a 1, the BLT is in progress. • When this bit is a 0, the BLT is complete.

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CL 28700

6.7.56 GR32: BLT Raster Operation Register (ROP)

I/O Port Address: 3CF

Index: 32

Bit	Description	Reset State
7	f [7]	0
6	f [6]	0
5	f [5]	0
4	f [4]	0
3	f [3]	0
2	f [2]	0
1	f [1]	0
0	f [0]	0

This register selects a raster operation function. For more information, refer to Appendix A1.

Bit	Description
7:0	**f [7:0]:** This eight-bit value selects 1 of 16 possible two-operand raster operation (ROP) functions, as indicated in the table below:

Z (Logical Function: Algebraic Notation)	ROP No. (Hex)	Comparable Microsoft Name	Value Microsoft Uses to Get ROP
0	00	BLACKNESS	00000042
1	0E	WHITENESS	00FF0062
S	0D	SRCCOPY	00CC0020
D	06	–	00AA0029
-S	D0	NOTSRCCOPY	00330008
-D	0B	DSTINVERT	00550009
S.D	05	SRCAND	008800C6
S.-D	09	SRCERASE	00440328
-S.D	50	–	00220326
-S.-D	90	NOTSRCERASE	001100A6
S+D	6D	SRCPAINT	00EE0086
S+-D	AD	–	00DD0228
-S+D	D6	MERGEPAINT	00BB0226
-S+-D	DA	–	007700E6
S- = D	59	SRCINVERT (xor)	00660046
S = D	95	- (xnor)	00990066

6.7.57 GR34: BLT Transparent Color Low Register

I/O Port Address: 3CF

Index: 34

Bit	Description	Reset State
7	BLT Transparent Color [7]	0
6	BLT Transparent Color [6]	0
5	BLT Transparent Color [5]	0
4	BLT Transparent Color [4]	0
3	BLT Transparent Color [3]	0
2	BLT Transparent Color [2]	0
1	BLT Transparent Color [1]	0
0	BLT Transparent Color [0]	0

This register contains the low-order eight bits of the 16-bit Transparent Color. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Transparent Color [7:0]:** • This field is the low-order eight bits of the BLT Transparent Color. • When GR30[3] = 1, this value will be compared with the raster operation result. If it is equal, the raster operation result is not written to the destination.

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CL 28702

6.7.58 GR35: BLT Transparent Color High Register

I/O Port Address: 3CF

Index: 35

Bit	Description	Reset State
7	BLT Transparent Color [15]	0
6	BLT Transparent Color [14]	0
5	BLT Transparent Color [13]	0
4	BLT Transparent Color [12]	0
3	BLT Transparent Color [11]	0
2	BLT Transparent Color [10]	0
1	BLT Transparent Color [9]	0
0	BLT Transparent Color [8]	0

This register contains the high-order eight bits of the 16-bit Transparent Color. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Transparent Color [15:8]:** • This field is the high-order eight bits of the BLT Transparent Color. • When Graphics Controller Register GR30[3] = 1, this value will be compared with the raster operation result. If it is equal, the result is not written to the destination. • For 8-bit color modes, Graphics Controller Register GR35 must be set equal to GR34.

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CL 28703

6.7.59 GR38: BLT Transparent Color Mask Low Register

I/O Port Address: 3CF

Index: 38

Bit	Description	Reset State
7	BLT Transparent Color Mask [7]	0
6	BLT Transparent Color Mask [6]	0
5	BLT Transparent Color Mask [5]	0
4	BLT Transparent Color Mask [4]	0
3	BLT Transparent Color Mask [3]	0
2	BLT Transparent Color Mask [2]	0
1	BLT Transparent Color Mask [1]	0
0	BLT Transparent Color Mask [0]	0

This register contains the low-order eight bits of the 16-bit Transparent Color Mask. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Transparent Color Mask [7:0]:** • This field is the low-order eight bits of the BLT Transparent Color Mask. • When Graphics Controller Register GR30[3] = 1, the transparent color will be compared with the raster operation result under this mask. If it is equal, the result is not written to the destination. • A 1 in any bit location makes the corresponding compare a don't care.

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CL 28704

6.7.60 GR39: BLT Transparent Color Mask High Register

I/O Port Address: 3CF

Index: 39

Bit	Description	Reset State
7	BLT Transparent Color Mask [15]	0
6	BLT Transparent Color Mask [14]	0
5	BLT Transparent Color Mask [13]	0
4	BLT Transparent Color Mask [12]	0
3	BLT Transparent Color Mask [11]	0
2	BLT Transparent Color Mask [10]	0
1	BLT Transparent Color Mask [9]	0
0	BLT Transparent Color Mask [8]	0

This register contains the high-order eight bits of the 16-bit Transparent Color Mask.

Bit	Description
7:0	**BLT Transparent Color Mask [15:8]:** • This field is the high-order eight bits of the BLT Transparent Color Mask. • When Graphics Controller Register GR30[3] = 1, the transparent color will be compared with the raster operation result under this mask. If it is equal, the result is not written to the destination. • For 8-bit color modes, GR39 must equal GR38. • A 1 in any bit location makes the corresponding compare a don't care.

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CL 28705

6.7.61 CR19: Interlace End Register

I/O Port Address: 3?5

Index: 19

Bit	Description	Reset State
7	Interlace End [7]	0
6	Interlace End [6]	0
5	Interlace End [5]	0
4	Interlace End [4]	0
3	Interlace End [3]	0
2	Interlace End [2]	0
1	Interlace End [1]	0
0	Interlace End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains the ending horizontal character count for the Odd Field VSYNC.

Bit	Description
7:0	**Interlace End:** • This value is the number of characters in the last scanline of the Odd Field in interlaced timing. • This value can be adjusted to center the scanlines in the Odd Field half-way between scanlines in the Even Field. • This register is typically programmed to approximately half of the Horizontal Total.

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6.7.62 CR1A: Miscellaneous Control Register

I/O Port Address: 3?5

Index: 1A

Bit	Description	Reset State
7	Vertical Blanking End Extension [9]	0
6	Vertical Blanking End Extension [8]	0
5	Horizontal Blanking End Extension [7]	0
4	Horizontal Blanking End Extension [6]	0
3	DAC Mode Switching / Overlay Mode Control [1]	0
2	DAC Mode Switching / Overlay Mode Control [0]	0
1	Enable Double Buffered Display Start Address	0
0	Enable Interlaced Timing	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains timing extension bits as well as some miscellaneous control bits.

Bit **Description**

7:6 **Vertical Blanking End Extension [9:8]:**
This two-bit field is used to extend the Vertical Blanking End value to 10 bits.
- These bits are enabled only when CR1B[5] is 1 or when CR1B[7] is 1.
- For more information on the functioning of these bits, refer to CR16.

5:4 **Horizontal Blanking End Extension [7:6]:**
This two-bit field is used to extend the Horizontal Blanking End value to 8 bits.
- These bits are enabled only when CR1B[5] is 1 or when CR1B[7] is 1.
- For more information on the functioning of these bits, refer to CR3[4:0].

3:2 **DAC Mode Switching / Overlay Mode Control [1:0]:**
This field is used to select DAC Mode Switching and Overlay Mode, as summarized in the following table. For more information, refer to Appendix A8.

CR1A [3]	CR1A [2]	DAC Mode Switching Enabled or Disabled	Overlay Mode Control
0	0	(Normal VGA-compatible operation.)	
		Disabled	No Overlay.
0	1	Enabled	Overlay controlled with FCEVIDEO#.
1	0	Enabled	Overlay controlled with color key and OVRW#.
1	1	Enabled	Overlay controlled with color key only.

Continued on next page

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6.7.62 CR1A: Miscellaneous Control Register *(cont.)*

Bit	Description
1	**Enable Double Buffered Display Start Address:** When this bit is 1, the Display Start Address will be updated on the VSYNC following a write to Start Address Low. This update provides control of display frame switching without the need to explicitly monitor VSYNC.
0	**Enable Interlaced Timing:** When this bit is 1, it enables interlaced timing. • In text mode, interlaced sync is enabled. • In graphics mode: — Both interlaced sync and video data are enabled. — For both interlaced sync and video data, the CRTC Scanline Double bit (CR9[7]) must be 0. — Graphics modes 4 and 6 must always be non-interlaced. • When this bit is 1, IRQ requests are generated only at the end of odd fields, that is, at the end of a frame.

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6.7.63 CR1B: Extended Display Controls Register

I/O Port Address: 3?5

Index: 1B

Bit	Description	Reset State
7	Enable Blanking End Extension	0
6	Enable Text Mode Fast-Page	0
5	Blanking Control	0
4	Offset Register Extension [8]	0
3	Screen A Start Address Bit [18]	0
2	Screen A Start Address Bit [17]	0
1	Enable Extended Address Wrap	0
0	Screen A Start Address Bit [16]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains miscellaneous bits that control extended display functions.

Bit	Description
7	**Enable Blanking End Extension:** • When this bit is 1, the Vertical and Horizontal Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are enabled, regardless of the CR1B[5] level. • When this bit is 0 and CR1B[5] = 0, the Vertical and Horizontal Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are disabled.
6	**Enable Text Mode Fast-Page:** • When this bit is 0, all font fetch cycles take place as random-read cycles. This bit must be 0 for standard VGA dual-font operation. • When this bit is 1, fast-page-mode cycles will be used to fetch font data. This setting allows for text modes with a VCLK greater than 30 MHz, as is required for 132-column modes.
5	**Blanking Control:** • When this bit is 0 (the standard VGA mode): — The blanking signal generated by the CRTC controls the DAC blanking. — The border can be used. (For more information, refer to AR11.) • When this bit is 1: — The display enable controls the DAC blanking. — The border cannot be used, as the blanking registers will no longer be available to control the border. Instead, the blanking registers are used to generate the OVRW# signal. — The DAC is blanked during the time the border is normally displayed. — The OVRW# pin is an output and follows the blanking signal generated by the CRTC. — The Vertical and Horizontal Blanking End Extension Bits in CR1A[7:4] are enabled and used to specify the active portion of the video overlay. For more information, refer to Appendix A8.

Continued on next page.

6.7.63 CR1B: Extended Display Controls Register *(cont.)*

Bit	Description
4	**Offset Register Extension [8]:** This bit is the most-significant ninth bit of the CRT Controller Offset field. For more information, refer to CRT Controller Offset Register CR13.
3:2	**Screen A Start Address Bits [18:17]:** These are the most-significant two bits of the CTR Controller Screen A Start Address Registers CRC and CRD. Bit 16 is in CR1B[0].
1	**Enable Extended Address Wrap:** • When this bit is 0, VGA compatibility is offered as follows: — the CRTC Character Address Counter is 16 bits wide. — the display memory address wraps at 64K maps (for 256K total memory). • When this bit is 1: — *and* Chain-4 addressing is selected (Sequencer Register SR4[3] = 1), then DRAM addresses MA[0] and MA[1] are supplied from addresses XMA[16] and XMA[17]. The other DRAM addresses are supplied from the XMA[18:12] addresses,which are the sum of bus addresses XA[16:12] and either Graphics Controller Offset Register 0 (GR9) or Offset Register 1 (GRA). — *and* CRTC Double Word addressing is selected (CR14[6] = 1), then DRAM addresses MA[0] and MA[1] are supplied from the CL-GD7542 internal CRT address counter addresses CR[14] and CR[15]. This action provides four displayable pages in video mode 13h. — the CL-GD7542 internal CRT character counter addresses CA[16] and CA[18] provide up to 256K bytes in each bit plane, or one Mbyte of packed-pixel memory. — the CL-GD7542 CRT controller address counter is 19 bits wide. — the display memory address wraps at the total available memory size.
0	**Screen A Start Address Bit [16]:** This is bit 16 of the Screen A Start Address. Bits 17 and 18 are in CR1B[3:2]. For more information, refer to CRT Controller Screen A Start Address Registers CRC and CRD.

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6.7.64 CR1D: Overlay Mode Register

I/O Port Address: 3?5

Index: 1D

Bit	Description	Reset State
7	Reserved	
6	Overlay Timing Signal Source	0
5	Reserved	
4	Reserved	
3	Reserved	
2	DAC Mode Switching Control [1]	0
1	DAC Mode Switching Control [0]	0
0	Reserved	

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains controls for the extended overlay modes.

Bit 7 — Reserved

Bit 6 — **Overlay Timing Signal Source:**

- When this bit is 0, *and* Extension Register CR1A[3:2] = 01, the FCEVIDEO# input is used as the timing signal for the overlay modes.
- When this bit is 1, *and* Extension Register CR1A[3:2] = 10, the internally generated OVRW# output is used as the timing signal for the overlay modes. This bit setting eliminates the need to connect the OVRW# output to the FCEVIDEO# input.

Bits 5:3 — Reserved

Bits 2:1 — **DAC Mode Switching Control [1:0]:**
This field controls DAC mode switching. CR1A[3:2] selects the overlay mode.

CR1D		DAC Mode Switch State and Results		
[2]	[1]	DAC Mode Switch State	Result for: Background	Result for: Overlay Window Mode
0	0	True. Selected Extended DAC mode is enabled	VGA data from display memory (typically mode 5F)	Live video (typically true color)
0	1	False. Selected Extended DAC mode is enabled6	Live video (typically true color)	VGA data from display memory (typically mode 5F)
1	X	Don't Care. Extended DAC mode is disabled	-	-

Bit 0 — Reserved

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6.7.65 CR1E: LCD Shading

I/O Port Address: 3?5

Index: 1E

Bit	Description	Access	Reset State
7(MSB)	Shade Mapping [1]	R/W	0
6	Shade Mapping [0]	R/W	0
5	Reverse Video for Text Modes	R/W	0
4	Reverse Video for Graphics Modes	R/W	0
3	Reserved		
2	Horizontal CRTC Registers Access Control Override	R/W	0
1	Text-Mode Contrast Enhancement	R/W	0
0(LSB)	Graphics Mode Dithering Enable	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit — **Description**

7:6 **Shade Mapping [1:0]:**
These two bits are used to program monochrome grayscale mapping (that is, shading) according to the following table:

CR1E [7]	CR1E [6]	Shade Map
0	0	Graphics Mode. 18-bit output of Look-up Table converted to 64 shades, with NTSC weighting.
0	0	Reserved
1	0	Text Mode. Direct display of up to 16 or 64 shades of pixel data (4-bit planar, or lower 6 of 8 bits packed-pixel)
1	1	Reserved

5 **Reverse Video for Text Modes:**
When this bit is 1, all text modes are displayed in reverse video.

4 **Reverse Video for Graphics Modes:**
When this bit is 1, all graphics modes are displayed in reverse video.

3 Reserved

Continued on next page.

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6.7.65 CR1E: LCD Shading *(cont.)*

Bit	Description
2	**Horizontal CRTC Registers Access Control Override:** If this bit is 0: • *and* the following conditions exist: — CR20[5] = 1 (the LCD panel interface is enabled) — R9X[3:2] = 01 (the LCD panel interface is set for 800 x 600 panel) — CR2E[3:2] = 11 (horizontal expansion is on) — CR2E[5] = 1 (horizontal centering is on) then standard CRT Controller Horizontal Registers CR0,2,3,4,5 are automatically used to control the CRT controller. • *but* not all of the above conditions take place as described, then horizontal timing shadow registers RiY and RiZ are automatically used to control the CRT controller. If this bit is 1: • then the automatic selection described above is overridden, and horizontal timing shadow registers RiY and RiZ are automatically used to control the CRT controller.
1	**Text-Mode Contrast Enhancement:** This bit is used along with R8X[4] to enable text-mode contrast enhancement.

CR1E[1]	R8X[4]	Text-Mode Contrast-Enhancement Characteristics
0	0	No enhancement of text mode.
0	1	Foreground-only enhancement If BG > FG, then BGC = BG and FGC = 0. If BG < FG, then BGC = BG and FGC = 1.
1	0	Contrast enhancement If BG > FG, then BGC = BG and FGC = 0. If BG < FG, then BGC = 0 and FGC = FG.

BG = Background, FG = Foreground, xxC = Color

0	**Graphics Mode Dithering Enable:** This bit: • = 1 to enable dithering in graphics mode. • = 0 to disable dithering in non-packed pixel graphics mode.

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6.7.66 CR1F: LCD Modulation Control

I/O Port Address: 3?5

Index: 1F

Bit	Description	Access	Reset State
7(MSB)	External / Internal Modulation Control	R/W	0
6	MOD or Retrace LLCLK Control [6]	R/W	0
5	MOD or Retrace LLCLK Control [5]	R/W	0
4	MOD or Retrace LLCLK Control [4]	R/W	0
3	MOD or Retrace LLCLK Control [3]	R/W	0
2	MOD or Retrace LLCLK Control [2]	R/W	0
1	MOD or Retrace LLCLK Control [1]	R/W	0
0(LSB)	MOD or Retrace LLCLK Control [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used for one of two purposes:

1. It controls the characteristics of the LCD Modulation (MOD) signal.
2. During vertical blanking, it generates extra line clocks (LLCLKs), which have two functions.
   a. They eliminate any "waterfall motion" (rolling lines appearing on the entire panel).
   b. They guarantee the panel receives a specific number of LLCLKS per frame.

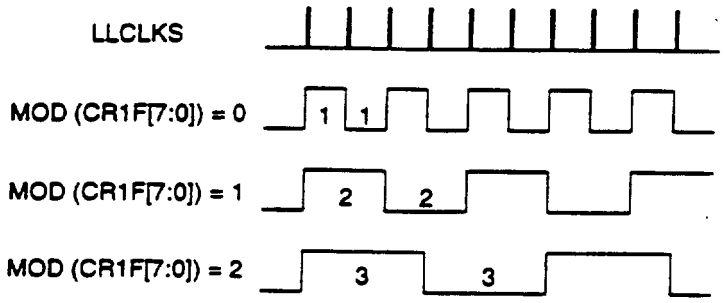
Bit	Description
7	**External or Internal Modulation Control:** This bit controls the source of the modulation (MOD) signal for the LCD. • Clear this bit to 0 when an LCD needs an externally supplied MOD signal. — In this case, CR1F[6:0] can be used to program from 1 to 128 scanlines before MOD changes polarity. — Program CR1F[6:0] to determine the half-period of the square-wave output on the MOD pin, based on the programmed number of LLCLKs

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6.7.66 CR1F: LCD Modulation Control *(cont.)*

Bit	Description
7(Cont.)	**External or Internal Modulation Control:** • When CR1F[7] = 0, the resulting value of the MOD signal is one more than the value that is programmed into CR1F[7:0]. — For example, if register bits CR1F[7:0] are programmed: — to 0, the half-period of the square-wave MOD output is 1. — to 1, the half-period of the square-wave MOD output is 2. — to 2, the half-period of the square-wave MOD output is 3.



	• Set this bit to 1 when the LCD generates its own internal MOD signal and does not require an externally supplied MOD signal. (In addition, set CR1F[6:0] appropriately, as described below.)
6:0	**MOD or Retrace LCD Line Clock (LLCLK) Control [6:0]:** • When CR1F[7] is 0: — The LCD requires an externally supplied MOD signal. — The contents of CR1F[6:0] can select up to 128 scanlines before the MOD signal changes polarity. • When CR1F[7] is 1: — The LCD generates its own internal MOD signal and does not require an externally supplied MOD signal. — For dual-scan LCDs, program CR1F[6:0] for only the number of LLCLKs that appear during vertical retrace (seen on every other half-frame of the LCD). — For single-scan LCDs, program CR1F[6:0] for the total number of LLCLKs for the entire frame of the LCD. — The contents of CR1F[6:0] are added to 180 hex (384 decimal) to determine the total number of LLCLKs. (The number 180 hex has been determined to allow a working range of LLCLKs.) Total number of LLCLKs = 180h + [value in (CR1F[6:0])]

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6.7.67 CR20: Power Management Register

I/O Port Address: 3?5

Index: 20

Bit	Description	Access	Reset State
7(MSB)	Debounce Timer Resolution	R/W	0
6	CRT Enable	R/W	0
5	LCD Enable	R/W	0
4	Activate Standby Mode	R/W	0
3	Activate Suspend Mode	R/W	0
2	DRAM Refresh Select [1]	R/W	0
1	DRAM Refresh Select [0]	R/W	0
0(LSB)	Text Mode Shading Control	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Debounce Timer Resolution:** • When this bit is 0, the debounce-timer resolution = 30 µsec (32-kHz period). • When this bit is 1, the debounce-timer resolution = 1.0 sec.
6	**CRT Enable:** Setting this bit to 1 enables the analog CRT output from the video DAC.
5	**LCD Enable:** To enable the LCD interface, set this bit to 1. • When this bit has a transition that is : — low to high, the CL-GD7542 LCD power-up sequence will occur, which enables the internal LCD BIAS, backlight, logic supply, and drive signals. — high to low, the CL-GD7542 LCD power-down sequence will occur, which disables the internal LCD BIAS, backlight, logic supply, and drive signals. • When this bit is 1, the Line Frame Signal (LFS) and LCD Line Clock (LLCLK) timing signals for monochrome LCDs are generated. These bits are generated from the LCD Timing Registers, R0X through RBX. — For most TFT-color LCDs, the sync timing programmed by the CRT controller is used, in which case, specially compensated VSYNC and HSYNC signals are sent to the LFS and LLCLK outputs. — In addition, the display enable signal controls the display data. • When this bit is 1, some VGA register bits are redefined for LCDs as shown in the following table:

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6.7.67 CR20: Power Management Register *(cont.)*

Bit **Description**

5 (Cont.)

VGA-Defined Register Bits	New LCD Definition for Register Bits *When CR20[5] = 1*
AR13[3:0]	When Sequencer Register SR1[0] = 0 (DCLK is divided by 8) and when pixel panning, the shift effect of Attribute Controller Register AR13[3:0] is masked. As a result, a value of either 8h or 0h equals a "no shift".
MISC[7:6]	CRT sync polarity bits are redefined for External/General Register MISC[7:6] so that 00 = 800 x 600 LCD and 11 = 640 x 480 LCD.
SR1[0]	This bit is locked to 0 so that it is = 8 dots/character.
SR1[3]	Except for video mode 13, this bit selects the horizontally-locked timing for 40- or 80-column (character) modes.

NOTE: Clock select bits do not need to be locked. As required by the LCD, clock programming registers must be set for the same frequency.

4 **Activate Standby Mode:**
Setting this bit to 1 overrides the current internal Standby timer setting and immediately places the CL-GD7542 into Standby mode.

3 **Activate Suspend Mode:**
Setting this bit to 1 initiates software-controlled Suspend mode. In this mode, the power-down sequence is started to blank the LCD.

2:1 **DRAM Refresh Select:**
The programming of these two bits control the type of refresh applied to the display memory during Suspend mode as follows.

CR20 [2]	CR20 [1]	Display Memory Refresh Type
0	0	Refresh cycle 8 ms, CAS*-before-RAS*.
0	1	Refresh cycle 64-ms, CAS*-before-RAS*.
1	0	Self-refresh
1	1	No refresh All clock inputs are disabled. All outputs to display memory are high-impedance.

0 **Text Mode Shading Control.**
When this bit:
- is 0, text shades are derived directly from foreground/background data.
- is 1, text shades are derived the same way as graphics, with CR1E[7:6].

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6.7.68 CR21: Power-Down Timer Control

I/O Port Address: 3?5

Index: 21

Bit	Description	Access	Reset State
7(MSB)	Timer for FPBL Control [3]	R/W	0
6	Timer for FPBL Control [2]	R/W	0
5	Timer for FPBL Control [1]	R/W	0
4	Timer for FPBL Control [0]	R/W	0
3	Timer for Standby Mode Control [3]	R/W	0
2	Timer for Standby Mode Control [2]	R/W	0
1	Timer for Standby Mode Control [1]	R/W	0
0(LSB)	Timer for Standby Mode Control [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register has two timers, each of which control the time at which power to the LCD is switched off.

- Programming CR21[7:4] controls the time it takes for the LCD backlight to switch off.
- Programming CR21[3:0] controls the time it takes for the Standby mode to be entered and power to the LCD to be switched off.

The timers operate as follows.

- Both timers may be set for times from 1 to 15 minutes.
- A programmed value of zero disables the timer.
- Instead of 60 seconds, the timers use 64 seconds for each "minute" programmed.
- The timers subtract a correcting factor of 32 seconds from the timed subtotal.
- For example, a setting of 15 minutes (Fh) will result in:

  [(15 counts X 64 seconds) – 32 seconds] =
  [(960 seconds) – 32 seconds] =
  928 seconds, or an actual time of (928 ÷ 60) = 15.5 minutes.

For typical power-down timer settings, refer to the table shown.

Bit	Description
7:4	**Timer for FPBL [3:0]:** These bits program the value for the internal flat panel backlight timer.
3:0	**Timer for Standby Mode Control [3:0]:** These bits program the value for the internal Standby mode timer.

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6.7.68 CR21: Power-Down Timer Control *(cont.)*

Table 6–6. Typical Power-Down Timer Settings

CR21 Backlight Timer Control Bits				Hex Code	Actual Seconds Programmed for Delay Time (Seconds)	Approximate Corresponding Delay Time (Minutes)
[7]	[6]	[5]	[4]			
CR21 Standby Mode Timer Control Bits						
[3]	[2]	[1]	[0]			
0	0	0	0	0h	disabled	disabled
0	0	0	1	1h	32	0.5
0	1	0	1	5h	288	4.8
0	1	1	1	7h	416	6.9
1	0	1	0	Ah	608	10.1
1	1	1	1	Fh	928	15.5

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6.7.69 CR23: SUSPI Debounce Timer

I/O Port Address: 3?5

Index: 23

Bit	Description	Access	Reset State
7(MSB)	SUSPI Debounce Timer [3]	R/W	0
6	SUSPI Debounce Timer [2]	R/W	0
5	SUSPI Debounce Timer [1]	R/W	0
4	SUSPI Debounce Timer [0]	R/W	0
3	FPBL Control Override	R/W	0
2	FPBL Output State	R/W	0
1	FPVCC Control Override	R/W	0
0(LSB)	FPVCC Output State	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit **Description**

7:4 **SUSPI Debounce Timer [3:0]:**
These bits define the number of seconds the input to the SUSPI pin must remain high and stable before the CL-GD7542 enters Suspend mode.

- The SUSPI debounce timer may be set for 1 to 15 seconds.
- A setting of 0000 disables the SUSPI debounce timer.

CR23				Setting for SUSPI Debounce Timer (seconds)
[3]	[2]	[1]	[0]	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	16

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Continued on next page.

6.7.69 CR23: SUSPI Debounce Timer *(cont.)*

Bit	Description
3	**FPBL Control Override:** Setting this bit to 1: • overrides the flat panel backlight (FPBL) Standby mode • enables CR23[2] to control the output state of the flat panel backlight
2	**FPBL Output State:** When CR23[3] = 1, this bit defines the flat panel backlight output state (1 or 0).
1	**FPVCC Control Override:** Setting this bit to 1: • overrides the flat panel VCC (FPVCC) Standby mode • enables CR23[0] to control the output state of the flat panel VCC
0	**FPVCC Output State:** When CR23[1] = 1, this bit defines the flat panel VCC output state (1 or 0).

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6.7.70 CR25: Manufacturing Revision ID Register

I/O Port Address: 3?5

Index: 25

Bit	Description	Reset State
7(MSB)	Manufacturing Revision ID [7]	'MFG revision'
6	Manufacturing Revision ID [6]	'MFG revision'
5	Manufacturing Revision ID [5]	'MFG revision'
4	Manufacturing Revision ID [4]	'MFG revision'
3	Manufacturing Revision ID [3]	'MFG revision'
2	Manufacturing Revision ID [2]	'MFG revision'
1	Manufacturing Revision ID [1]	'MFG revision'
0(LSB)	Manufacturing Revision ID [0]	'MFG revision'

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register is used for factory testing and internal tracking only. Application programs should not use this register.

Bit	Description
7:0	**Manufacturing Revision ID [7:0]:** • These bits are the least-significant eight bits of a ten-bit field that uniquely identifies the CL-GD7542 manufacturing revision level • The most-significant two bits are in CR27[1:0].

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6.7.71 CR27: Device ID and Manufacturing Revision ID Register

I/O Port Address: 3?5

Index: 27

Bit	Description	Reset State
7(MSB)	Device ID [5]	0
6	Device ID [4]	0
5	Device ID [3]	1
4	Device ID [2]	0
3	Device ID [1]	1
2	Device ID [0]	1
1	MFG Revision ID [9]	1
0(LSB)	MFG Revision ID [8]	1

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register will return in bits [7:2] a value that uniquely identifies the CL-GD7542.

Bit	Description
7:2	**Device ID [5:0]:** This five-bit field contains a unique value that identifies the CL-GD7542 as a Cirrus Logic product, according to the code below. The product code ID is given in both hex and binary values.

Product	Corresponding Product Code ID, in CR27[7:2]
CL-GD7542	28h (001011b)

1:0	**Manufacturing Revision ID [9:8]:** • These bits are the two most-significant bits of a ten-bit field that uniquely identifies the CL-GD7542 manufacturing revision level • The least-significant eight bits are in CR25[7:0].

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6.7.72 CR29: CL-GD7542 Configuration Status Register

I/O Port Address: 3?5

Index: 29

Bit	Description	Reset State
7(MSB)	Suspend Mode Status	0
6	32kHz Input Status	0
5	Power-Up/Power-Down Cycling Activity	0
4	Standby Mode Status	0
3	Reserved	
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register identifies the configuration of the memory and bus interface selected for the chip.

Bit	Description
7	**Suspend Mode Status:** • This bit is 1 when the CL-GD7542 is in Suspend mode. This bit remains 1 from the time the clocks are stopped until 32 mseconds after the clocks are restarted, that is, until power-up sequencing is started. • While this bit is 1, the SUSPST# pin output remains low.
6	**32kHz Input Status:** This bit reflects the status of the 32-kHz input clock. • This bit is 1 when the 32-kHz input clock signal is high. • This bit is 0 when the 32-KHz input clock signal is low. • This bit can be used to create a software timer.
5	**Power-Up/Power-Down Cycling Activity:** • This bit is 1 while the CL-GD7542 is going through a power-up or power-down sequence. • This bit can be read in all modes except hardware-controlled Suspend mode, which locks out access to all registers.
4	**Standby Mode Status:** • This bit is 1 when the CL-GD7542 is in Standby mode. This bit remains 1 from the time the clocks are stopped until 32 mseconds after the clocks are restarted, that is, until power-up sequencing is started. • While this bit is 1, the SBYST# pin remains low.
3 0	Reserved

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6.7.73 CR2C: LCD Interface

I/O Port Address: 3?5

Index: 2C

Bit	Description	Reset State
7(MSB)	LCD Class Select [1]	0
6	LCD Class Select [0]	0
5	Write Protect Horizontal-Timing Shadow Registers	0
4	Select Set of Horizontal-Timing Shadow Registers	0
3	Write Protect CRT Controller Registers for LCD Timing	0
2	Reserved	
1	Invert LLCLK	0
0(LSB)	Invert LFS	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit **Description**

7:6 **LCD Class Select [1:0]:**
These two bits select the class of LCD to be connected. The following table lists available choices:

CR2C [7]	CR2C [6]	LCD Class Selected
0	0	Dual-scan monochrome LCD selected if CR2C[7:6] = 00 *and* R8X[5] = 0. Single-scan monochrome LCD selected if CR2C[7:6] = 00 *and* R8X[5] = 1.
0	1	Reserved
1	0	Dual-scan color STN LCD selected if CR2C[7:6] = 10 *and* SR21[6] = 1. Single-scan color STN LCD selected if CR2C[7:6] = 10 *and* SR21[6] = 0.
1	1	TFT-color LCDs selected.

5 **Write Protect Horizontal-Timing Shadow Registers:**

- When this bit is 0:
  - The shadow horizontal timing registers RiY and RiZ (i = 0,2,3,4,5) are write-protected and cannot be accessed.
  - Writing and reading applies only to standard VGA horizontal timing registers.
  - Writing to standard VGA registers alone has no affect on CRTC timing.
- When this bit is 1.
  - Writing is done to both the standard VGA horizontal timing registers and the shadow horizontal timing registers RiY and RiZ (i = 0,2,3,4,5).
  - Reading is done only from the shadow registers.
- To access the standard VGA horizontal timing registers, this bit is a don't care

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6.7.73 CR2C: LCD Interface *(cont.)*

Bit	Description
4	**Select Set of Horizontal-Timing Shadow Registers:** This bit selects which set of horizontal-timing shadow registers the CL-GD7542 uses. When CR2C[5] = 1 *and* this bit: • is 0, it selects registers R0Y to R5Y, used with the normal DCLK. • is 1, it selects registers R0Z to R5Z, used with DCLK ÷ 2. (For information on DCLK ÷ 2, refer to Sequencer Register SR1[3].)
3	**Write Protect CRT Controller Registers for LCD Timing:** For LCD operation, some CRT controller registers must be write protected, that is, the last data bits written are used for CRT controller timing control, and a read/write shadow register is enabled for any subsequent I/O. • When this bit is 1, the CRT Controller registers in the table below are write protected for LCD timing.
2	Reserved
1	**Invert LLCLK:** When this bit is 1, the LLCLK output is inverted.
0	**Invert LFS:** When this bit is 1, the LFS output is inverted.

CRT Controller Register / Bits	Description of CRT Controller Registers That Are Write Protected for LCD Timing
CR6 [7:0]	Vertical Total (Protected value is used.)
CR7 [7, 5, 2, 0]	Vertical Overflow bits for total and sync start
CR10 [7:0]	Vertical Retrace Start (Protected value is used for CRT VSYNC.)
CR11 [7:0]	Vertical Retrace End (Protected value is used for CRT VSYNC.)
CR15 [7:0]	Vertical Blanking Start
CR16 [7:0]	Vertical Blanking End

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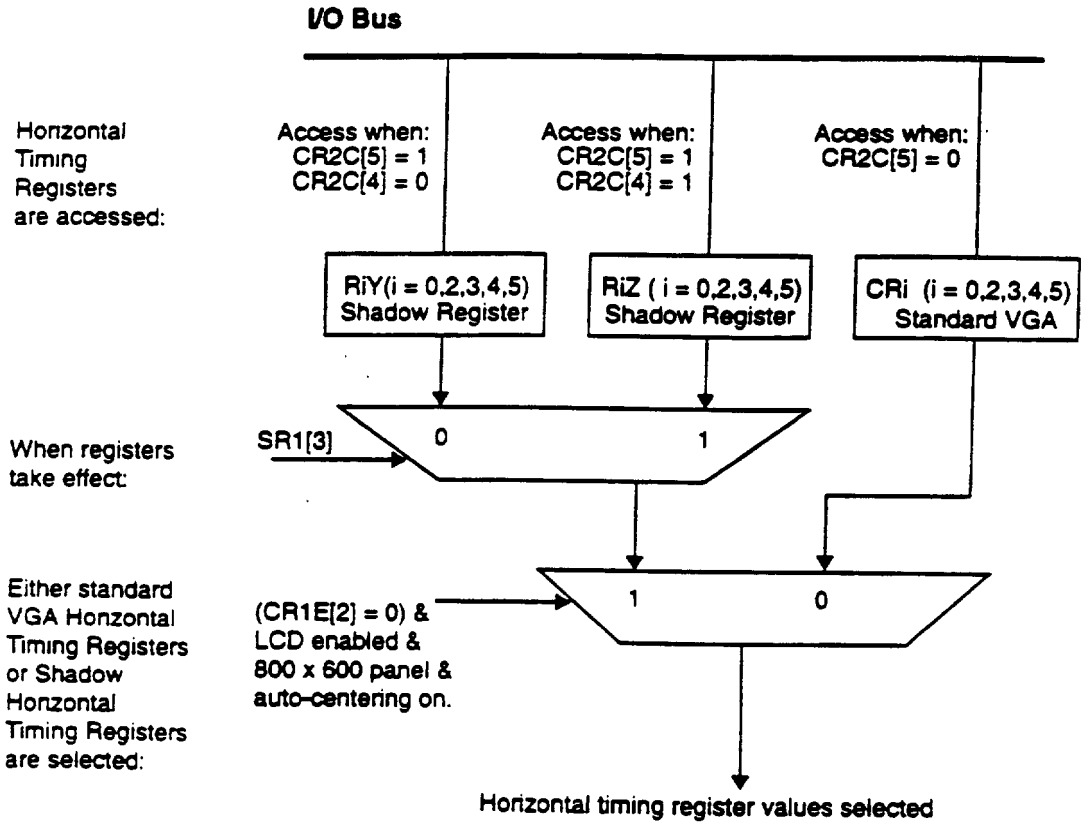


Figure 6–3 Horizontal Timing Register Values Selection

Table 6–7. Horizontal Timing Register References

CRi (Standard VGA) Horizontal (H) Timing Registers		Horizontal (H) Timing Shadow Registers			
		RiY Registers		RiZ Registers	
CR0	H Total	R0Y	H Total	R0Z	H Total
CR2	H Blanking Start	R2Y	H Blanking Start	R2Z	H Blanking Start
CR3	H Blanking End	R3Y	H Blanking End	R3Z	H Blanking End
CR4	H Sync Start	R4Y	H Sync Start	R4Z	H Sync Start
CR5	H Sync End	R5Y	H Sync End	R5Z	H Sync End

6.7.74 CR2D: LCD Display Controls

I/O Port Address: 3?5

Index: 2D

Bit	Description	Reset State
7(MSB)	Enable LCD Timing Registers	0
6	Enable ACTI to Reset Standby Timer	0
5	Enable VGA Access to Reset Standby Timer	0
4	Suspend Mode Clock Source	0
3	Enable ACTI to Reset Backlight Timer	0
2	Enable VGA Access to Reset Backlight Timer	0
1	Enable Vertical Auto-Expand for 640 x 480 LCDs	0
0(LSB)	Enable Auto-Center	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Enable LCD Timing Registers:** • The CRT Controller Index register (CRX) does not have bits to index the LCD timing registers (R2X to REX). Instead, CR2D[7] acts as an extra CRT Controller Index register bit to enable registers R2X to REX. • When this bit is 1, it enables read/write of the hidden LCD Timing Registers, R2X through REX, which are mapped at the standard CRTC locations. These special registers are used to control LLCLK, LFS, and other LCD control signals.
6	**Enable ACTI to Reset Standby Timer:** When this bit is set to 1, activity on the ACTI input pin will reset the internal Standby Timer.
5	**Enable VGA Access to Reset Standby Timer:** When this bit is set to 1, any valid VGA memory access will reset the internal Standby Timer.
4	**Suspend Mode Clock Source:** This bit selects the source for the clock used during Suspend mode. • When this bit is 0, a 32k-Hz clock must be connected to the 32-kHz pin. • When this bit is 0, *and* when the CL-GD7542 is in Suspend mode, the OSC input pin is disabled. • When this bit is set to 1, the 14M-Hz clock, required on the OSC input pin, will be divided by 432 to derive the 32k-Hz clock.
3	**Enable ACTI to Reset Backlight Timer:** When this bit is set to 1, activity on the ACTI input will reset the Backlight control timer for the LCD.
2	**Enable VGA Access to Reset Backlight Timer:** When this bit is set to 1, any valid VGA memory access will reset the Backlight control timer for the LCD.

Continued on next page.

6.7.74 CR2D: LCD Display Controls *(cont.)*

Bit **Description**

1 **Enable Vertical Auto-Expand for 640 x 480 LCDs:**
When this bit is 1, it enables automatic vertical expansion for 640 x 480 LCDs, as controlled by the sync polarity bits in External/General Register MISC[7:6].

MISC [7]	MISC [6]	Automatic Vertical Expansion
0	0	In CL-GD7542, used for 800 x 600 LCDs with more than 480 lines. Reserved in standard VGA.
0	1	400-line/200-line modes. 400-line mode is for text only. 200-line mode is for double-scanned graphics only.
1	0	350-line modes (text or graphics)
1	1	480-line mode (graphics only, no vertical expansion)

Expansion Method For Graphics Modes:

Original Number of Lines	Expansion Method for Graphics Modes
200	Pattern used is double-scan and triple-scan: 2,2,3,2,2,3,2,3 This pattern expands 200 lines to 475 lines by expanding every 8 lines to 19.
350	Pattern used is single-scan and double-scan: 1,1,2,1,1,2,1,2,1,1,2,1,1,2. This pattern expands 350 lines to 475 lines by expanding every 14 lines to 19.

Expansion Method For Text Modes:

Original Lines/ Font	Expansion Method for Text Modes
200 lines, 8 x 8 font	Normal double-scan is applied. An extra top line and 2 extra bottom lines are added to each character row (only when maximum row scan is set for 7 lines).
350 lines, 8 x 14 font	An extra 2 top lines and 3 extra bottom lines are added to each character row (only when maximum row scan is set for 14 lines).
400 lines, 8 x 16 font	An extra top line and 2 extra bottom lines are added to each character row (only when maximum row scan is set for 16 lines).

0 **Enable Auto-Center:**
When this bit is 1, and when auto-expand bit CR2D[1] is 0 (based on sync polarities), it enables LCD auto-centering. This action uses alternate LFS (Line-Frame Start) timing as programmed in LCD Timing registers R2X through REX.

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6.7.75 CR2E: High-Resolution LCD Control Register

I/O Port Address: 3?5

Index: 2E

Bit	Description	Reset State
7(MSB)	Expansion Select Override [1]	0
6	Expansion Select Override [0]	0
5	Horizontal Centering for 800 x 600 LCDs	0
4	10-Dot True Fonts	0
3	Horizontal Graphics Expansion for 800 x 600 LCDs	0
2	Horizontal Font Expansion for 800 x 600 LCDs	0
1	Vertical Graphics Expansion for 800 x 600 LCDs	0
0(LSB)	Text Expansion for 800 x 600 LCDs	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:6	**Expansion Select Override [1:0]:** • When these bits are 00, graphics expansion is controlled by CR2E[3,1]. • When these bits are 01, *and* R9X[3:2] bits are 01, an 800 x 600 LCD display size is selected. However, graphics expansion is disabled, even when bits CR2E[3,1] are set to 1. • Bit values 10 and 11 are reserved for future use.
5	**Horizontal Centering for 800 x 600 LCDs:** When this bit is 1, horizontal centering is enabled on 800 x 600 LCDs.
4	**10-Dot True Fonts:** When this bit is 1, and a text mode is selected, 10-dot true fonts are selected.
3	**Horizontal Graphics Expansion for 800 x 600 LCDs:** When this bit is 1, and a graphics mode is selected, horizontal graphics expansion is enabled, which replicates every fourth pixel. • For an 800 x 600 LCD, this bit is used to expand 640-pixel data of each scanline to 800-pixel data. • This bit does not work in 16-bit/pixel and 24-bit/pixel modes.
2	**Horizontal Font Expansion for 800 x 600 LCDs:** When this bit is 1, and a text mode is selected, 8-dot-wide true fonts are expanded to 10 dots wide (instead of the normal 9-dot-wide VGA expansion).
1	**Vertical Graphics Expansion for 800 x 600 LCDs:** When this bit is 1, and a graphics mode is selected, vertical graphics on 800 x 600 LCDs are expanded by: • doubling every odd scanline in 350-line and 400-line modes • replicating every fourth scanline in 480-line mode
0	**Text Expansion for 800 x 600 LCDs:** When this bit is 1, and a text mode is selected, the text font is expanded by: • doubling every odd scanline for 9 x 14 fonts or 8 x 16 fonts • tripling every scanline for 8 x 8 fonts

6.7.76 CR2F: Driver and BIOS Revision Register

I/O Port Address: 3?5

Index: 2F

Bit	Description	Reset State
7(MSB)	Driver Revision [3]	'Driver Revision'
6	Driver Revision [2]	'Driver Revision'
5	Driver Revision [1]	'Driver Revision'
4	Driver Revision [0]	'Driver Revision'
3	BIOS Revision [3]	'BIOS Revision'
2	BIOS Revision [2]	'BIOS Revision'
1	BIOS Revision [1]	'BIOS Revision'
0(LSB)	BIOS Revision [0]	'BIOS Revision'

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register will return two 4-bit codes that uniquely identifies the CL-GD7542 to drivers and to the BIOS.

Bit	Description
7:4	**Drivers Revision [3:0]:** This 4-bit field contains a 4-bit value that identifies the CL-GD7542 to various software drivers.
3:0	**BIOS Revision [3:0]:** This 4-bit field contains a 4-bit value that identifies the CL-GD7542 to the video BIOS.

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6.7.77 CR30: TV-OUT Control Register

I/O Port Address: 3?5

Index: 30

Bit	Description	Reset State
7(MSB)	PROG Pin-Level Control	0
6	Reserved	
5	Horizontal Total Dot-Clock Delay Control [1]	0
4	Horizontal Total Dot-Clock Delay Control [0]	0
3	TV-OUT Mode Enable	0
2	NTSC / PAL Output Control	0
1	CSYNC Dot-Clock Delay Control [1]	0
0(LSB)	CSYNC Dot-Clock Delay Control [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**PROG Pin-Level Control:** This bit controls the logic level on the CL-GD7542 PROG output pin. When this bit is: • a 1, the PROG pin level is high. • a 0, the PROG pin level is low.
6	Reserved
5:4	**Horizontal Total Dot-Clock Delay Control [1:0]:** The value in these bits control the dot-clock delay for the horizontal total signal according to the following table:

CR30		Dot-Clock Delay
[5]	[4]	
0	0	No Delay
0	1	Delay = 2 Dot Clocks
1	0	Delay = 4 Dot Clocks
1	1	Delay = 6 Dot Clocks

3	**TV-OUT Mode Enable:** • When this bit is 1, the TV-OUT mode is enabled, and TVON output is high. • When this bit is 0, the NTSC/PAL, CSYNC, and TVON outputs are all forced low, and CR30[2] is disabled. • When Extension Register External RAMDAC Address / Chip Select Enable SR25[6] = 1, the TVON pin is not controlled by CR30[3]. However, the TV-OUT feature can still be used without a power-down feature on CR30[3].

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6.7.77 CR30: TV-OUT Control Register *(Cont.)*

Bit	Description
2	**NTSC / PAL Output Control:** This bit is programmed to reflect the required input levels to the NTSC/PAL encoder. When CR30[3]: • is 0, this bit is disabled. • is 1, *and* this bit: — is 0, this bit creates a low on the NTSC/PAL output pin. — is 1, this bit creates a high on the NTSC/PAL output pin
1:0	**CSYNC Dot-Clock Delay Control [1:0]:** The value in these bits control the dot-clock delay for the generation of a composite synchronization signal (CSYNC) according to the following table.

CR30		Horizontal CSYNC Start
[1]	[0]	
0	0	No Delay
0	1	Delay = 2 Dot Clocks
1	0	Delay = 4 Dot Clocks
1	1	Delay = 6 Dot Clocks

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6.7.78 CR33: MotionVideo™ Window Horizontal Start (XS) / Width (XW) Overflow

I/O Port Address: 3?5

Index: 33

Bit	Description	Reset State
7(MSB)	Reserved	0
6	MVW Horizontal Start (XS) [9]	0
5	MVW Horizontal Start (XS) [8]	0
4	Reserved	
3	MVW Horizontal Start (XW) [9]	0
2	MVW Horizontal Start (XW) [8]	0
1	Reserved	
0(LSB)	Enable Fast MVA FIFO Request	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

In the MVW (MotionVideo™ Window) architecture, the horizontal position is programmed using the number of memory cycles used by the surrounding pixel depth number environment.

Bit	Description
7	Reserved
6:5	**MVW Horizontal Start (XS) [9:8]:** These are the most-significant two bits of a ten-bit field that defines the horizontal starting position of the MotionVideo™ Window. For details, refer to Extension Register CR34.
4	Reserved
3.2	**MVW Horizontal Start (XW) [9:8]:** These are the most-significant two bits of a ten-bit field that defines the horizontal width of the MotionVideo™ Window. For details, refer to Extension Register CR35.
1	Reserved
0	**Enable Fast MVA FIFO Request:** This bit enables bypassing the synchronizer in the MotionVideo™ Window Architecture (MVA) circuitry to fill the FIFO faster.

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6.7.79 CR34: MotionVideo™ Window Horizontal Start (XS) Register

I/O Port Address: 3?5

Index: 34

Bit	Description	Reset State
7(MSB)	MVW Horizontal Start (XS) [7]	0
6	MVW Horizontal Start (XS) [6]	0
5	MVW Horizontal Start (XS) [5]	0
4	MVW Horizontal Start (XS) [4]	0
3	MVW Horizontal Start (XS) [3]	0
2	MVW Horizontal Start (XS) [2]	0
1	MVW Horizontal Start (XS) [1]	0
0(LSB)	MVW Horizontal Start (XS) [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

In the MVW (MotionVideo™ Window), the starting horizontal position is programmed by using the number of memory fetch cycles in the surrounding pixel-depth environment.

Bit	Description
7:0	**MVW Horizontal-Start (XS) [7:0]:** • These eight bits are the least-significant bits of a ten-bit field. • CR33[6:5] are the most-significant two bits of this field. To program XS, the horizontal coordinate to start the MVW on the screen: • Determine the number of the pixel at which the MVW will start. • Determine the surrounding pixel-depth environment, in bits per pixel. • Determine the size of the memory bus, which determines how many bits each memory fetch cycle transfers. • Obtain the number of pixels per memory fetch cycle by dividing the size of the memory bus by the number of bits in the surrounding pixel-depth environment. (If the memory bus is 32 bits wide, and 4 bits per pixel is used for the surrounding pixel-depth environment, then the number of pixels per memory fetch cycle is 8.) • Divide the number of the pixel at which the MVW will start by the number of pixels per memory fetch cycle. • Program the resulting value into CR34[7:0]. For example. If A MVW is to start at pixel 16. The surrounding pixel-depth environment is 4 bits per pixel. The memory bus transfers 32 bits (32-bit memory fetch cycle). Then The number of pixels per memory fetch cycle is 32 ÷ 4 = 8 . The number of memory fetch cycles needed for a MWV starting at pixel 16 will be 2. (Starting MVW value pixel number 16 ÷ 8 pixels per memory fetch cycle = 2 memory fetch cycles.) Program into CR34[7:0] the value 2 as the number of memory fetch cycles needed for a MVW starting at pixel 16.

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0 CR35: MotionVideo™ Window Horizontal Width (XW) Register

I/O Port Address: 3?5

Index: 35

Bit	Description	Reset State
7(MSB)	MVW Horizontal Width (XW) [7]	0
6	MVW Horizontal Width (XW) [6]	0
5	MVW Horizontal Width (XW) [5]	0
4	MVW Horizontal Width (XW) [4]	0
3	MVW Horizontal Width (XW) [3]	0
2	MVW Horizontal Width (XW) [2]	0
1	MVW Horizontal Width (XW) [1]	0
0(LSB)	MVW Horizontal Width (XW) [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

In the MVW (MotionVideo™ Window) architecture, the horizontal width of the MVW is calculated in memory fetch cycles, as explained below.

Bit	Description
7:0	**MVW Horizontal Width (XW) [7:0]:** • These eight bits are the least-significant bits of a ten-bit field. This field must be programmed for the MVW, even when the MVW is displayed on the full screen. • The most-significant bits of this field are in CR33[3:2]. To program the number of memory fetch cycles needed for the value of XW, the horizontal width: • Determine the panel's width in pixels. • Determine the color depth of the MVW display, in bits per pixel. • Determine the size of the memory bus, which determines how many bits each memory fetch cycle transfers. • Multiply the panel's width in pixels times the pixel depth. • Divide the above quantity by the number of bits each memory fetch cycle transfers. • Program the resulting value into CR35[7:0]. For example, if a panel is 320 pixels wide, the MVW display has a color depth of 16 bits per pixel, and the memory bus transfers 32 bits (32-bit memory fetch cycle) then in memory fetch cycles, the MVW horizontal width is 160. [(320 pixels) x (16 bits/pixel)] ÷ [32 bits/memory fetch cycle] = 160 memory fetch cycles, which is the number to program into CR35[7:0].

EX

6.7

Provided by the Department of Defense

6.7.81 CR36: YUV-to-RGB Conversion and MVW Vertical-Position High Register

I/O Port Address: 3?5

Index: 36

Bit	Description	Reset State
7(MSB)	Force Linear Display Memory Map	0
6	Convert YUV to RGB with Standard Algorithm or Other	0
5	Convert YUV to RGB with Excess 128 or 2's Complement	0
4	MVW Memory-Address Offset [8]	0
3	MVW Vertical End (YE) Position [9]	0
2	MVW Vertical End (YE) Position [8]	0
1	MVW Vertical Start (YS) Position [9]	0
0(LSB)	MVW Vertical Start (YS) Position [8]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Force Linear Display Memory Map:** This bit is used to simplify the use of MVA drivers by providing a unique way of accessing the memory for MVW, from the CPU side. • When this bit is 1, the CPU linearly writes data to the display memory, the same way as in extended 8-bit-per-pixel packed-pixel modes. • Set this bit to 1, when writing to MVW memory and running Microsoft® Windows in 4-bit-per-pixel planar mode, to ensure that writes to MVW memory execute independently of surrounding graphics. • After executing writes to the MVW memory area, the Windows driver must set this bit to 0.
6	**Convert YUV to RGB with Standard Algorithm or Other:** • When this bit is 1, the YUV-to-RGB conversion uses the algorithm. R = Y + V; G = Y - 0.25U - 0.5V; B = Y + U • When this bit is 0, the YUV-to-RGB conversion uses the standard algorithm R = Y+ 1.375V; G = Y-.375U-.75V; B = Y+1.75U
5	**Convert YUV to RGB with Excess 128 or 2's Complement:** These conversions assume that U and V are expressed in either excess 128 or 2's complement notation • When this bit is 1, the YUV-to-RGB conversion uses excess 128 notation. • When this bit is 0, the YUV-to-RGB conversion uses the 2's complement notation (that is, Philips SAA15B and SAA9051 TV decoders).
4	**MVW Memory-Address Offset [8]:** This is the most-significant bit of the MVW Memory-Address Offset Register CR3B
3 2	**MVW Vertical End (YE) Position [9:8]:** These are the most-significant bits of the MVW Vertical End Register CR38.
1 0	**MVW Vertical Start (YS) Position [9:8]:** These are the most-significant bits of the MVW Vertical Start Register CR37.

6.7.82 CR37: MVW Vertical Start (YS) Position Register

I/O Port Address: 3?5

Index: 37

Bit	Description	Reset State
7(MSB)	MVW Vertical Start (YS) Position [7]	0
6	MVW Vertical Start (YS) Position [6]	0
5	MVW Vertical Start (YS) Position [5]	0
4	MVW Vertical Start (YS) Position [4]	0
3	MVW Vertical Start (YS) Position [3]	0
2	MVW Vertical Start (YS) Position [2]	0
1	MVW Vertical Start (YS) Position [1]	0
0(LSB)	MVW Vertical Start (YS) Position [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**MVW Vertical Start (YS) Position [7:0]:** • These are the 8 least-significant bits of the 10-bit field for the MVW Vertical Start (YS) Position. • The ten bits of this field: — define actual scanlines — are not affected by scanline doubling or LCD vertical expansion • The most-significant two bits are in register CR36[1:0].

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6.7.83 CR38: MVW Vertical End (YE) Position Register

I/O Port Address: 3?5

Index: 38

Bit	Description	Reset State
7(MSB)	MVW Vertical End (YE) Position [7]	0
6	MVW Vertical End (YE) Position [6]	0
5	MVW Vertical End (YE) Position [5]	0
4	MVW Vertical End (YE) Position [4]	0
3	MVW Vertical End (YE) Position [3]	0
2	MVW Vertical End (YE) Position [2]	0
1	MVW Vertical End (YE) Position [1]	0
0(LSB)	MVW Vertical End (YE) Position [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**MVW Vertical End (YE) Position [7:0]:** • These are the 8 least-significant bits of the 10-bit field for the MVW Vertical End (YE) Position. • The ten bits of this field: — define actual scanline — are not affected by scanline doubling or LCD vertical expansion • The most-significant two bits are in register CR36[3:2].

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6.7.84 CR39: MVW Surrounding-Address Offset Register

I/O Port Address: 3?5

Index: 39

Bit	Description	Reset State
7(MSB)	MVW Surrounding-Address Offset [7]	0
6	MVW Surrounding-Address Offset [6]	0
5	MVW Surrounding-Address Offset [5]	0
4	MVW Surrounding-Address Offset [4]	0
3	MVW Surrounding-Address Offset [3]	0
2	MVW Surrounding-Address Offset [2]	0
1	MVW Surrounding-Address Offset [1]	0
0(LSB)	MVW Surrounding-Address Offset [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines a value that is added to the CRT address counter of the display, so the counter value skips over the MotionVideo™ Window. This action allows the surrounding restart address to be defined without having to count through MVW.

Bit	Description
7:0	**MVW Surrounding-Address Offset [7:0]:** • The offset value in this register is added to the CRT address counter to allow the counter to skip over the area for the MotionVideo™ Window without having to count through it. • This offset value depends on the resolution of the surrounding mode. For example: Assume a scanline of 1024 pixels, and 8 bits/pixel (4 pixels/address). As a result, the largest offset value is 256 addresses. • To obtain a desired address offset, program this register for one-half of the desired offset. Example. Assume a 320-pixel-wide window with a surrounding resolution of 4 bits/ pixel — A memory fetch has 8 pixels. — 320 pixels ÷ 8 pixels/address = 40-address offset — One-half of 40 is 20 decimal — As a result, program 14h for the surrounding-address offset.

6.7.85 CR3A: MVW Memory-Address Start Register

I/O Port Address: 3?5

Index: 3A

Bit	Description	Reset State
7(MSB)	Reserved	
6	MVW Memory-Address Start [6]	0
5	MVW Memory-Address Start [5]	0
4	MVW Memory-Address Start [4]	0
3	MVW Memory-Address Start [3]	0
2	MVW Memory-Address Start [2]	0
1	MVW Memory-Address Start [1]	0
0(LSB)	MVW Memory-Address Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	Reserved
6:0	**MVW Memory-Address Start [6:0]:** This address is programmed in increments of 16 Kbytes (4K words). For example: • For 1 Mbyte, the physical address is 00000:3FFF F from the start of display memory. • For 2 Mbytes, the physical address is 00000:7FFF F from the start of display memory. Note: This start address must be aligned at a 16-Kbyte boundary in the CPU host address space.

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6.7.86 CR3B: MVW Memory-Address Offset Register

I/O Port Address: 3?5

Index: 3B

Bit	Description	Reset State
7(MSB)	MVW Memory-Address Offset [7]	0
6	MVW Memory-Address Offset [6]	0
5	MVW Memory-Address Offset [5]	0
4	MVW Memory-Address Offset [4]	0
3	MVW Memory-Address Offset [3]	0
2	MVW Memory-Address Offset [2]	0
1	MVW Memory-Address Offset [1]	0
0(LSB)	MVW Memory-Address Offset [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, along with the most-significant bit in CR36[4], defines an offset value.

Bit	Description
7:0	**MVW Memory-Address Offset [7:0]:** • These are the 8 least-significant bits of the 9-bit MVW memory-address offset value. This offset value is added to the present MVW Memory Start Address to get the next MVW Memory-Start Address. ADD: Present MVW Memory-Start Address AND: + MVW Memory-Address Offset (9-bit value) TO GET: = Next MVW Memory-Start Address • Using the MVW Memory-Address Offset to define the next memory-start address of the MVW allows panning through a large area of the MVW. The actual image stored in memory may be as large as 2K pixels at 16 bits/pixel. • The most-significant bit is in register CR36[4].

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6.7.87 CR3C: MVW Zoom, MVW Enable, and MVW Encoding Format Register

I/O Port Address: 3?5

Index: 3C

Bit	Description	Reset State
7(MSB)	MVW Horizontal Zoom	0
6	MVW Vertical Zoom	0
5	Full-Screen Live-Video Enable	0
4	MotionVideo™ Window Enable	0
3	Encoding Format for MotionVideo™ Window [3]	0
2	Encoding Format for MotionVideo™ Window [2]	0
1	Encoding Format for MotionVideo™ Window [1]	0
0(LSB)	Encoding Format for MotionVideo™ Window [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**MVW Horizontal Zoom:** When this bit is 1, each pixel is duplicated horizontally.
6	**MVW Vertical Zoom:** When this bit is 1, each pixel is duplicated vertically.
5	**Full-Screen Live-Video Enable:** When this bit is 1, the entire screen displays live video.
4	**MotionVideo™ Window Enable:** When this bit is 1, access is enabled to the MotionVideo™ Window registers CR33 through CR3B.
3:0	**Encoding Format for MotionVideo™ Window:** These bits define in which format the MVW is encoded.

CR3C[3:0]		Encoding Format for MVW
0h	0000	8-bit RGB 3:3:2 (data go through the palette RAMDAC)
1h	0001	16-bit RGB (5:5:5)
2h	0010	16-bit RGB XGA (5:6:5)
3h	0011	4 2.2 YUV Y0UY1V
4h	0100	4 1 1 YUV Linear Y0Y1Y2Y3UV
5h	0101	4 1 1 YUV Array Y0Y1Y2Y3UV, but Y2Y3 are in next scanline
8h	1000	24-bit RGB through MVA™
9h to 15h	1001 to 1111	Reserved for future formats

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6.7.88 CR3D: MotionVideo™ Window Horizontal-Pixel-Width Register

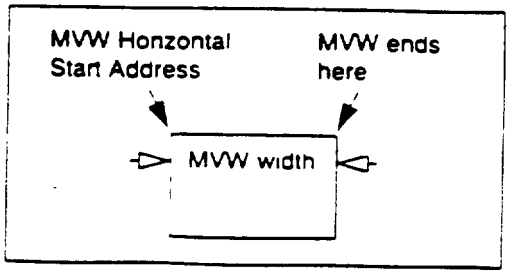
I/O Port Address: 3?5

Index: 3D

Bit	Description	Reset State
7(MSB)	Reserved	
6	MotionVideo™ Window Horizontal Pixel Width [6]	0
5	MotionVideo™ Window Horizontal Pixel Width [5]	0
4	MotionVideo™ Window Horizontal Pixel Width [4]	0
3	MotionVideo™ Window Horizontal Pixel Width [3]	0
2	MotionVideo™ Window Horizontal Pixel Width [2]	0
1	MotionVideo™ Window Horizontal Pixel Width [1]	0
0(LSB)	MotionVideo™ Window Horizontal Pixel Width [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	Reserved
6:0	**MotionVideo™ Window Horizontal Pixel Width [6:0]:** These bits contain a hex value used to define the MotionVideo™ Window width for each scanline the MVW is enabled. To calculate the value: • Determine the MVW's desired width, which must be at least 32 pixels wide. • From the desired width, subtract 24 pixels (three sets of eight pixels). • Divide the resulting number by 8-pixel increments. • Translate the resulting decimal number into a hex number. For example, to calculate the hex value for a 320-pixel wide MVW: DIVIDE: The quantity (320 pixels - 24 pixels = 296 pixels) BY: ÷ 8-pixel increments TO GET: = Value for a 320-pixel-wide MVW, which = 37 (decimal) = 25h Note For CL-GD7542 version BC or later, the MVW width will be able to be expressed in 2-pixel increments.



LCD Display with MotionVideo Window

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6.7.89 CR40: LCD Horizontal-Display-Enable Start Register – No Centering

I/O Port Address: 3?5

Index: 40

Bit	Description	Reset State
7(MSB)	LCD HDE Start [7]	0
6	LCD HDE Start [6]	0
5	LCD HDE Start [5]	0
4	LCD HDE Start [4]	0
3	LCD HDE Start [3]	0
2	LCD HDE Start [2]	0
1	LCD HDE Start [1]	0
0(LSB)	LCD HDE Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of four registers – CR40, CR41, CR42, and CR43 – used both to generate LCD horizontal timing and to center 640 x 480 and 800 x 600 LCDs.

Three registers – CR40, CR41, and CR42 – are complementary and mutually exclusive. They store the same timing-signal parameters, but values for the timing-signal parameters are usually different.

- Only one of these three registers is enabled at any time.
- The selection of which of these three registers control the LCD is done automatically, based on the conditions explained for each register.
- These three registers are generally programmed only once at power-on self-test.

The CR40 register is the default LCD HDE start register. The CL-GD7542 automatically selects it if:

- either CR41 or CR42 *are not* selected, or
- horizontal expansion *is* selected

In normal 24-bit LCD modes, the CL-GD7542 starts to send data to the LCD immediately after HDE start, which may cause problems for some graphics modes. These three registers may be programmed to avoid the problems.

For typical timing relationships, refer to Figure 6–4.

Continued on next page

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6.7.89 CR40: LCD Horizontal-Display-Enable Start Register – No Centering *(Cont.)*

Bit	Description
7:0	**LCD HDE Start [7:0]:** When no horizontal centering is needed, this register defines: • LCD HDE start, the rising edge of the LCD horizontal display enable signal, relative to the previous CRT HDE start. • LLCLK, the rising edge of the LCD line clock signal, which starts one DCLK (dot clock) after the LCD HDE start. The LCD HDE start is expressed in 4-DCLK units, with CR43[1:0] defining a fine adjustment in 1-DCLK units. To calculate the LCD HDE start: DIVIDE: [(Number of CRT Horizontal Total pixels) minus 32 pixels BY: ÷ 4 (Number of 4-DCLK units) TO GET: = LCD HDE Start where Horizontal Total = CRT horizontal total in DCLK units. For example, for a 640 x 480 CRT, Horizontal Total = 800. LCD Line-Clock Start and the LCD HDE start signal for both 640 x 480 and 800 x 600 LCDs. A fine (dot-clock) adjustment for this register is in CR43[1:0].

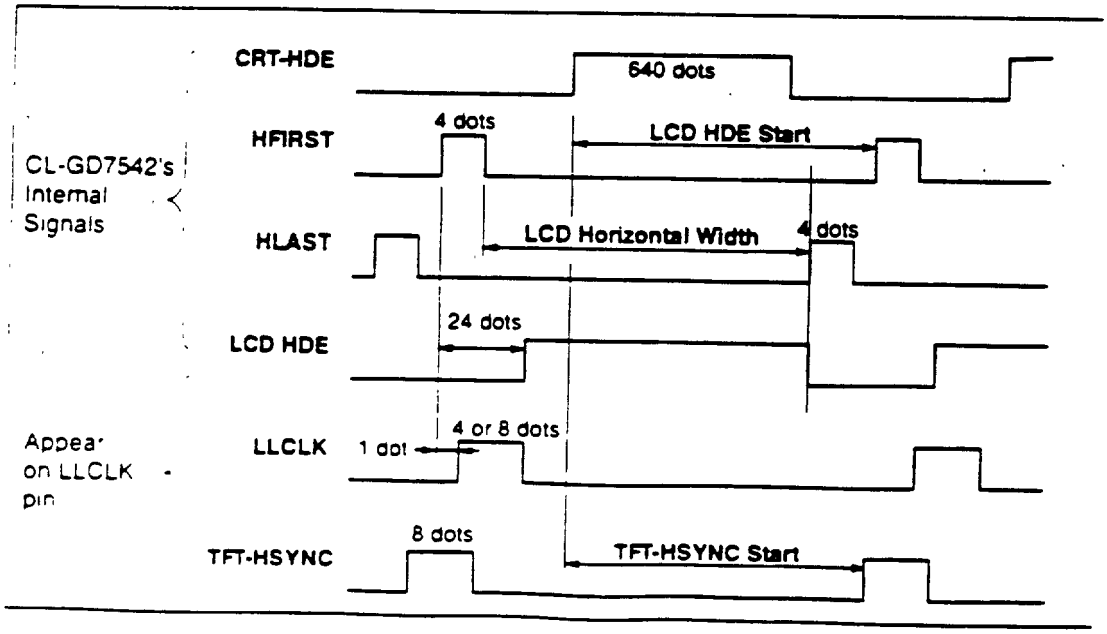


Figure 6–4 Horizontal Timing for 800 x 600 LCD Displaying 640 x 480 Picture

6.7.90 CR41: LCD Horizontal-Display-Enable Start to Center 720-Dot Display

I/O Port Address: 3?5

Index: 41

Bit	Description	Reset State
7(MSB)	LCD HDE Start to Center 720-Dot Display [7]	0
6	LCD HDE Start to Center 720-Dot Display [6]	0
5	LCD HDE Start to Center 720-Dot Display [5]	0
4	LCD HDE Start to Center 720-Dot Display [4]	0
3	LCD HDE Start to Center 720-Dot Display [3]	0
2	LCD HDE Start to Center 720-Dot Display [2]	0
1	LCD HDE Start to Center 720-Dot Display [1]	0
0(LSB)	LCD HDE Start to Center 720-Dot Display [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of four registers – CR40, CR41, CR42, and CR43 – used both to generate LCD horizontal timing and to center 640 x 480 and 800 x 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

The CL-GD7542 automatically uses this register to provide centering of a 720-dot display (text or graphics) when all the following conditions are met:

- The LCD is an 800 x 600.
- The LCD is not using 800 x 600 graphics modes.
- The LCD is using a character clock of 9-DCLK cycles (in text mode), or CRT HDE > 50h (in graphics mode).
- The LCD is not using horizontal expansion.

Bit	Description
7:0	**LCD HDE Start to Center 720-Dot Display [7:0]:** This register provides centering of a 720-dot display (text or RiX graphics mode) on a 800 x 600 LCD by defining the present LCD HDE start signal. • This register defines the present HDE start signal, relative to the previous HDE start signal, in 4-DCLK increments. (The DCLK is never divided by two.) • The value programmed in this register is in 4-DCLK increments, and this value is one less than the HDE start parameter. • On a 800 x 600 LCD, the value in this register defines both the LCD line-clock start and the LCD HDE start signals. A fine adjustment for this register is in CR43[3:2]. • When horizontal expansion is enabled, instead of using this register to define the LCD HDE start signal, the value in CR40 is used to define the LCD HDE start signal

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6.7.91 CR42: LCD Horizontal-Display-Enable Start to Center 640-Dot Display

I/O Port Address: 3?5

Index: 42

Bit	Description	Reset State
7(MSB)	LCD HDE Start to Center 640-Dot Display [7]	0
6	LCD HDE Start to Center 640-Dot Display [6]	0
5	LCD HDE Start to Center 640-Dot Display [5]	0
4	LCD HDE Start to Center 640-Dot Display [4]	0
3	LCD HDE Start to Center 640-Dot Display [3]	0
2	LCD HDE Start to Center 640-Dot Display [2]	0
1	LCD HDE Start to Center 640-Dot Display [1]	0
0(LSB)	LCD HDE Start to Center 640-Dot Display [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of four registers – CR40, CR41, CR42, and CR43 – used both to generate LCD horizontal timing and to center 640 x 480 and 800 x 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

The CL-GD7542 automatically uses this register to provide centering of a 640-dot display (text or graphics) when all the following conditions are met:

- The LCD is an 800 x 600.
- The LCD is not using 800 x 600 graphics modes.
- The LCD is using a character clock of 8-DCLK cycles, and CRT HDE ≤ 50h.
- The LCD is not using horizontal expansion.

Bit	Description
7:0	**LCD HDE Start to Center 640-Dot Display [7:0]:** This register provides centering of a 640-dot display on a 800 x 600 LCD by defining the present LCD HDE start signal. • This register defines the present HDE start signal, relative to the previous HDE start signal, in 4-DCLK increments. (The DCLK is never divided by two.) • The value programmed in this register is in 4-DCLK increments, and this value is one less than the HDE start parameter. • On a 800 x 600 LCD, the value in this register defines both the LCD line-clock start and the LCD HDE start signals. A fine adjustment for this register is in CR43[5:4]. • When horizontal expansion is enabled, instead of using this register to define the LCD HDE start signal, the value in CR40 is used to define the LCD HDE start signal.

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6.7.92 CR43: LCD Dot-Clock-Delay Control Register

I/O Port Address: 3?5

Index: 43

Bit	Description	Reset State
7(MSB)	LCD Line-Clock Width [1]	0
6	LCD Line-Clock Width [0]	0
5	CR42 Fine Dot-Clock Delay [1]	0
4	CR42 Fine Dot-Clock Delay [0]	0
3	CR41 Fine Dot-Clock Delay [1]	0
2	CR41 Fine Dot-Clock Delay [0]	0
1	CR40 Fine Dot-Clock Delay [1]	0
0(LSB)	CR40 Fine Dot-Clock Delay [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of four registers – CR40, CR41, CR42, and CR43 – used both to generate LCD horizontal timing and to center 640 x 480 and 800 x 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

Bits [7:6] set the LCD line clock width.

Bits [5:0] make up three fields that when required, compensate for the CL-GD7542's internal delays of the LCD horizontal display enable (HDE) start signal.

- For the different types of LCDs, these three fields make it possible to change the LCD horizontal display enable (HDE) start by adjusting the fine dot-clock delay in 1-DCLK units.
- When it is necessary to change the LCD horizontal display enable (HDE) start, automatic switching takes place between these three fields. The switching is based on the following:
  - — values in the CRT controller registers
  - — value in the sequencer registers
  - — the type of LCD used (that is, 640 x 480 or 800 x 600)

Note Because LCD counters are reset 1 dot clock after resetting the CRT HDE Total counter, values in LCD registers must be programmed with a delay of one less than the model.

Bit	Description
7 6	**LCD Line-Clock Width [1:0]:** This two-bit field sets the LCK line-clock width in dot clocks, as shown in the following table

CR43 [7]	CR43 [6]	LCD Line-Clock Width (in dot clocks)
0	0	4 dot clocks
0	1	8 dot clocks
1	0	Reserved
1	1	Reserved

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6.7.92 CR43: LCD Dot-Clock Delay-Control Register *(Cont.)*

Bit	Description
5:4	**CR42 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 6–8.
3:2	**CR41 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 6–8.
1:0	**CR40 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 6–8.

Table 6–8. Fine Dot-Clock Delay Options for LCD HDE Start Signals

CR43		Fine Dot-Clock Delay for:
[5]	[4]	CR42
[3]	[2]	CR41
[1]	[0]	CR40
0	0	No Delay
0	1	Delay LCD HDE Start by one DCLK
1	0	Delay LCD HDE Start by two DCLKs
1	1	Delay LCD HDE Start by three DCLKs

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6.7.93 CR44: LCD Horizontal Display Width Register

I/O Port Address: 3?5

Index: 44

Bit	Description	Reset State
7(MSB)	LCD Horizontal Display Width [7]	0
6	LCD Horizontal Display Width [6]	0
5	LCD Horizontal Display Width [5]	0
4	LCD Horizontal Display Width [4]	0
3	LCD Horizontal Display Width [3]	0
2	LCD Horizontal Display Width [2]	0
1	LCD Horizontal Display Width [1]	0
0(LSB)	LCD Horizontal Display Width [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines the LCD horizontal width.

Bit	Description
7:0	**LCD Horizontal Display Width [7:0]:** The value programmed in this register: • defines the LCD horizontal display width, which can be different from the stored picture width. • is used to compensate for internal delays when displaying a narrow picture on a wide screen. • is never expressed in units of DCLK ÷ 2. • is the desired width (expressed in 4 DCLK increments), plus four, all expressed in hex. — For example, for a 640 (horizontal) x 480 (vertical) LCD, program A4h. — When the width of 640 is expressed in 4 DCLK increments = 640 ÷ 4 = 160, the desired width in 4 DCLK increments. — Desired width of 160, plus 4 = 164 decimal. — In hex, 164 decimal = A4 hex.

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6.7.94 CR47: TFT HSYNC Horizontal Start Position Register

I/O Port Address: 3?5

Index: 47

Bit	Description	Reset State
7(MSB)	TFT HSYNC Horizontal Start Position [7]	0
6	TFT HSYNC Horizontal Start Position [6]	0
5	TFT HSYNC Horizontal Start Position [5]	0
4	TFT HSYNC Horizontal Start Position [4]	0
3	TFT HSYNC Horizontal Start Position [3]	0
2	TFT HSYNC Horizontal Start Position [2]	0
1	TFT HSYNC Horizontal Start Position [1]	0
0(LSB)	TFT HSYNC Horizontal Start Position [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines the start of the TFT HSYNC signal. This register is not dependent on character-clock width or DCLK/2 control.

Bit	Description
7:0	**TFT HSYNC Horizontal Start Position [7:0]:** This register defines the exact starting position of the TFT HSYNC signal. The TFT HSYNC Horizontal Start Position: • is relative to the previous LCD CRT horizontal display enable (HDE) start, in DCLK/4 increments. • is about 144 dot clocks before the start of the LCD HDE start signal, which is also relative to the CRT HDE start. • can be adjusted in 1-DCLK increments with CR48[1:0] • When R7X[2] = 1, . — the TFT HSYNC signal, instead of the LLCLK signal, appears on the LLCLK pin. (The LLCLK signal always starts 1 DCLK after the LCD HDE start.) — This setup is needed to support TFT LCDs that require 144 dot clocks between LLCLK and the first shift clock on a scanline. Note: Some LCD manufacturers call the LLCLK signal HSYNC. Cirrus Logic calls this signal TFT HSYNC, to differentiate it from the CRT HSYNC signal.

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6.7.95 CR48: TFT HSYNC and LCD-Height Overflow Register

I/O Port Address: 3?5

Index: 48

Bit	Description	Reset State
7(MSB)	Reserved	
6	Reserved	
5	Vertical Size for LCDs [9]	0
4	Vertical Size for LCDs [8]	0
3	Reserved	
2	Vertical Size for Upper Half of Dual-Scan STN LCDs [8]	0
1	TFT HSYNC Dot-Clock Delay [1]	0
0(LSB)	TFT HSYNC Dot-Clock Delay [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:6	Reserved
5:4	**Vertical Size for LCDs [9:8]:** • These bits are the most-significant two bits of a ten-bit field that defines in scanlines the vertical size for one of the following: — the lower half of a dual-scan STN LCD — the total size of a single-scan LCD, either STN or TFT • The eight least-significant bits are in Extension Register CR4A[7:0].
3	Reserved
2	**Vertical Size for Upper Half of Dual-Scan STN LCDs [8]:** • This is the most-significant bit of a nine-bit field that defines in scanlines the vertical size for the upper half of a dual-scan STN LCD. • The least-significant eight bits are in Extension Register CR49[7:0].
1:0	**TFT HSYNC Dot-Clock Delay [1:0]:** • These bits provide further control, in 1-DCLK increments, for the TFT HSYNC horizontal start position defined in CR47 in 4-DCLK increments. • These bits control the dot-clock delay in 1-DCLK increments, according to the following table:

CR48		Dot-Clock Delay
[1]	[0]	
0	0	No Delay
0	1	Delay = 1 Dot Clock
1	0	Delay = 2 Dot Clocks
1	1	Delay = 3 Dot Clocks

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6.7.96 CR49: Vertical Size for Upper Half of Dual-Scan STN LCDs

I/O Port Address: 3?5

Index: 49

Bit	Description	Reset State
7(MSB)	Vertical Size for Upper Half of Dual-Scan STN LCDs [7]	0
6	Vertical Size for Upper Half of Dual-Scan STN LCDs [6]	0
5	Vertical Size for Upper Half of Dual-Scan STN LCDs [5]	0
4	Vertical Size for Upper Half of Dual-Scan STN LCDs [4]	0
3	Vertical Size for Upper Half of Dual-Scan STN LCDs [3]	0
2	Vertical Size for Upper Half of Dual-Scan STN LCDs [2]	0
1	Vertical Size for Upper Half of Dual-Scan STN LCDs [1]	0
0(LSB)	Vertical Size for Upper Half of Dual-Scan STN LCDs [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Vertical Size for Upper Half of Dual-Scan STN LCDs [7:0]:** • These bits are the least-significant eight bits of a nine-bit field that defines the vertical size in scanlines. • The most-significant ninth bit of this field is in CR48[2]. • This vertical display position is relative to the start of the first vertical pulse, which is ahead of the actual vertical display when the centering feature is enabled (using registers CR40 through CR43). • Up to 511 scanlines can be defined for display on the upper half of a dual-scan STN LCD. • The actual value in this register will be one less than the lines displayed. For example: — For an LCD using a 480-line mode, program 239. (1/2 x 480) = 240 lines being displayed for upper half. 240 - 1 = 239 — For an LCD using a 600-line mode, program 299. (1/2 x 600) = 300 lines being displayed for upper half. 300 - 1 = 299 Note: The number of lines programmed in this register represents actual displayed lines.

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6.7.97 CR4A: Vertical Size for LCDs

I/O Port Address: 3?5

Index: 4A

Bit	Description	Reset State
7(MSB)	Vertical Size for LCDs [7]	0
6	Vertical Size for LCDs [6]	0
5	Vertical Size for LCDs [5]	0
4	Vertical Size for LCDs [4]	0
3	Vertical Size for LCDs [3]	0
2	Vertical Size for LCDs [2]	0
1	Vertical Size for LCDs [1]	0
0(LSB)	Vertical Size for LCDs [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Vertical Size for LCDs [7:0]:** • These bits are the least-significant eight bits of a ten-bit field that defines the overall vertical size in scanlines for the LCD, regardless of whether the LCD is dual scan or single scan. • The vertical display position is relative to: — the start of the vertical mid-point on dual-scan LCDs — the first vertical pulse on single-scan LCDs • The actual value in this register will be two less than the total lines being displayed. (For example, for a 480-line display, program 478 lines.) • Dual-scan LCDs normally have the same amount of scanlines in both the upper and lower halves of the LCD. • The most-significant two bits of this field are in CR48[5:4].

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CL 28755

6.7.98 CR4B: Reserved — Scratch Pad Register

I/O Port Address: 3?5

Index: 4B

Bit	Description	Reset State
7(MSB)	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is reserved for the exclusive use of the CL-GD7542 BIOS, and must never be written by any application program.

Bit	Description
7:0	Reserved. This register is used as a scratch-pad register by the BIOS.

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CL 28756

6.7.99 CR4C: Input-Resolution Override for Dithering

I/O Port Address: 3?5

Index: 4C

Bit	Description	Reset State
7(MSB)	Input-Resolution Override Enable	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Input Resolution Override [3]	0
2	Input Resolution Override [2]	0
1	Input Resolution Override [1]	0
0(LSB)	Input Resolution Override [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, which is used with both TFT and STN LCDs, is used to change the CL-GD7542's default input resolution settings for the data sent to the dither block.

- When the MVA is enabled, this override register affects only the surrounding area.
- The MVW display is controlled by independent input and output resolution control bits.
- This register supports a maximum of 6 x 6 dithering.

Bit **Description**

7 **Input-Resolution Override Enable:**
When this bit:

- is 0, the settings from HDR (the Hidden DAC Register) apply, including the default input resolution settings shown in the table below:

Dithering Matrix	Default Input Resolution Settings
8 bits/gun	8-8-8 True Color Mode
6 bits/gun	All VGA-compatibility color modes
	All extended color modes that go through the palette RAMDAC
	5-6-5 High Color Mode
5 bits/gun	5-5-5 High Color Mode
3 bits/gun	3-3-2 Color Mode (does not go through the palette RAMDAC)

  - For the default input resolution settings, the CL-GD7542 dithers to maximize the number of colors displayed on an LCD.
- is 1, the default input resolution settings are overridden, and new input resolution values are defined in CR4C[3:0].
  - If the default input resolution settings are not desired, the BIOS can override them by programming any number between 0h and Fh. As a result, the CL-GD7542 can dither more or less than the default case
  - As long as the dithering matrix is smaller than or equal to 6 x 6, the CL-GD7542 can support a combination of input and output resolutions.

Continued on next page

6.7.99 CR4C: Input-Resolution Override for Dithering *(Cont.)*

Bit	Description
6:4	Reserved
3:0	**Input Resolution Override [3:0]:** • When the CR4C[7] override enable bit is 1, the CR4C[3:0] bits define the new input-resolution values for data sent to the dithering block. • The hex value programmed in these bits define the number of bits per gun that the CL-GD7542 uses to control the dithering on an LCD, independent of the following: — the output resolution — the dithering state (enabled vs. disabled) — the CL-GD7542 mode (graphics vs. text)

CR4C				Dithering Result for LCD
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/gun
0	1	0	0	4 bits/gun
0	1	0	1	5 bits/gun
0	1	1	0	6 bits/gun
0	1	1	1	7 bits/gun
1	0	0	0	8 bits/gun

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CL 28758

6.7.99 CR4C: Input-Resolution Override for Dithering *(Cont.)*

Bit	Description
3:0 *(cont.)*	**Override Input Resolution [3:0]:**

Example 1:

When the given conditions are:
- Data comes from the 18-bit palette DAC color look-up table as 6 bits/gun.
- Colors displayed are 256.
- There are 8 bits/pixel.
- LCD is a 3 bits/gun TFT.

Then:
- The CL-GD7542 default input resolution is 6 bits/gun.
- The CL-GD7542 output resolution is 3 bits/gun.
- When 2 x 2 dithering is enough:
  - — The 6 bits/gun default input resolution is overridden with one of 5 bits/gun.
  - — Since 5 bits/gun - 3 bits/gun = 2 bits/gun, this leads to a 2 x 2 dithering and the equivalent of 5 bits/gun (2^5 = 32 colors per gun, or 32K colors).
- When 256K colors is not enough and a better effect is desired:
  - — More dithering is possible by programming an input resolution of 7 bits/gun.
  - — Since 7 bits/gun - 3 bits/gun = 4 bits/gun, this leads to a 4 x 4 dithering and the equivalent of 7 bits/gun (2^7 = 128 colors per gun, or 2M colors).

Example 2:

When the given conditions are:
- Colors displayed are 16.
- There are 8 bits/pixel.
- LCD is a color STN.
- The output resolution is programmed as 4 bits/gun (2^4 = 16).

Then
- The CL-GD7542 default input resolution is 6 bits/gun.
  (Combining 2^4 = 16 colors with 2^2 = 4 color dithering results in $2^4 \times 2^2 = 2^6$ = 6 bits/gun.)
- By changing the output resolution to 3 bits/gun, the CL-GD7542 generates 2^3 = 8 colors.
- When the input resolution is 6 bits/gun, the CL-GD7542 does more dithering to get 6 bits/gun
- When the input resolution is 4 bits/gun, the CL-GD7542 needs only 1 x 1 dithering to get a total of 16 equivalent colors per gun

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CL 28759

6.7.100 CR4D: Output Resolution for Dithering

I/O Port Address: 3?5

Index: 4D

Bit	Description	Reset State
7(MSB)	MVA Output Resolution for Dithering [3]	0
6	MVA Output Resolution for Dithering [2]	0
5	MVA Output Resolution for Dithering [1]	0
4	MVA Output Resolution for Dithering [0]	0
3	Output Resolution for Dithering [3]	0
2	Output Resolution for Dithering [2]	0
1	Output Resolution for Dithering [1]	0
0(LSB)	Output Resolution for Dithering [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:4	**MVA Output Resolution for Dithering [3:0]:** These bits define the output resolution value for dithering exactly the same as CR4D[3:0] below, except they apply to the MotionVideo™ Window (MVW). These bits are active even when the MVW is displayed on the entire screen.
3:0	**Output Resolution for Dithering [3:0]:** These bits define typical output resolution values for dithering various LCDs. The hex value programmed in these bits define the number of bits per gun used by the CL-GD7542.

CR4D				Output Resolution for Dithering LCDs:	
[3]	[2]	[1]	[0]	TFT LCDs (No Frame-Rate Modulation)	STN LCDs (Frame-Rate Modulation Occurs)
0	0	0	1	Not applicable	2-shade STN LCDs: 1 bit/gun
0	0	1	0	Not applicable	4-shade STN LCDs: 2 bits/gun
0	0	1	1	3 bits/gun	8-shade STN LCDs: 3 bits/gun
0	1	0	0	4 bits/gun	16-shade STN LCDs: 4 bits/gun
0	1	1	0	6 bits/gun	Not applicable
1	0	0	0	8 bits/gun	Not applicable

Note: Programming values other than the ones specified in the above table may have unpredictable results. Also, the Reset value of zero is not a valid value. Therefore, **this register must be programmed at start-up with the correct output resolution for the LCD used (TFT or STN).**

6.7.101 CR4E: MVA Input-Resolution Override for Dithering

I/O Port Address: 3?5

Index: 4E

Bit	Description	Reset State
7(MSB)	MVA Input-Resolution Override Enable	0
6	Enable Dithering for the MVA	0
5	Reserved	
4	Reserved	
3	MVA Input Resolution Override [3]	0
2	MVA Input Resolution Override [2]	0
1	MVA Input Resolution Override [1]	0
0(LSB)	MVA Input Resolution Override [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to change the CL-GD7542's default resolution settings for the data sent to the dither block, either for the MVA window or for when the MVA fills the entire screen.

Bit 7 — MVA Input-Resolution Override Enable:
When this bit:

- is 0, the settings from HDR (the Hidden DAC Register) apply, including the default input resolution settings shown in the table below:

Dithering Matrix	Default Input Resolution Settings
8 bits/gun	8-8-8 True Color Mode
6 bits/gun	All VGA-compatibility color modes
	All extended color modes that go through the palette RAMDAC
	5-6-5 High Color Mode
5 bits/gun	5-5-5 High Color Mode
3 bits/gun	3-3-2 Color Mode (does not go through the palette RAMDAC)

- is 1, the default input resolution settings for the MVA are overridden, and new values are defined in CR4E[3:0].

Bit 6 — Enable Dithering for the MVA:
When this bit is 1, MVA dithering is enabled.

Bit 5 4 — Reserved

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6.7.101 CR4E: MVA Input-Resolution Override for Dithering *(Cont.)*

Bit	Description
3:0	**MVA Input Resolution Override [3:0]:** • When the CR4E[7] override enable bit is 1, the CR4E[3:0] bits define the new input-resolution values for data sent to the dithering block, so that the amount of colors in MVW can differ from the surrounding area. • The hex value programmed can be any number between 1h and Fh. • The value programmed in these bits define the number of bits per gun that the CL-GD7542 uses to control the dithering on an LCD, independent of the following: — the output resolution — the dithering state (enabled vs. disabled) — the CL-GD7542 mode (graphics vs. text)

CR4E				Dithering Result for LCD
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/gun
0	1	0	0	4 bits/gun
0	1	0	1	5 bits/gun
0	1	1	0	6 bits/gun All data goes through the palette RAMDAC. Data may be either 4 or 8 bits/pixel.)
0	1	1	1	7 bits/gun
1	0	0	0	8 bits/gun. Includes: 8-8-8 RGB True Color Mode 8-bit True Color Mode YUV 4-2-2

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CL 28762

6.7.102 HDR: Hidden DAC Register

I/O Port Address: 3C6

Index: (n/a)

Bit	Description	Reset State
7	5-5-5 Extended Color Mode Enable	0
6	Extended Color Mode Select Bits Enable	0
5	Clocking Mode	0
4	32K Extended Color Mode Control	0
3	Extended Color Mode Select [3]	0
2	Extended Color Mode Select [2]	0
1	Extended Color Mode Select [1]	0
0	Extended Color Mode Select [0]	0

This register:

- is used to enable extended color modes, including the following:
  - — 15-bit/pixel extended color mode
  - — 16-bit/pixel extended color mode
  - — 24-bit/pixel extended color mode
- is accessed by reading four times in succession the External/General 3C6 Pixel Mask Register. The next write or read at 3C6 will then access the Hidden DAC Register.
  - — A *write* to the Hidden DAC Register resets the internal counter, and the four dummy reads of the 3C6 Pixel Mask Register must be executed again.
  - — A *read* from the Hidden DAC Register resets the internal counter, and the four dummy reads of the 3C6 Pixel Mask Register must be executed again.
  - — Reads from the 3C6 do not lock the Hidden DAC Register.
- is cleared to all zeroes at reset, putting the CL-GD7542 in VGA-compatibility mode.
- does not affect Motion Video Architecture modes.

Bit	Description
7	**5-5-5 Extended Color Mode Enable:** • When this bit is 0: — The extended color modes are disabled. — The Palette DAC is VGA-compatible. • When this bit is 1: — it enables the extended color modes (including the 5-5-5 extended color mode), as chosen by bit [6] and bits [3:0] of this register
6	**Extended Color Mode Select Bits Enable:** When bit [7] = 1, and this bit is • 0, the extended color mode select bits [3:0] of this register are ignored, and the extended color mode will be the 5-5-5 mode. • 1, the extended color mode select bits [3:0] of this register are enabled to select an extended color mode (other than the 5-5-5 mode).

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6.7.102 HDR: Hidden DAC Register *(cont.)*

Bit — **Description**

5 — **Clocking Mode:**

- When this bit is 0, Clocking Mode 1 will be chosen. In Clocking Mode 1:
  - — 16-bit/pixel modes will use both edges of DCLK to latch data.
  - — The rising edge of DCLK will latch the least-significant byte, and the falling edge of DCLK will latch the most-significant byte.
- When this bit is 1, Clocking Mode 2 will be chosen. In Clocking Mode 2:
  - — 16-bit/pixel modes will use only the rising edge of DCLK to latch data.
  - — The DCLK must be supplied at twice the pixel rate.
  - — The first rising edge of DCLK will latch the least-significant byte, and the second rising edge of DCLK will latch the most-significant byte.

NOTE: All modes other than 16-bit/pixel use only the rising DCLK edge, regardless of this bit.

4 — **32K Extended Color Mode Control:**

When this bit:

- is 0, a 5-5-5 extended color mode operation will take place normally.
- is 1 *and* Pixel Data Bit [15]:
  - — is a 0, then the 5-5-5 extended color mode operation that is chosen allows 5-5-5 data to overlay 256-color images on a pixel-by-pixel basis.
  - — is a 1, then Pixel Data Bits [7:0] choose a palette entry and Pixel Data Bits [14:8] are ignored.

3:0 — **Extended Color Mode Select [3:0]:**

When HDR[7:6] = 11, this four-bit field selects an extended color mode according to the following table:

HDR						Color Mode	
[7]	[6]	[3]	[2]	[1]	[0]		
0	X	X	X	X	X	VGA Compatibility Color Mode	
1	0	X	X	X	X	Extended Color Modes	5-5-5
1	1	0	0	0	1		5-6-5 XGA™
1	1	0	1	0	1		8-8-8 16-million Color
1	1	0	1	1	X		DAC Power-Down
1	1	1	0	0	0		8-bit Grayscale
1	1	1	0	0	1		3-3-2 8-bit RGB

NOTE: Any undefined settings are reserved.

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6.7.103 R2X: LCD Timing — LFS Vertical Position #1 (MISC[7:6] = 11)

I/O Port Address: 3?5

Index: 2 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	LFS Vertical Position [7]	R/W	0
6	LFS Vertical Position [6]	R/W	0
5	LFS Vertical Position [5]	R/W	0
4	LFS Vertical Position [4]	R/W	0
3	LFS Vertical Position [3]	R/W	0
2	LFS Vertical Position [2]	R/W	0
1	LFS Vertical Position [1]	R/W	0
0(LSB)	LFS Vertical Position [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Register R2X (and Registers R3X, R4X, R5X, and RCX with overflow bits in R6X and REX) define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal.

- At power-on self-test, these registers are programmed according to the type of LCD used.
- Which registers are automatically selected depends on the graphic modes that are selected and which expansion and centering options are selected.
- Refer to Table 6–10 for selection options.

Bit	Description
7:0	**LFS Vertical Position #1 [7:0]:** • These bits are the least-significant eight bits of a 10-bit field. The field's value defines in scanlines the vertical position of the line frame start (LFS) signal, relative to the CRT frame start signal. • For 640 x 480 LCDs, the R2X field is used when: — CR2D[1] = 0 (automatic vertical expansion is disabled). — CR2D[0] = 0 (automatic centering is disabled). — External/General Register MISC[7:6] = 11 (480 lines are displayed). • For 640 x 480 LCDs, the R2X field is used for *all* modes when: — CR2D[1] = 1 (automatic vertical expansion is enabled). — CR2D[0] = 0 (automatic centering is disabled). • For 800 x 600 LCDs, the R2X field is used in all cases: — CR2D[1] = 0 (automatic vertical expansion is disabled). — CR2D[0] = 0 (automatic centering is disabled). — *except* when External/General Register MISC[7:6] = 10 (350 lines are displayed) • The most-significant two bits of this field are stored in register R6X[7:6]. • For LFS Vertical-Position-Selection Logic Diagram, refer to Figure 6–5.

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6.7.103 R2X: LCD Timing — LFS Vertical Position #1 (MISC[7:6] = 11) – *(Cont.)*

Table 6–9. LFS Vertical Position Register Automatic Selection

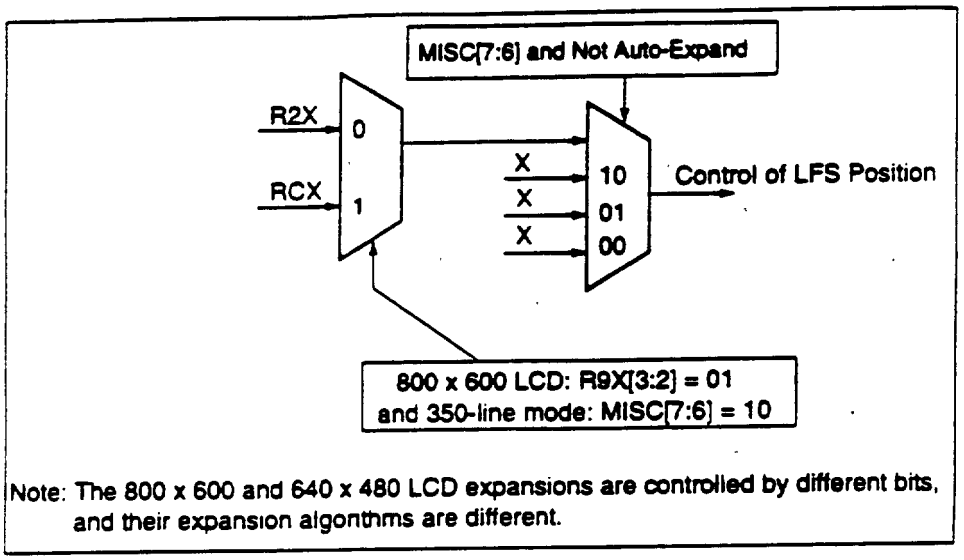
LFS Vertical Position Register Selected	Auto Vertical Expand	Auto Center	MISC[7:6]	Display Resolution Mode	LCD Size
R2X[7:0] and R6X[7:6]	Off	On	11	640 x 480	640 x 480
	On CR2D[1]	X	X	All display resolution modes	640 x 480
	On CR2E[1:0]	X	11, 01, 00	All display resolution modes except for 350 lines	800 x 600
R3X[7:0] and R6X[5:4]	Off	On CR2D[0]	10	640 x 350	640 x 480 or 800 x 600
R4X[7:0] and R6X[3:2]	Off	On CR2D[0]	01	640 x 400	640 x 480 or 800 x 600
	Off	On	01	720 x 400	800 x 600
R5X[7:0] and R6X[1.0]	Off	On	00	800 x 600	800 x 600
RCX[7:0] and REX[1:0]	On	X	10	640 x 350	800 x 600

a. Automatic vertical expansion is controlled by different registers, depending on the LCD size selected.
"Off" means all the appropriate bits are set to 0.
"On" means all the appropriate bits are set to 1.

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6.7.103 R2X: LCD Timing — LFS Vertical Position #1 (MISC[7:6] = 11) – *(Cont.)*



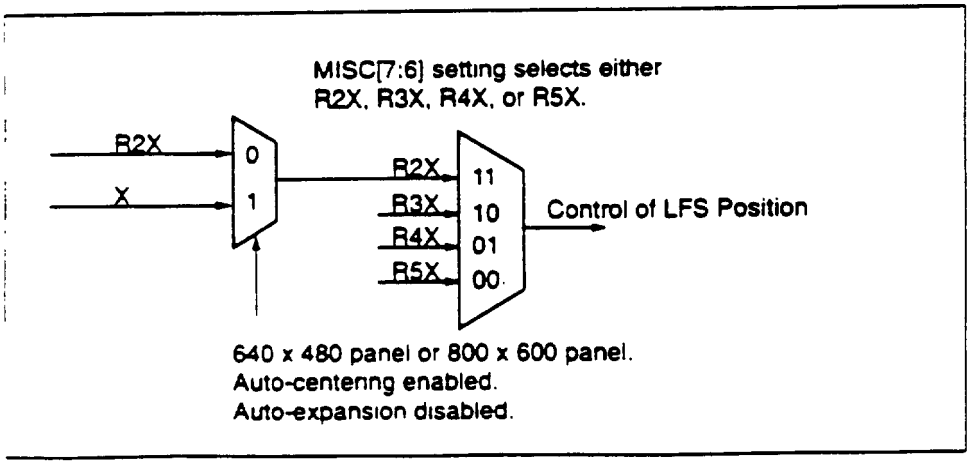


Figure 6–5. LFS Vertical-Position-Selection Logic Diagrams

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6.7.103 R2X: LCD Timing — LFS Vertical Position #1 (MISC[7:6] = 11) – *(Cont.)*

Table 6–10. LFS Vertical Position Register Automatic Selection

LFS Vertical Position Register Selected	Automatic Vertical Expansion	Automatic Centering	MISC		Display Resolution Mode	LCD Size
			[7]	[6]		
R2X[7:0] and R6X[7:6]	Off	On	1	1	640 x 480	640 x 480
	On CR2D[1]	X	X	X	All display resolution modes	640 x 480
	On CR2E[1:0]	X	1	1	All display resolution modes except for 350 lines	800 x 600
		X	0	1		
		X	0	0		
R3X[7:0] and R6X[5:4]	Off	On CR2D[0]	1	0	640 x 350	640 x 480 or 800 x 600
R4X[7:0] and R6X[3:2]	Off	On CR2D[0]	0	1	640 x 400	640 x 480 or 800 x 600
	Off	On	0	1	720 x 400	800 x 600
R5X[7:0] and R6X[1:0]	Off	On	0	0	800 x 600	800 x 600
RCX[7:0] and REX[1:0]	On	X	1	0	640 x 350	800 x 600

a. Automatic vertical expansion is controlled by different registers, depending on the LCD size selected.
"Off" means all the appropriate bits are set to 0.
"On" means all the appropriate bits are set to 1.

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6.7.104 R3X: LCD Timing — LFS Vertical Position #2 (MISC[7:6] = 10)

I/O Port Address: 3?5

Index: 3 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	LFS Vertical Position #2 [7]	R/W	0
6	LFS Vertical Position #2 [6]	R/W	0
5	LFS Vertical Position #2 [5]	R/W	0
4	LFS Vertical Position #2 [4]	R/W	0
3	LFS Vertical Position #2 [3]	R/W	0
2	LFS Vertical Position #2 [2]	R/W	0
1	LFS Vertical Position #2 [1]	R/W	0
0(LSB)	LFS Vertical Position #2 [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #2 [7:0]:** • These bits are the least-significant eight bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General Register MISC[7:6] = 10 (350 lines are displayed). — Extension Register CR2D[1] = 0 (automatic vertical expansion is disabled). — Extension Register CR2D[0] = 1 (automatic centering is enabled, when CR2D[1] = 0). • The most-significant two bits are stored in register R6X[5:4]. • For selection options, refer to Table 6–10.

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6.7.105 R4X: LCD Timing — LFS Vertical Position #3 (MISC[7:6] = 01)

I/O Port Address: 3?5

Index: 4 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	LFS Vertical Position #3 [7]	R/W	0
6	LFS Vertical Position #3 [6]	R/W	0
5	LFS Vertical Position #3 [5]	R/W	0
4	LFS Vertical Position #3 [4]	R/W	0
3	LFS Vertical Position #3 [3]	R/W	0
2	LFS Vertical Position #3 [2]	R/W	0
1	LFS Vertical Position #3 [1]	R/W	0
0(LSB)	LFS Vertical Position #3 [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #3 [7:0]:** • These bits are the least-significant eight bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General Register MISC[7:6] = 01 (400 lines are displayed). — Extension Register CR2D[1] = 0 (automatic vertical expansion is disabled). — Extension Register CR2D[0] = 1 (automatic centering is enabled, when CR2D[1] = 0). • The most-significant two bits are stored in register R6X[3:2]. • For selection options, refer to Table 6–10.

6.7.106 R5X: LCD Timing — LFS Vertical Position #4 (MISC[7:6] = 00)

I/O Port Address: 3?5

Index: 5 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	LFS Vertical Position #4 [7]	R/W	0
6	LFS Vertical Position #4 [6]	R/W	0
5	LFS Vertical Position #4 [5]	R/W	0
4	LFS Vertical Position #4 [4]	R/W	0
3	LFS Vertical Position #4 [3]	R/W	0
2	LFS Vertical Position #4 [2]	R/W	0
1	LFS Vertical Position #4 [1]	R/W	0
0(LSB)	LFS Vertical Position #4 [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #4 [7:0]:** • These bits are the least-significant eight bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General Register MISC[7:6] = 00. — Extension Register CR2D[1] = 0 (automatic vertical expansion is disabled). — Extension Register CR2D[0] = 1 (automatic centering is enabled, when CR2D[1] = 0). • The most-significant two bits are stored in register R6X[1:0]. • For selection options, refer to Table 6–10.

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6.7.107 R6X: LCD Timing — Overflow Bits for LFS Signal Compare

I/O Port Address: 3?5

Index: 6 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	R2X LFS Vertical Position #1 [9]	R/W	0
6	R2X LFS Vertical Position #1 [8]	R/W	0
5	R3X LFS Vertical Position #2 [9]	R/W	0
4	R3X LFS Vertical Position #2 [8]	R/W	0
3	R4X LFS Vertical Position #3 [9]	R/W	0
2	R4X LFS Vertical Position #3 [8]	R/W	0
1	R5X LFS Vertical Position #4 [9]	R/W	0
0(LSB)	R5X LFS Vertical Position #4 [8]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines the two most-significant overflow bits for the LFS Vertical Position registers R2X, R3X, R4X, and R5X.

Bit	Description
7:6	**R2X LFS Vertical Position #1 [9:8]:** When External/General Register MISC[7:6] = 11, these are the most-significant two bits of register R2X, creating a 10-bit value.
5:4	**R3X LFS Vertical Position #2 [9:8]:** When External/General Register MISC[7:6] = 10, these are the most-significant two bits of register R3X, creating a 10-bit value.
3:2	**R4X LFS Vertical Position #3 [9:8]:** When External/General Register MISC[7:6] = 01, these are the most-significant two bits of register R4X, creating a 10-bit value.
1:0	**R5X LFS Vertical Position #4 [9:8]:** When External/General Register MISC[7:6] = 00, these are the most-significant two bits of register R5X, creating a 10-bit value.

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CL 28772

6.7.108 R7X: LCD Timing — LCD Signal Control for Color TFT LCDs

I/O Port Address: 3?5

Index: 7 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	LFS Output	R/W	0
2	LLCLK Output	R/W	0
1	FPVDCLK Inversion	R/W	0
0(LSB)	Free-Running FPVDCLK for TFT LCDs	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:4	Reserved
3	**LFS Output:** In both of the following cases, the line frame signal (LFS) output is controlled by the first vertical pulse, which marks the beginning of the LCD display. • When this bit is 0: — the LFS output pin drives both STN and DE-type TFT LCDs. — the LFS output (which may also be called FLM) is one line wide and is programmable. • When this bit is 1: — the LFS output pin drives the VSYNC input for non-DE-type TFT LCDs. — the LFS output (which may also be called TFT-VSYNC) is two lines wide and can support only single-scan LCDs. • Set this bit to 1 for Matsushita TFT LCDs.

Continued on next page.

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CL 28773

6.7.108 R7X: LCD Timing — LCD Signal Control for Color TFT LCDs *(Cont.)*

Bit	Description
2	**LLCLK Output:** • When this bit is 0: — The LLCLK output pin drives both STN and DE-type TFT LCDs. — The LLCLK signal position is controlled by "LCD Horizontal Display Enable Start" values stored in Extension Registers CR40 to CR42, and Extension Register CR43 is used for fine positioning. — The LLCLK signal starts with the HFirst pulse. (Refer to the timing diagram within the description of the Extension Register CR40.) — The LLCLK signal is always 25 dot clocks before the LCD display enable start signal. • When this bit is 1: — Tie LFS to VSYNC. (Refer to Extension Register R7X[3].) • This bit must be set to 1 for: — non-DE-type TFT LCDs. — LCDs that require an offset different than 25 dot clocks between the LLCLK (or LCD HSYNC) signal and the LCD display enable start signal. For instance, some LCDs require an offset of 144 dot clocks between LLCLK and the first LCD shift clock. In this case, set R7X[2] = 1, which places the LLCLK output under the control of Extension Register CR47[7:0].
1	**FPVDCLK Inversion:** This bit can be used with all LCDs. • When this bit is: — 1, the FPVDCLK signal is inverted, and LCD data are latched on the low-to-high transition of FPVDCLK. — 0, the FPVDCLK signal is not inverted, and LCD data are latched on the high-to-low transition of FPVDCLK. • During Suspend mode, FPVDCLK is forced low, independent of this bit's polarity.
0	**Free-Running FPVDCLK Enable for TFT LCDs:** Set this bit to 1 only for TFT LCDs that have a display enable input pin. When this bit: • = 1, and when the LCD power sequence is on, FPVDCLK is always active (free-running) for TFT LCDs. • = 0, FPVDCLK is gated by the display enable signal and remains active only during display time

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CL 28774

6.7.109 R8X: LCD Timing — Shift Clock and Data Format Select for STN LCDs

I/O Port Address: 3?5

Index: 8 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Horizontal Cross-Talk Reduction Enable	R/W	0
6	Vertical Cross-Talk Reduction Disable	R/W	0
5	Dual-Scan/Single-Scan Monochrome LCD Select	R/W	0
4	Foreground-Only Text Enhancement	R/W	0
3	Reserved		0
2	Reserved		
1	Dual/Single Shift-Clock Select for STN LCDs	R/W	0
0(LSB)	16-Bit / 8-Bit Data-Interface Select for STN LCDs	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Horizontal Cross-Talk Reduction Enable:** When this bit is 1, horizontal cross-talk reduction is enabled. This bit is a test bit, and it must never be written by any application program. It is listed here only for completeness.
6	**Vertical Cross-Talk Reduction Disable:** When this bit is 1, vertical cross-talk reduction is disabled. This bit is a test bit, and it must never be written by any application program. It is listed here only for completeness.
5	**Dual-Scan/Single-Scan Monochrome LCD Select:** • When this bit is 0, dual-scan monochrome LCDs are selected. • When this bit is 1, single-scan monochrome LCDs are selected.
4	**Foreground-Only Text Enhancement:** • When this bit is 0, normal text is displayed. • When this bit is 1 and Extension Register CR1E[1] = 1, the foreground-only text enhancement is enabled.
3 2	Reserved
1	**Dual/Single Shift-Clock Select for STN LCDs:** On an STN LCD, when this bit: • = 0, a single-shift clock is supplied to the FPVDCLK pin. • = 1, dual-shift clocks are supplied to the FPVDCLK and FPDE pins.
0	**16-Bit / 8-Bit Data-Interface Select for STN LCDs:** • On an STN LCD, when this bit is 0, a 16-bit data LCD interface is selected. • On an STN LCD, when this bit is 1, an 8-bit data LCD interface is selected.

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6.7.110 R9X: LCD Size and TFT LCD Data Format

I/O Port Address: 3?5

Index: 9 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	LCD Size [1]	R/W	0
2	LCD Size [0]	R/W	0
1	TFT LCD Data Format [1]	R/W	0
0(LSB)	TFT LCD Data Format [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:4	Reserved
3:2	**LCD Size [1:0]:** These two bits select the LCD size as shown in the table below. For information on specific LCD types and for detailed connection information, refer to the *Guide to Interfacing Panels to the CL-GD7542.*

R9X [3]	R9X [2]	LCD Size	LCD Types to Which LCD Size Can Be Applied
0	0	640 x 480	STN and TFT
0	1	800 x 600	STN and TFT
1	0	Reserved	—
1	1	Reserved	—

1 0 **TFT LCD Data Format [1:0]:**
These two bits select the data format for TFT LCDs as shown in the table below. For information on specific LCD types and for detailed connection information, refer to the *Guide to Interfacing Panels to the CL-GD7542.*

R9X [1]	R9X [0]	TFT LCD Data Format
0	0	9-bit (333)
0	1	12-bit (444)
1	0	18-bit (666)
1	1	24-bit (888)

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CL 28776

6.7.111 RBX: Shade Conversion and Extra LCD Line Clock Insertion

I/O Port Address: 3?5

Index: B — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Shades 7 and 9 Convert	R/W	0
3	Shades 5 and 11 Convert	R/W	0
2	Extra LCD Line Clock Enable [2]	R/W	0
1	Extra LCD Line Clock Enable [1]	R/W	0
0(LSB)	Extra LCD Line Clock Enable [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:5	Reserved
4	**Shades 7 and 9 Convert:** When this bit is 1: • shade 7 is converted to shade 6. • shade 9 is converted to shade 8.
3	**Shades 5 and 11 Convert:** When this bit is 1: • shade 5 is converted to shade 4. • shade 11 is converted to shade 10.
2:0	**Extra LCD Line Clock Enable [2:0]:** The hex value in these three bits define up to five extra LCD line clocks, which can be inserted between the upper and lower half of a dual-scan LCD. • Extra line clocks are needed for those LCD manufacturers who disconnect the first one or two row drivers on the lower half of a dual-scan LCD. • These bits generate extra line clocks for disconnected row drivers.

RBX			Result
[2]	[1]	[0]	
0	0	0	0 extra LCD line clocks
0	0	1	1 extra LCD line clock
0	1	0	2 extra LCD line clocks
0	1	1	3 extra LCD line clocks
1	0	0	4 extra LCD line clocks
1	0	1	5 extra LCD line clocks

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CL 28777

6.7.112 RCX: LFS Vertical Position for 525-Line Modes

I/O Port Address: 3?5

Index: C — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Reset State
7	LFS Vertical Position for 525-Line Modes [7]	0
6	LFS Vertical Position for 525-Line Modes [6]	0
5	LFS Vertical Position for 525-Line Modes [5]	0
4	LFS Vertical Position for 525-Line Modes [4]	0
3	LFS Vertical Position for 525-Line Modes [3]	0
2	LFS Vertical Position for 525-Line Modes [2]	0
1	LFS Vertical Position for 525-Line Modes [1]	0
0	LFS Vertical Position for 525-Line Modes [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

For 800 x 600 LCDs, this register is used:

- to expand the 350 lines resulting from a 350-line mode to 525 lines and then to center the 525 lines
- to define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position for 525-Line Modes [7:0]:** • These bits are the least-significant eight bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — The LCD is a 525-line LCD, or the LCD is one that uses a 525-line mode that has been expanded to 600 lines. — External/General Register MISC[7:6] = 10 (350 lines are displayed). — Video modes 10 or F are being used. (These modes display 350 lines.) — Extension Register CR2D[1] = 1 (automatic vertical expansion is enabled). • The most-significant two bits of this field are in REX[1:0]. • For selection options, refer to to Table 6–10.

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CL 28778

6.7.113 RDX: LCD Timing — LFS Vertical Position #6

I/O Port Address: 3?5

Index: D — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0(LSB)	Reserved		

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is reserved.

Bit	Description
7:0	Reserved

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CL 28779

6.7.114 REX: Overflow Bits for RCX Register

I/O Port Address: 3?5

Index: E — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	RCX: LFS Vertical Position for 525-Line Modes [9]	R/W	0
0	RCX: LFS Vertical Position for 525-Line Modes [8]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:2	Reserved
1:0	**RCX LFS Vertical Position for 525-Line Modes [9:8]:** • These two overflow bits are the most-significant bits of a 10-bit field, LFS Vertical Position for 525-line modes. • For more information, refer to RCX[7:0], which contain the least-significant bits for this field.

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CL 28780

6.7.115 R0Y: Horizontal Total Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

The RiY (i = 0,2,3,4,5) Extension Registers are horizontal timing shadow registers.

- These registers are used to automatically control the CRT controller on 640 x 480 and 800 x 600 LCDs, for both low-resolution and high-resolution applications.
- These registers control LCD timing independent of VGA modes.

Bit	Description
7:0	**Horizontal Total [7:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR0[7:0]).

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CL 28781

6.7.116 R2Y: Horizontal Blanking Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR2[7:0].

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CL 28782

6.7.117 R3Y: Horizontal Blanking End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:5	Reserved
4:0	**Horizontal Blanking End [4:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR3[4:0]. • These bits are the least-significant five bits of a 6-bit word controlling the horizontal blanking end signal. • The most-significant bit that controls the horizontal blanking end signal is in Extension Register R5Y[7].

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CL 28783

6.7.118 R4Y: Horizontal Sync Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR4[7:0].

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CL 28784

6.7.119 R5Y: Horizontal Sync End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Reserved	
5	Reserved	
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Horizontal Blanking End [5]:** • This is the most-significant bit for the six-bit horizontal blanking end signal. • The least-significant five bits of the horizontal blanking end signal are in Extension Register R3Y[4:0].
6	Reserved
4:0	**Horizontal Sync End [4:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR5[4:0]

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CL 28785

6.7.120 R0Z: Horizontal Total Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

The RiZ (i = 0,2,3,4,5) Extension Registers are horizontal timing shadow registers.

- These registers are used to automatically control the CRT controller on 640 x 480 and 800 x 600 LCDs, for both low-resolution and high-resolution applications.
- These registers control LCD timing independent of VGA modes.

Bit	Description
7:0	**Horizontal Total [7:0]:** When Sequencer Register SR1[3] = 1 (VCLK is divided by 2), this register performs the same function as CRT Controller Register CR0[7:0].

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CL 28786

6.7.121 R2Z: Horizontal Blanking Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** When Sequencer Register SR1[3] = 1 (VCLK is divided by 2), this register performs the same function as CRT Controller Register CR2[7:0].

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CL 28787

6.7.122 R3Z: Horizontal Blanking End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:5	Reserved
4:0	**Horizontal Blanking End [4:0]:** When Sequencer Registser SR1[3] = 1 (VCLK is divided by 2), these bits perform the same function as CR3[4:0]. • These bits are the least-significant five bits of a 6-bit word controlling the horizontal blanking end signal. • The most-significant sixth bit that controls the horizontal blanking end signal is in register R5Z[7].

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CL 28788

6.7.123 R4Z: Horizontal Sync Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** When Sequencer Register SR1[3] = 1 (VCLK is divided by 2), this register performs the same function as CRT Controller Register CR4[7:0].

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CL 28789

6.7.124 R5Z: Horizontal Sync End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Reserved	
5	Reserved	
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Horizontal Blanking End [5]:** • This is the most-significant bit of the six-bit horizontal blanking end signal. • The least-significant five bits of the horizontal blanking end signal are in Extension Register R3Z[4:0].
6	Reserved
4.0	**Horizontal Sync End [4:0]:** When Sequencer Register SR1[3] = 1 (VCLK is divided by 2), this register performs the same function as Controller Register CR5[4:0].

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7. Electrical Specifications

7.1 Absolute Maximum Ratings

Table 7–1. Absolute Maximum Ratings

Specification	Maximum Rating
Ambient temperature while operating (T_A)	0° to 70° C
Storage temperature	-65° to 150°
Voltage on any pin	V_{SS} -0.5V to V_{DD} + 0.5V
Operating power dissipation	1.5 Watts
Power supply voltage	7.0 Volts
Injection current (latch-up testing)	100 mA

NOTES:

1) System components should be operated within the limits of the absolute maximum ratings. If system components are run at ratings at or outside these limits, the system components may be permanently damaged.
2) Functional operation at or outside any of the conditions indicated in the absolute maximum ratings is not implied.
3) Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

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CL 28791

7.2 DC Specifications

7.2.1 DC Specifications: Digital

In the table below, VDD = 5.0V ± 0.25V (or V_{DD} = 3.3V ± 0.3V) and T_A = 0° to 70° C, unless otherwise specified.)

Table 7–2. DC Digital Specifications

Symbol	Parameter	MIN	MAX	Conditions	Note
V_{DD} (5 V)	Power Supply Voltage (TTL)	4.75 Volts	5.25 Volts	Normal Operation	
V_{DD} (3.3V)	Power Supply Voltage (CMOS)	3.00 Volts	3.60 Volts	Normal Operation	
V_{IL}	Input Low Voltage (TTL)	0 Volts	0.8 Volts	3.0V < V_{DD} < 5.25V	
V_{IH}	Input High Voltage (TTL)	2.0 Volts	V_{DD} + 5% V_{DD} (Volts)	3.0V < V_{DD} < 5.25V	
V_{IHC}	Input High Voltage (CMOS)	0.7V_{DD} (Volts)	V_{DD} + 5% V_{DD} (Volts)	3.0V < V_{DD} < 5.25V	
V_{ILC}	Input Low Voltage (CMOS)	-0.5 Volts	0.3V_{DD} (Volts)	3.0V < V_{DD} < 5.25V	
V_{OL}	Output Low Voltage (TTL)		0.4 Volts	I_{OL} = (Refer to Table 7–6.)	1
V_{OH}	Output High Voltage (TTL)	2 4 Volts		I_{OH} = (Refer to Table 7–6.)	2
V_{OHC}	Output High Voltage (CMOS)	0.9V_{DD} (Volts)		I_{OHC} = -200 µA	
V_{OLC}	Output Low Voltage (CMOS)		0 1V_{DD} (Volts)	I_{OLC} = 3.2 mA	
I_{CC1}	Power Supply Current		150 mA	CRT-only Operation	3
I_{CC2}	Power Supply Current		100 mA	LCD-only Operation	3
I_{CC3}	Power Supply Current		1 0 mA	Hardware-Controlled Suspend mode	3
I_{IL}	Input Low Current		-10 µA	V_{IN} = 0.0V	
I_{IH}	Input High Current		10 µA	V_{IN} = V_{DD}	
I_{OZ}	Output Leakage Current	-10 µA	10 µA	0 < V_{OUT} < V_{DD}	4
C_{IN}	Input Capacitance		10 pF		5
C_{OUT}	Output Capacitance		10 pF		5

NOTES.

1) Data outputs (D[31.0]) rated at I_{OL} = 12 mA at V_{OL} = 0 4V, will sink I_{OL} = 24 mA at V_{OL} = 0.5V.

2) Data outputs (D[31:0]) rated at I_{OH} = -3.0 mA at V_{OH} = 2.4V, will source I_{OH} = -15 mA at V_{OH} = 2.0V.

3) These current values occur when V_{DD} = 3.3V, FPVDCLK = 28 MHz, and MCLK = 45 MHz.

4) This current is a measure of 3-state output leakage current when in high-impedance (high-Z) mode.

5) This capacitance is periodically sampled and tested

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7.2.2 DC Specifications: Loading Values

Table 7–3. Loading Values for 7542 Output Pins

Pin Number	Pin Name	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
3	LDEV#	—	20.0	200
4	RDY#	-3.0	20.0	200
5	INTR (INTR/INTR#)	-3.0	20.0	200
22	STOP#	-3.0	8.0	200
23	PAR	-3.0	8.0	200
43:46, 48:51, 53:61, 63:66, 68:72, 74:79, 136:135, 138:137,139:140	AD / D [31:0]	-3.0	12.0	240
91	VSYNC	-12	12	50
93	HSYNC	-12	12	50
94	NTSC/PAL	-12	12	50
140 133, 131 125, 123:122, 120:114	FP[23:0]	-12	12	50
95	CSYNC	-12	12	50
144 141,134,133,125,123	FCP[7:0]	-12	12	50
101	FCBLANK#	-12	12	50
102	FPVEE	-12	12	35
103	VCLK	-12	12	240
106	FPVCC	-12	12	35
108	FPDE	-12	12	50
110	LFS[a]	-12	12	50
112	LLCLK[a]	-12	12	50
113	FPVDCLK	-12	12	50
115	OVRW# (FP[1] / OVRW#)	-12	12	35
117	MOD (FP[3] / MOD)	-3.0	3.0	20
123	SBYST#	-6.0	6.0	35
125	SUSPST#	-6.0	6.0	35
146	TVON	-12	12	50
148	PROG	-6.0	6.0	35
151 161 163 167 186 191,193,196,202,204, 206 208,1,2	MD[31:0]	-12	12	50
169 170 195 194	CAS#[3:0]#	-12	12	50
169 170 195 194	WE#[3:0]	-12	12	50
171 180	MA[9:0]	-12	12	50
181	CAS#/WE#	-12	12	50
182	OE#	-12	12	50
184 183	RAS#[1:0]#	-12	12	50

[a] The LLCLK and FPVDCLK values depend on the bit setting of Extension Register SR2B[7].
When this bit = 0 the values for these pins are IOH = -12 mA, IOL = 12 mA, and the load is 50 pF.
When this bit = 1 the values for these pins are IOH = -24mA, IOL = 24 mA, and the load remains 50 pF

7.2.3 DC Specifications: Palette DAC

In the table below, VDD = 5.0V ± 0.25V (or V_{DD} = 3.3V ± 0.3V) and T_A = 0° to 70° C, unless otherwise specified.

Table 7–4. Palette DAC Specifications

Symbol	Parameter	MIN	MAX	Units	Conditions
DACVDD (5.0V)	DAC Supply Voltage	4.75	5.25	Volts	Normal Operation
DACVDD (3.3V)	DAC Supply Voltage	3.00	3.60	Volts	Normal Operation
$AI_{DD2.3}$ (5.0V)	Analog Supply Current		*tbd*	mA	$AV_{DD2.3}$ = 5.25V
$AI_{DD2.3}$ (3.3V)	Analog Supply Current		*tbd*	mA	$AV_{DD2.3}$ = 3.6V
I_{REF}[1]	DAC Reference Current	-3	-10	mA	

NOTE:

1) Refer to the detailed pin description in Chapter 2. for information regarding nominal I_{REF}.

7.2.4 DC Specifications: Frequency Synthesizer

In the table below, V_{DD} = 3.3V ± 0.3V and T_A = 0° to 70° C, unless otherwise specified.

Table 7–5. Frequency Synthesizer Specifications

Symbol	Parameter	MIN	MAX	Units	Conditions
MAV_{DD} VAV_{DD}	Synthesizer Supply Voltage	3.00	3.60	Volts	
MAI_{DD} + VAI_{DD}	Analog Supply Current		*tbd*[6]	mA	MAV_{DD} = VAV_{DD} = 3.6V

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7.3 DAC Characteristics

In the table below, V_{DD} = 3.3V ± 0.3V and T_A = 0° to 70° C, unless otherwise specified.

Table 7–6. DAC Characteristics

Symbol	Parameter	MIN	MAX	Units	Conditions	Notes
Res	Resolution		6	Bits		
I_O	Output Current		30	mA	V_O < 1V	
t_D	Analog Output Delay		*tbd*[8]	ns		Notes 1, 2, 3
t_r t_f	Analog Output Rise/Fall Time		8	ns		Notes 2, 3, 4
t_S	Analog Output Settling Time		15	ns		Notes 2, 3, 5
t_{SK}	Analog Output Skew		*tbd*	ns		Notes 2, 3, 6
FT	Clock and Data Feed-through		*tbd*	db		Notes 2, 3, 6
DT	DAC-to-DAC Correlation		*tbd*	%		Notes 6, 7
GI	Glitch Impulse		*tbd*	pV/sec.		Notes 2, 3, 6
CT	DAC-to-DAC Crosstalk		*tbd*	db		Notes 2, 3, 4

NOTES:

1) t_D is measured from the 50% point of VCLK to 50% point of full-scale transition.
2) Load is 50 ohms and 30 pF per analog output.
3) I_{REF} = to be determined from measures taken according to the IREF application note
4) t_r and t_f are measured from 10% to 90% full-scale.
5) t_S is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid-point of the distribution of the three DACs measured at full-scale output.
8) *tbd* = to be determined

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7.4 AC Parameters: Listing

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7.4.1 Bus Configuration: Reset Timing

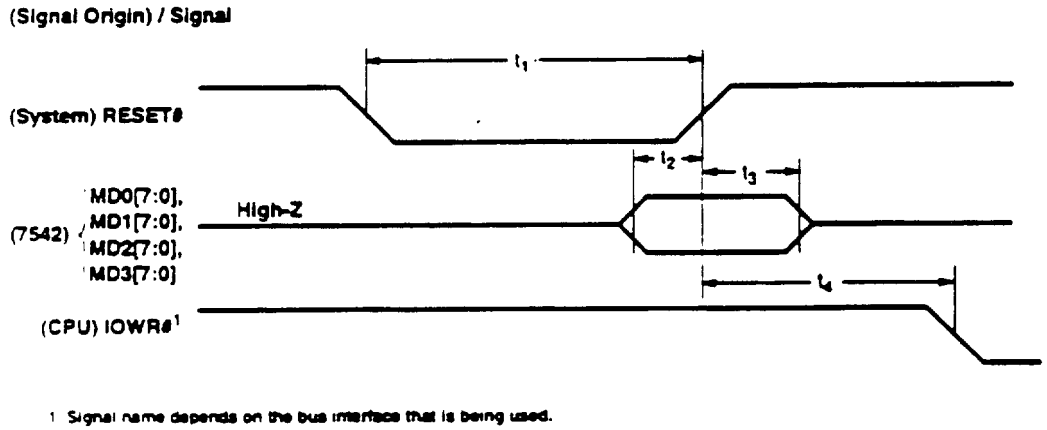
The timing diagram in this section is for the bus configuration, which takes place during setup.

Table 7–7 and Figure 7–1 refer to information from the SW0, SW1, and SW2 pins, which are read by SR24[2:0] and used by the memory data lines to configure the CL-GD7542.

Table 7–7. Bus Configuration: Reset# Timing

Symbol	Parameter	MIN	MAX
t_1	Reset Pulse Width	12t	–
t_2	Memory Data Setup time to Reset rising edge	2ns	–
t_3	Memory Data Hold time from Reset rising edge	5ns	–
t_4	Reset High to first I/O Read/Write Command	12t	–

Note: 't' is the period for MCLK, a clock that is internal to the CL-GD7542.



1 Signal name depends on the bus interface that is being used.

Figure 7–1. Bus Configuration: Reset# Timing

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7.4.2 Local Bus: Timing Diagrams

The timing diagrams in this section apply to the '486 local bus and VESA local bus (the VL bus) interfaces to the CL-GD7542.

Table 7–8. Local Bus: LCLK Timing

Symbol	Parameter	CLK1X	
		MIN	MAX
t_1	Rise Time	0.5ns	4.0ns
t_2	Fall Time	0.5ns	4.0ns
t_3	Positive High Pulse Width	40% t_5	60% t_5
t_4	Negative Low Pulse Width	40% t_5	60% t_5
t_5	Period	30ns	To be determined

Note: 't' is the period for MCLK, a clock that is internal to the CL-GD7542.

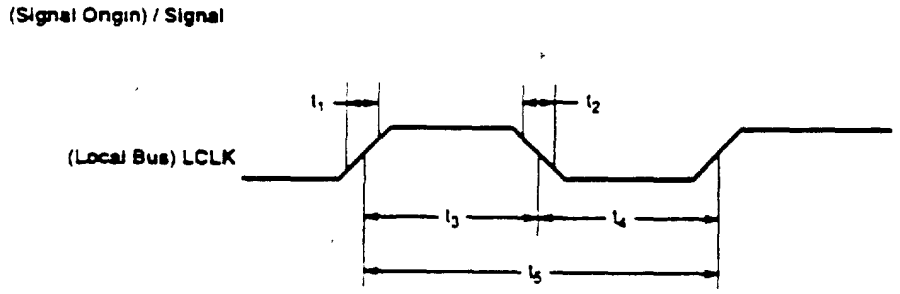


Figure 7–2. Local Bus: LCLK Timing

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Table 7–9. Local Bus: ADS# and LDEV# Timing

Symbol	Parameter	MIN	MAX
t_1	Address, Status, ADS# Setup to LCLK	5ns	–
t_2	LDEV# Low Delay from Address, Status (20-pF loading)	–	15ns
t_3	LDEV# High Delay from Address, Status	–	18ns

Note: 'Y' is the period for MCLK, a clock that is internal to the CL-GD7542.

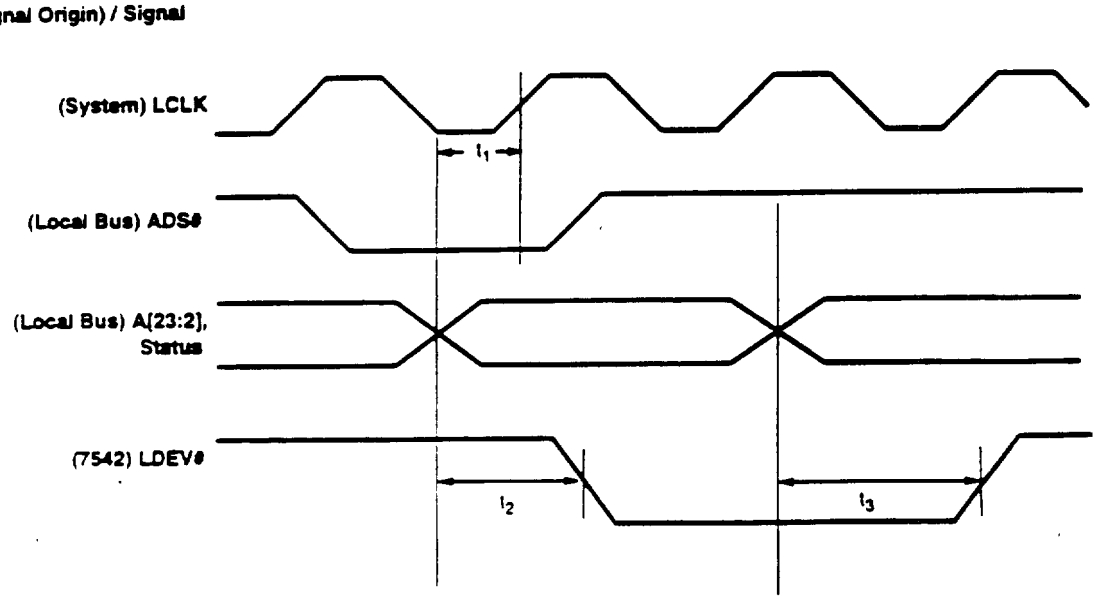


Figure 7–3. Local Bus: ADS# and LDEV# Timing

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Table 7–10. Local Bus: RDY# and Read-Data Timing

Symbol	Parameter	MIN	MAX
t_1	RDY# Low Delay from LCLK	0	12ns
t_2	RDY# High Delay from LCLK	0	12ns
t_3	RDY# High Pulse Width before High-Z	1/2 LCLK	–
t_4	Read Data Setup to RDY# Low	0ns	–
t_5	Read Data Hold from RDYRTN# High	12ns	To be determined

Note: T is the period for MCLK, a clock that is internal to the CL-GD7542.

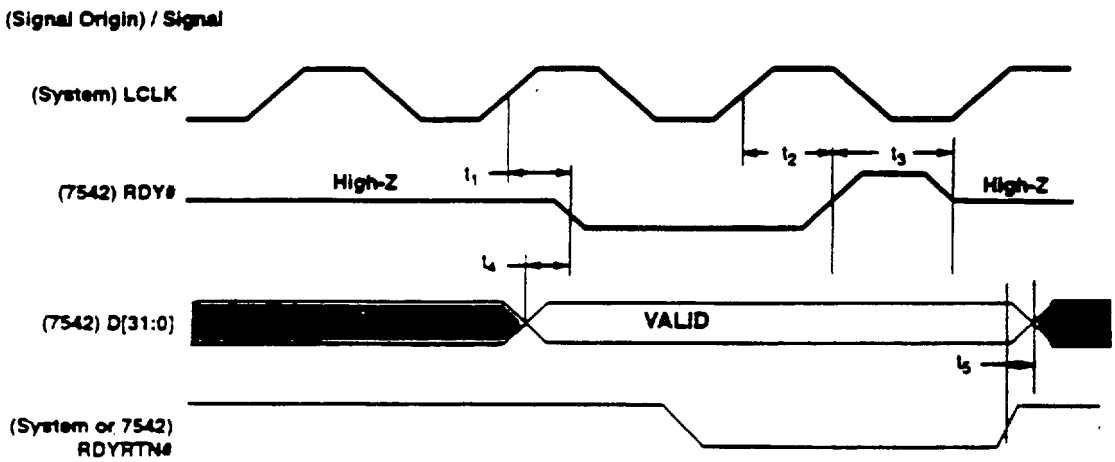


Figure 7–4. Local Bus: RDY# and Read-Data Timing

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Table 7–11. Local Bus: RDYRTN# Timing

Symbol	Parameter	MIN	MAX
t_1	RDYRTN# Setup time to LCLK	5ns	–
t_2	RDYRTN# Hold time from LCLK	2ns	–

Note: 'T' is the period for MCLK, a clock that is internal to the CL-GD7542.

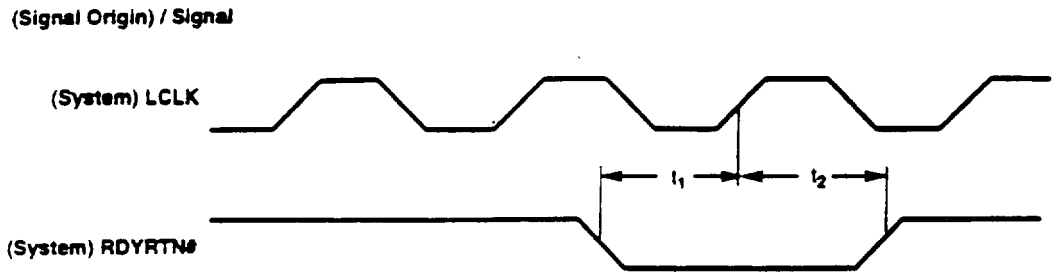


Figure 7–5. Local Bus: RDYRTN# Timing

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Table 7–12. Local Bus: Write Data Timing

Symbol	Parameter	MIN	MAX
t_1	Data Setup time to LCLK	7ns	
t_2	Data Hold time from LCLK	2ns	

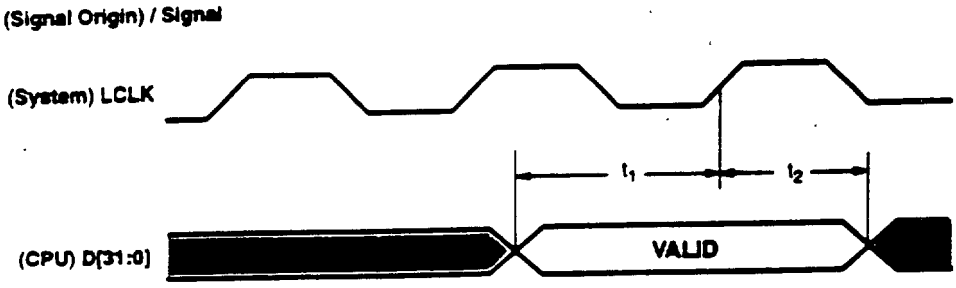


Figure 7–6. Local Bus: Write Data Timing

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7.4.3 PCI Bus: Timing Diagrams

The timing diagrams in this section apply to a PCI bus interface to the CL-GD7542.

Table 7–13. PCI Bus: FRAME#, DEVSEL#, AD[31:0], and C/BE#[3:0] Timing (Write)

Symbol	Parameter	MIN	MAX
t_1	FRAME# Setup to CLK	7 ns	–
t_2	AD[31:0] (Address) Setup to CLK	7 ns	–
t_3	AD[31:0] (Address) Hold from CLK	0 ns	–
t_4	AD[31:0] (Data) Setup to CLK (Write)	7 ns	–
t_5	AD[31:0] (Data) Hold from CLK (Write)	0 ns	–
t_6	C/BE#[3:0] (Bus CMD) Setup to CLK	7 ns	–
t_7	C/BE#[31:0] (Bus CMD) Hold from CLK	0 ns	–
t_8	C/BE#[3:0] (Byte Enable) Setup to CLK	7 ns	–
t_9	DEVSEL# Delay from CLK	0 ns	11
t_{10}	DEVSEL# High before HI-Z	1 CLK	–

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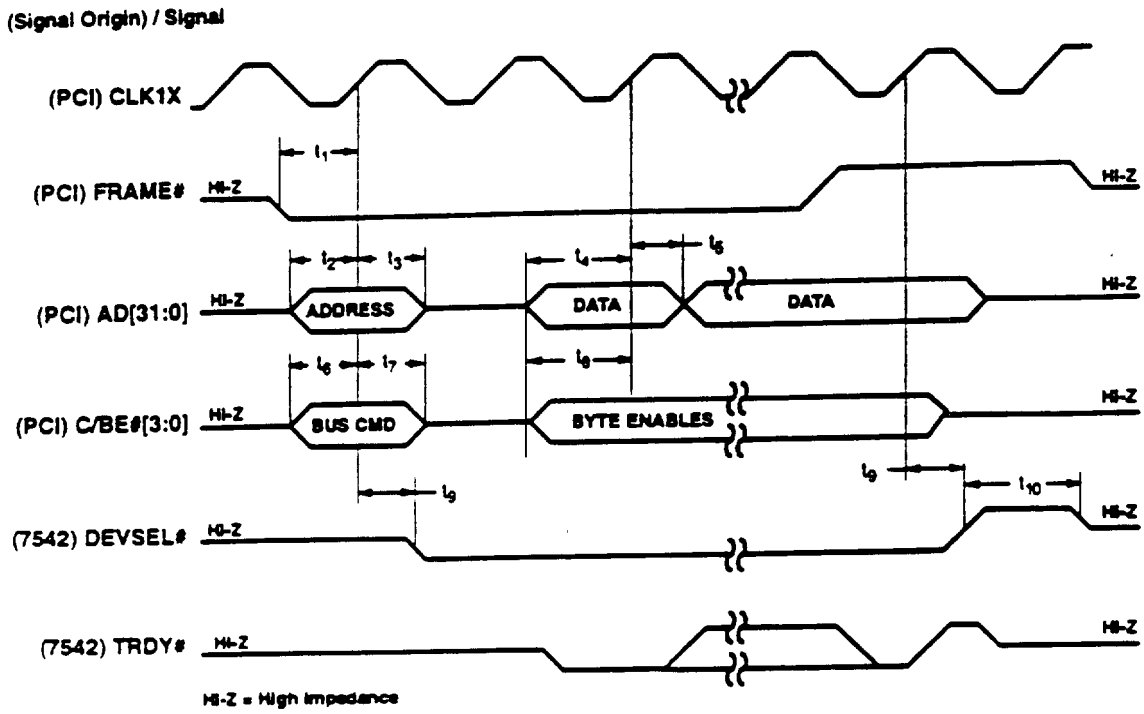


Figure 7–7. PCI Bus: FRAME#, DEVSEL#, AD[31:0], and C/BE#[3:0] Timing (Write)

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Table 7–14. PCI Bus: FRAME#, DEVSEL#, AD[31:0], and C/BE#[3:0] Timing (Read)

Symbol	Parameter	MIN	MAX
t_1	FRAME# Setup to CLK	7ns	–
t_2	AD[31:0] (Address) Setup to CLK	7ns	–
t_3	AD[31:0] (Address) Hold from CLK	0ns	–
t_4	AD[31:0], C/BE#[3:0] HI-Z from CLK (Read)	0ns	28ns
t_5	C/BE#[3:0] (Bus CMD) Setup to CLK	7ns	–
t_6	C/BE#[31:0] (Bus CMD) Hold from CLK	0ns	–
t_7	C/BE#[3:0] (Byte Enable) Setup to CLK	7ns	–
t_8	DEVSEL# Delay from CLK	0ns	11
t_9	DEVSEL# High before HI-Z	1 CLK	–
t_{10}	Data Delay from CLK (Read)	2ns	11ns
t_{11}	Data Hold from CLK (Read)	0ns	To be determined

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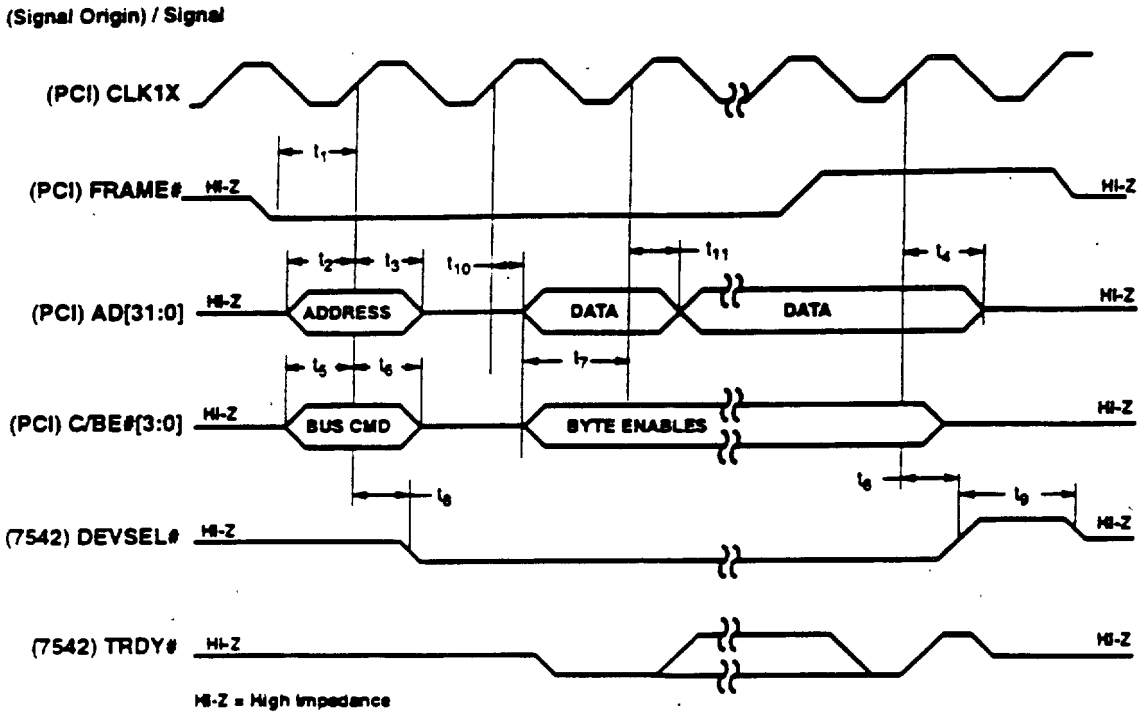


Figure 7–8. PCI Bus: FRAME#, DEVSEL#, AD[31:0], and C/BE#[3:0] Timing (Read)

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Table 7–15. PCI Bus: TRDY# Delay Timing

Symbol	Parameter	MIN	MAX
t_1	TRDY# Low Delay from CLK	0ns	15ns
t_2	TRDY# High Delay from CLK	0ns	15ns
t_3	TRDY# High pulse before HI-Z	1 CLK	–

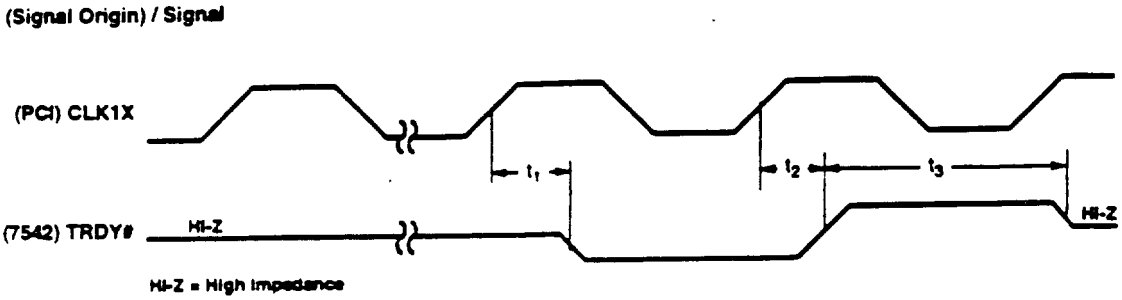


Figure 7–9. PCI Bus: TRDY# Delay Timing

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Table 7–16. PCI Bus: Read Data / IRDY# Timing

Symbol	Parameter	MIN	MAX
t_1	IRDY# Setup to CLK	7ns	–
t_2	IRDY# Hold from CLK	0ns	–

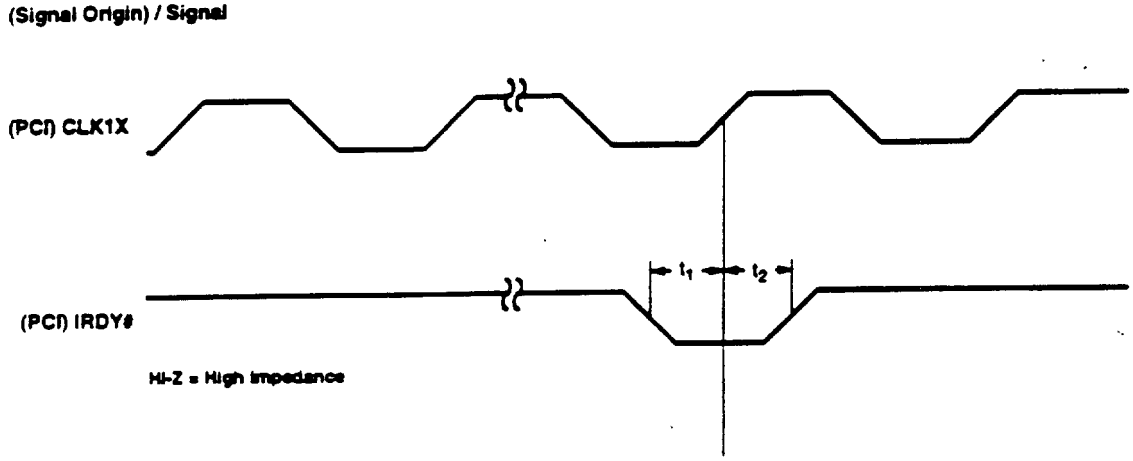


Figure 7–10. PCI Bus: Read Data / IRDY# Timing

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Table 7–17. PCI Bus: STOP# Delay Timing

Symbol	Parameter	MIN	MAX
t_1	STOP# Low Delay from CLK	2ns	11ns
t_2	STOP# High Delay from CLK	2ns	11ns
t_3	STOP# High pulse before HI-Z	1 CLK	–

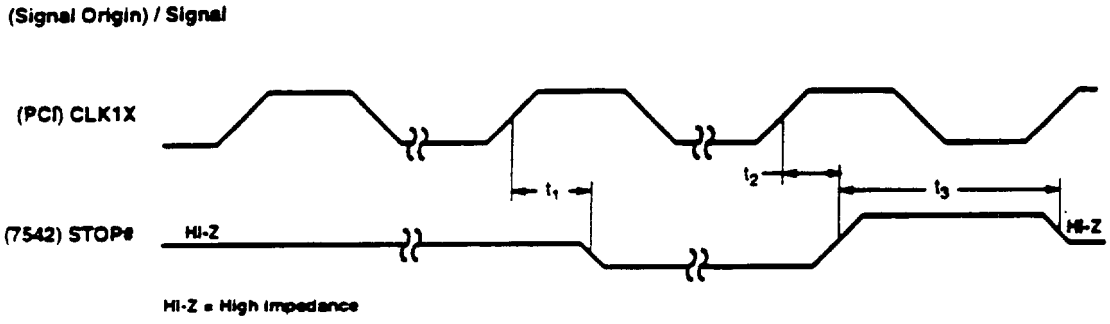


Figure 7–11. PCI Bus: STOP# Delay Timing

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Table 7–18. PCI Bus: IDSEL Timing

Symbol	Parameter	MIN	MAX
t_1	IDSEL Setup to CLK	7ns	–
t_2	IDSEL Hold	0ns	–

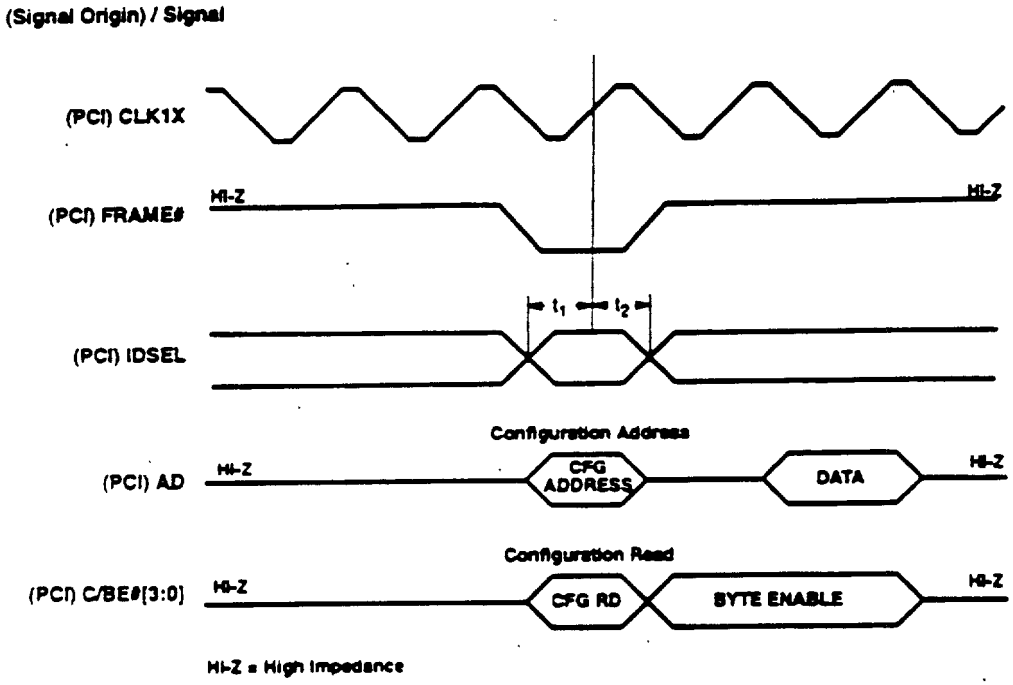


Figure 7–12. PCI Bus: IDSEL Timing

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Table 7–19. PCI Bus: PAR Timing (Write)

Symbol	Parameter	MIN	MAX
t_1	Address PAR Setup from CLK (Input to CL-GD7542)	7ns	–
t_2	Address PAR Hold from CLK (Input to CL-GD7542)	0ns	–
t_3	Data PAR Setup from CLK (Input to CL-GD7542)	7ns	–
t_4	Data PAR Hold from CLK (Input to CL-GD7542)	0ns	–

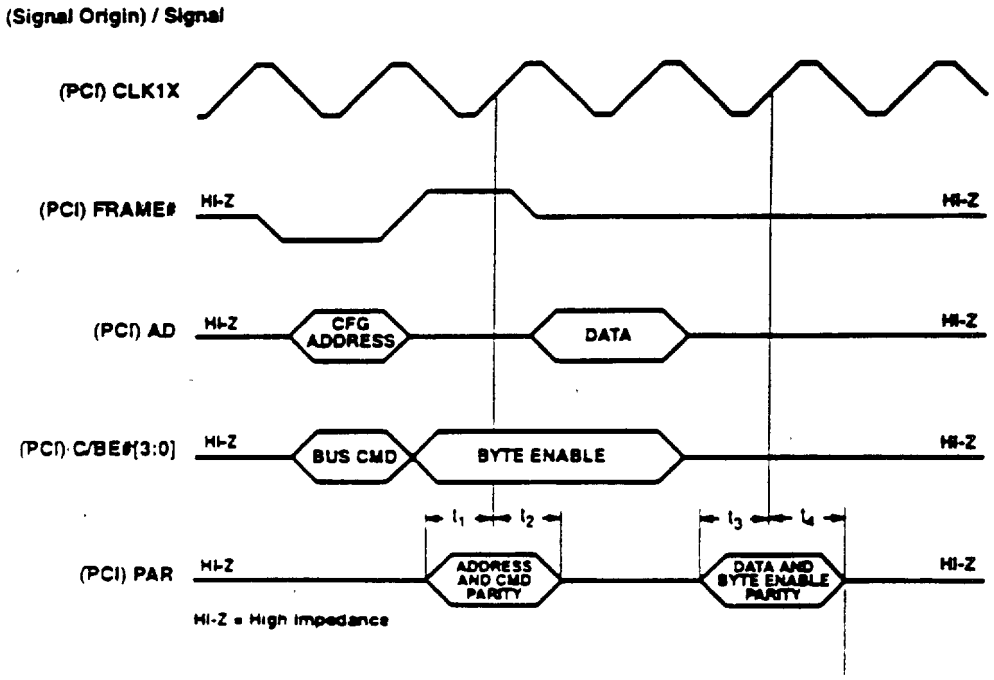


Figure 7–13. PCI Bus: PAR Timing (Write)

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Table 7–20. PCI Bus: PAR Timing (Read)

Symbol	Parameter	MIN	MAX
t_1	PAR Setup from CLK (Input to CL-GD7542)	7ns	-
t_2	PAR Hold from CLK (Input to CL-GD7542)	0ns	-
t_3	PAR Delay from CLK (Output to CL-GD7542)	2ns	11ns
t_4	PAR Off Delay from CLK (Output to CL-GD7542)	-	28ns

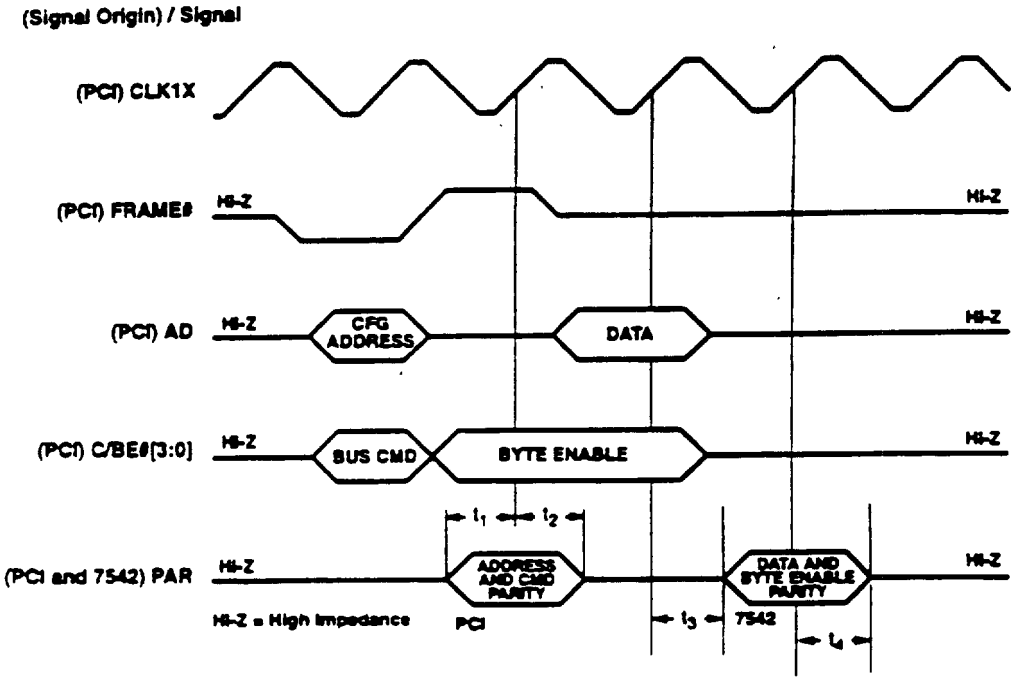


Figure 7–14. PCI Bus: PAR Timing (Read)

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7.4.4 Display Memory Bus: Timing Diagrams

The timing diagrams in this section apply to the CL-GD7542 bus interface to the display memory.

Table 7-21. Display Memory Bus: Read Timing (t^8 = MCLK)

Symbol	Parameter	MIN	MAX
t_1	Address Setup to RAS# Low	1.5t- 9ns	–
t_2	Address Setup to CAS# Low	1.0t - 3ns	–
t_3	RAS# Low to CAS# Low Delay (Standard RAS#)	2.5t - 7.5ns	
t_3	RAS# Low to CAS# Low Delay (Extended RAS#)	3.0t	
t_4	Row Address Hold from RAS# Low	1.5t - 5ns	–
t_5	Column Address Hold from CAS# Low	1.0t	–
t_6	Data Valid from RAS# Low (Standard RAS#)	–	4.0t -1ns
t_6	Data Valid from RAS# Low (Extended RAS#)	–	4.5t -1ns
t_7	Data Valid from CAS# Low	–	1.0t + 3ns
t_8	Data Valid from Column Address Valid	–	2t
t_9	RAS# Precharge (RAS# Pulse Width High) (Std. RAS#)	2.5t + 4.5ns	–
t_9	RAS# Precharge (RAS# Pulse Width High) (Ext. RAS#)	3.0t - 1.5ns	–
t_{10}	Read Cycle Time (Standard RAS#)	6.0t	–
t_{10}	Read Cycle Time (Extended RAS#)	7.0t	–
t_{11}	Read Command Hold from CAS# High	0.5t - 7.5ns	0.5t - 5ns
t_{12}	CAS# Precharge (CAS# Pulse Width High)	1.0t - 6ns	1.0t - 3ns
t_{13}	RAS# Pulse Width Low (Standard RAS#)	3.5t - 8.5ns	–
	RAS# Pulse Width Low (Page-Mode)	–	32µs
t_{14}	CAS# Pulse Width Low	1.0t + 3ns	32µs
t_{15}	Read Data Hold from CAS# High	10ns	–
t_{22}	CAS# Cycle Time	2.0t	–
t_{23}	Read Data Hold from OE# High	10ns	–

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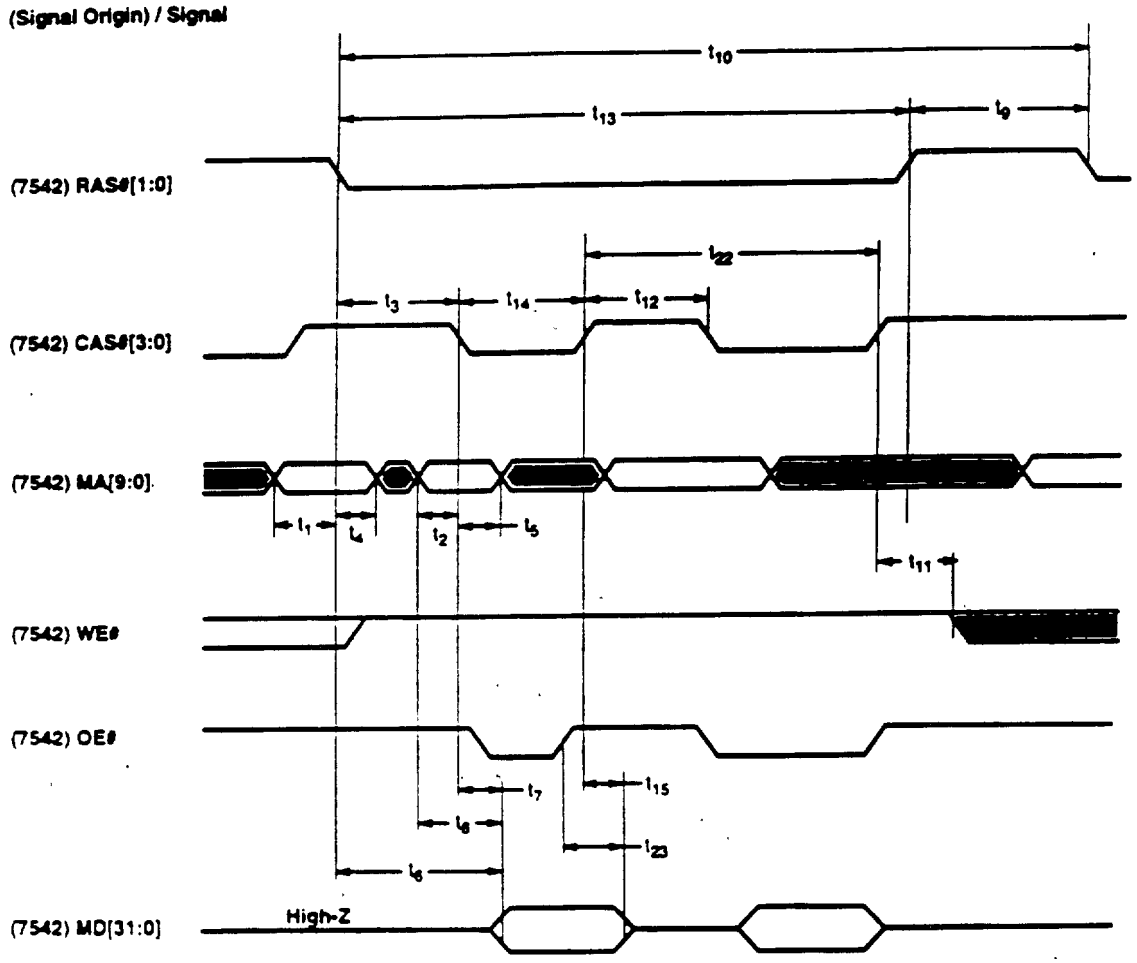


Figure 7–15. Display Memory Bus: Read Timing

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Table 7–22. Display Memory Bus: Write Timing (t^b = MCLK)[a]

Symbol	Parameter	MIN	MAX
t_1	Address Setup to RAS# Low	1.5t - 9ns	–
t_2	Address Setup to CAS# Low	1.5t - 3ns	–
t_3	RAS# Low to CAS# Low Delay (Standard RAS)	2.5t - 7.5ns	–
t_3	RAS# Low to CAS# Low Delay (Extended RAS)	3.0t	–
t_4	Row Address Hold from RAS# Low	1.5t - 5ns	–
t_5	Column Address Hold from CAS# Low	1t	–
t_6	RAS# Precharge (RAS# Pulse Width High) (Std. RAS)	2.5t + 4.5ns	–
t_6	RAS# Precharge (RAS# Pulse Width High) (Ext. RAS)	3.0t - 1.5ns	–
t_7	Write Cycle Time (Standard RAS#)	6.0t	–
t_7	Write Cycle Time (Extended RAS#)	7.0t	–
t_8	CAS# Precharge (CAS# Pulse Width High)	1.0t - 6ns	–
t_{11}	CAS# Cycle Time	2.0t	–
t_{12}	CAS# Pulse Width Low	1.0t + 3ns	32µs
t_{13}	RAS# Pulse Width Low (Standard RAS#)	3.5t - 8.5ns	
	RAS# Pulse Width Low (Page Mode)		32µs
t_{14}	WE# Low Setup to CAS# Low	1.0t - 0.5ns	–
t_{15}	WE# Low Hold to CAS# Low	1.5t - 2ns	–
t_{16}	WE# Low Pulse Width	2.5t - 2ns	–
t_{17}	Write Data Setup to CAS# Low	1.0t + 0.5ns	–
t_{18}	Write Data Hold from CAS# Low	1.0t - 8ns	–

a. The memory interface specifications are valid from 0° to 70° C at operating voltages of 3.3 volts ± 0.3 volts and 5 volts ± 0.5 volts.
b. t = MCLK period: an internal clock.

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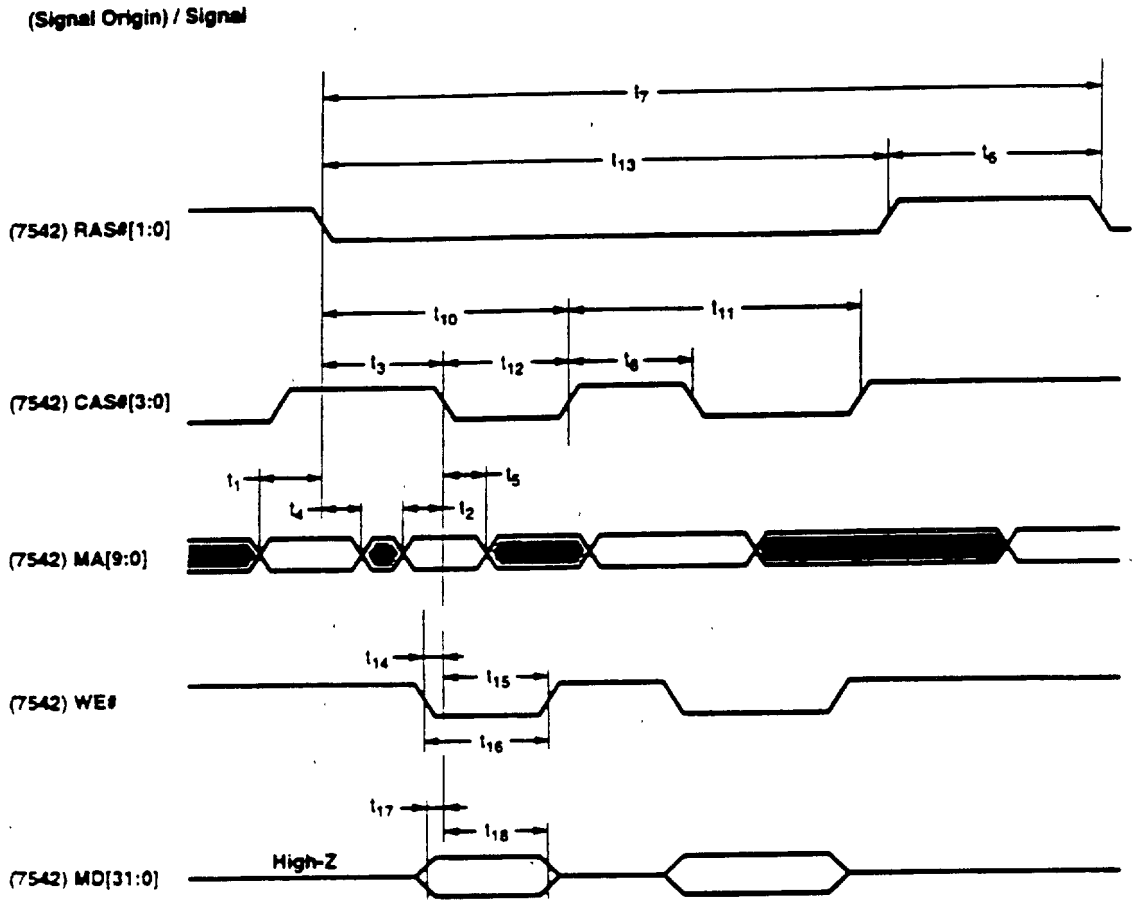


Figure 7–16. Display Memory Bus: Write Timing

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Table 7–23. Display Memory Bus: CAS#-Before-RAS# Refresh Timing[a]

Symbol	Parameter	MIN	MAX	Units
t_1	CAS# Low Setup time to RAS# Active1	1	–	T[b]
t_2	RAS# Low Pulse Width	4	–	T[b]
t_3	RAS# High Pulse Width	3	–	T[b]
t_4	CAS# Hold time for Refresh	1.5	–	T[b]
t_5	Refresh Cycle Period	7	–	T[b]
t_6	CAS# Pulse Width High (Precharge time)	2	–	T[b]
t_7	RAS# High to CAS# Low (Precharge time)	1	–	T[b]

a. There will be either three or five RAS# pulses while CAS# remains Low.
b. T is the MCLK period, an internal clock.

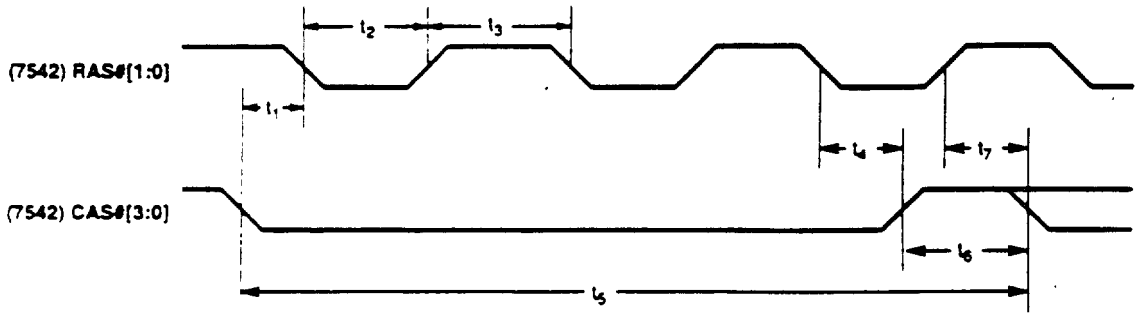


Figure 7–17. Display Memory Bus: CAS#-Before-RAS# Refresh Timing

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7.4.5 Feature Connector: Timing Diagrams

The timing diagrams in this section apply to the CL-GD7542 interface to the Feature Connector (FC).

Table 7–24. Feature Connector: Timing with Clock and Data Driven Externally

Symbol	Parameter	MIN	MAX
t_1	FCP[7:0] Setup to FCVCLK	6ns	–
t_2	FCP[7:0] Hold from FCVCLK	6ns	–

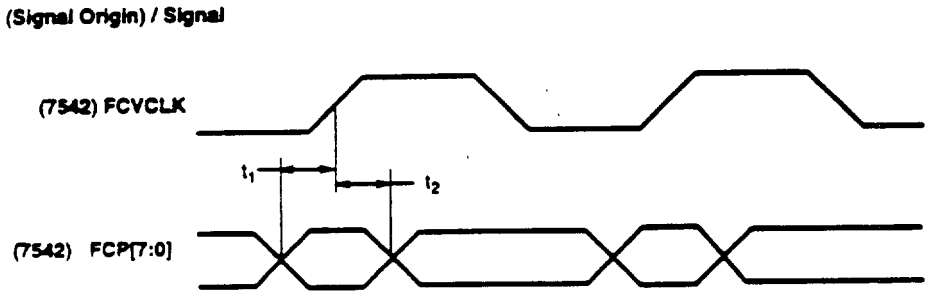


Figure 7–18. Feature Connector: Timing with Clock and Data Driven Externally

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Table 7–25. Feature Connector: FCVCLK Input Timing Requirements

Symbol	Parameter	MIN	MAX
t_1	Rise Time (FCVCLK)	–	3ns
t_2	Fall Time (FCVCLK)	–	3ns
t_3	High Period (FCVCLK)	40% of t_5	60% of t_5
t_4	Low Period (FCVCLK)	40% of t_5	60% of t_5
t_5	Period (FCVCLK)	26ns	–

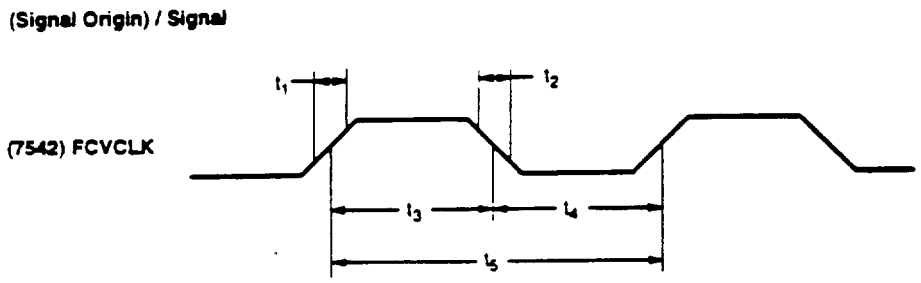


Figure 7–19. Feature Connector: FCVCLK Input Timing Requirements

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7.4.6 LCD Interface: Timing Diagrams

The timing diagrams in this section apply to the CL-GD7542 interface to LCD flat panels.

Table 7-26. LCD Interface: Timing for STN Monochrome and Color-Passive LCD[a]

Symbol	Parameter	M2DD-8	M2SS-8	C8DD-16	C8DD-8	C8SS-16	M2DD-16	C8SS-8
		Mono.	Mono.	Color	Color	Color	Mono. Hi-Res.	Color
t_1	FPVDCLK period	4t	8t	2.5t	t	5t	8t	5t
t_2	FPVDCLK high time	2t - 6ns	4t - 6ns	t - 6ns	0.5t - 6ns	2t - 6ns	4t - 6ns	t - 6ns
t_3	FPVDCLK low time	2t - 6ns	4t - 6ns	t - 6ns	0.5t - 6ns	2t - 6ns	4t - 6ns	4t - 6ns
t_4	FPVDCLK rise and fall time (maximum)	6ns	6ns	6ns	6ns	6ns	6ns	6ns
t_5	Data setup time	2t - 10ns	4t - 10ns	t - 6ns	0.5t - 6ns	2t - 10ns	4t - 10ns	t - 10ns
t_6	Data hold time	2t - 10ns	4t - 10ns	t - 6ns	0.5t - 6ns	2t - 10ns	4t - 10ns	t - 10ns
t_7	FPVDCLK low to LLCLK low	4t - 10ns	8t -10ns	t - 6ns	2t - 10ns	4t - 10ns	8t -10ns	2t - 10ns
t_8	FPVDCLK low from LLCLK low	4t - 10ns	8t - 10ns	t - 6ns	2t - 10ns	4t - 10ns	8t - 10ns	2t - 10ns
t_9	LLCLK high time	3t - 6ns	t - 6ns	3t - 6ns	3t - 6ns	3t - 6ns	t - 6ns	3t - 6ns
t_{10}	LFS high setup to LLCLK low (typical)	2t	t	2t	2t	2t	t	2t
t_{11}	LFS high hold time to LLCLK low (typical)	2t	2t	2t	2t	2t	2t	2t
t_{12}	MOD delay from FPVDCLK high (maximum)	300ns	300ns	300ns	300ns	300ns	300ns	300ns

a Values are MINIMUM unless otherwise specified

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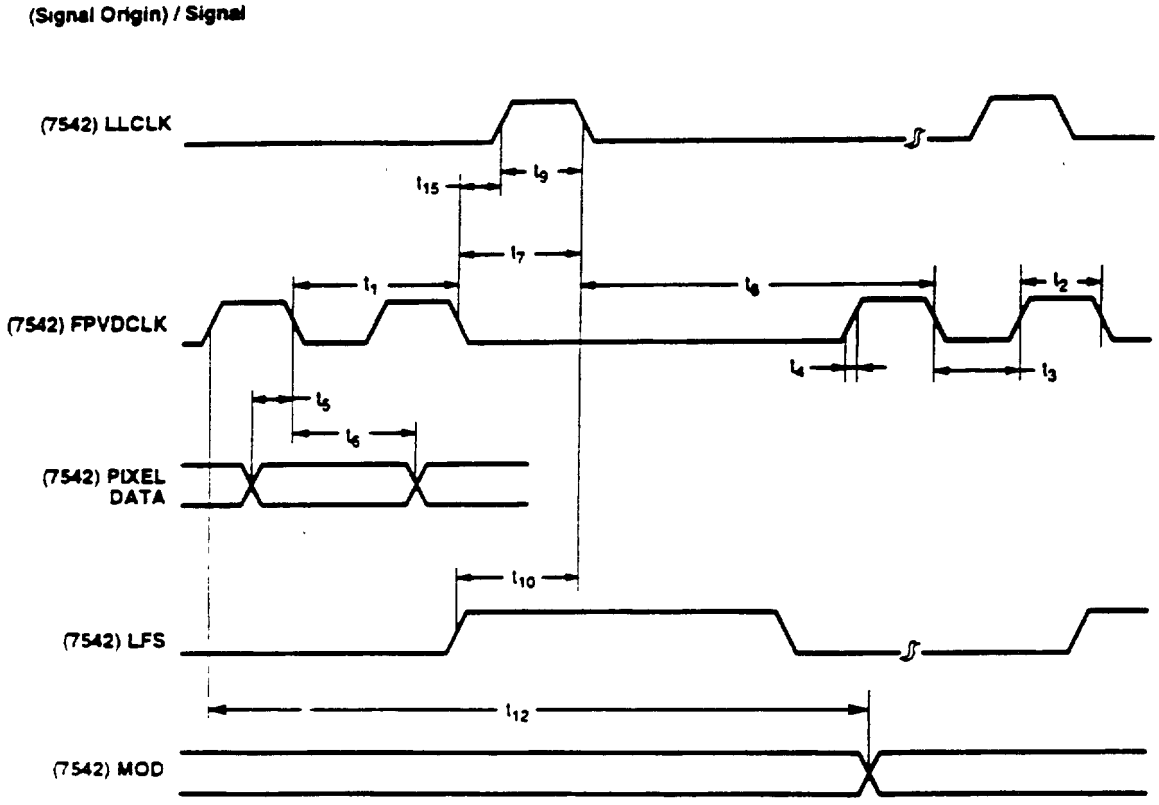
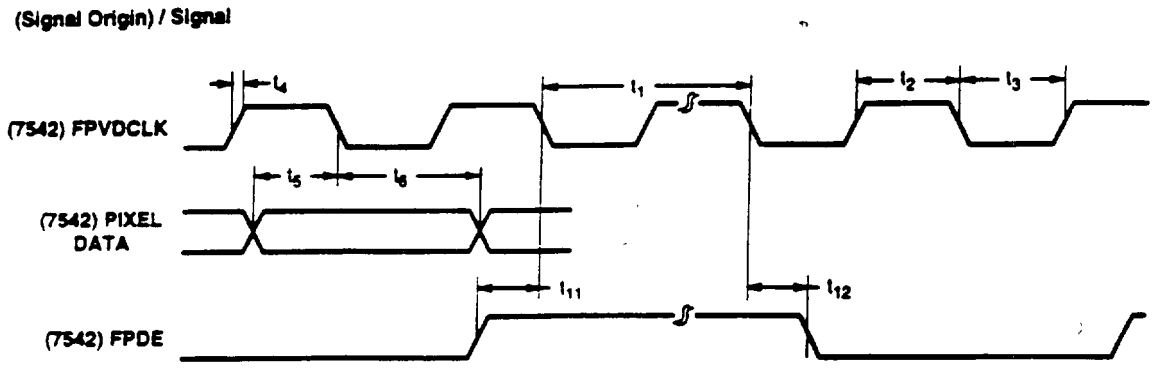


Figure 7-20. LCD Interface: Timing for STN Monochrome and Color-Passive LCD

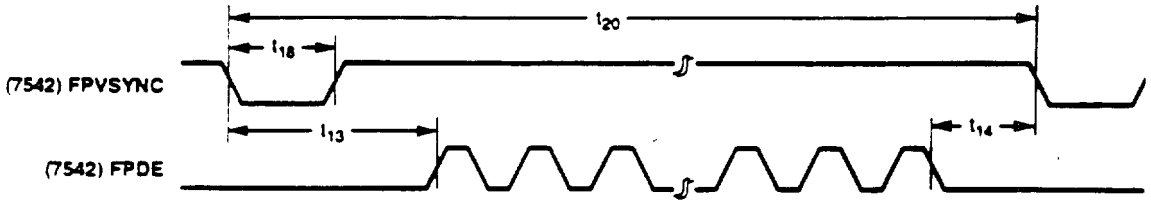
Table 7–27. LCD Interface: Timing for TFT Color LCD

Symbol	Parameter	TFT: C512SS / C4KSS / C256KSS / C16MSS / C64SSI	
		Minimum	Maximum
t_1	FPVDCLK period	t_1	
t_2	FPVDCLK high pulse width	.5t - 6ns	
t_3	FPVDCLK low pulse width	.5t - 6ns	
t_4	FPVDCLK rise and fall time		10ns
t_5	Data setup time	.5t - 6ns	
t_6	Data hold time	.5t - 6ns	
t_7	FPHSYNC setup to FPVDCLK	.25t	
t_8	FPHSYNC hold to FPVDCLK	.25t	
t_9	FPVSYNC setup to FPHSYNC	$1.5t_1$	
t_{10}	FPVSYNC hold to FPHSYNC	$1t_1$	
t_{11}	FPDE setup to FPVDCLK	.25t	
t_{12}	FPDE hold to FPVDCLK	.25t	
t_{13}	Vertical front porch	0 lines	30 lines
t_{14}	Vertical back porch	1 line	31 lines
t_{15}	Horizontal front porch	0ns	$96t_1$
t_{16}	Horizontal back porch	$32t_1$	$128t_1$
t_{17}	FPHSYNC width	$32t_1$	$128t_1$
t_{18}	FPVSYNC width	2 lines	2 lines

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TFT Line Timing



TFT Frame Timing

Figure 7–21. LCD Interface: Timing for Single-Scan TFT Color LCD

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7.4.7 Frequency Synthesizer: Input Timing Diagrams

The timing diagram in this section applies to the inputs to the frequency synthesizer.

Table 7-28. Frequency Synthesizer: Input Timing

Symbol	Parameter	3.3V		5.0V	
		MIN	MAX	MIN	MAX
t_1	Input Clock Rise Time	1 ns	7 ns	1 ns	7 ns
t_2	Input Clock Fall Time	1 ns	7 ns	1 ns	7 ns
t_3	Input Clock Low Period	$t_{CLKP}/2$ - 10% t_5	t_{CLKP} + 10% t_5	t_{CLKP} - 10% t_5	t_{CLKP} + 10% t_5
t_4	Input Clock High Period	$t_{CLKP}/2$ - 10% t_5	t_{CLKP} + 10% t_5	t_{CLKP} - 10% t_5	t_{CLKP} + 10% t_5
t_5	Input Clock Frequency/Period	69.84 ns - 0.1%	69.84 ns + 0.1%	69.84 ns - 0.1%	69.84 ns + 0.1%
V_{IH}	Input High Voltage	2.0 volts	Vcc	2.0 volts	Vcc
V_{IL}	Input Low Voltage	GND	0.5 volts	GND	0.8 volts

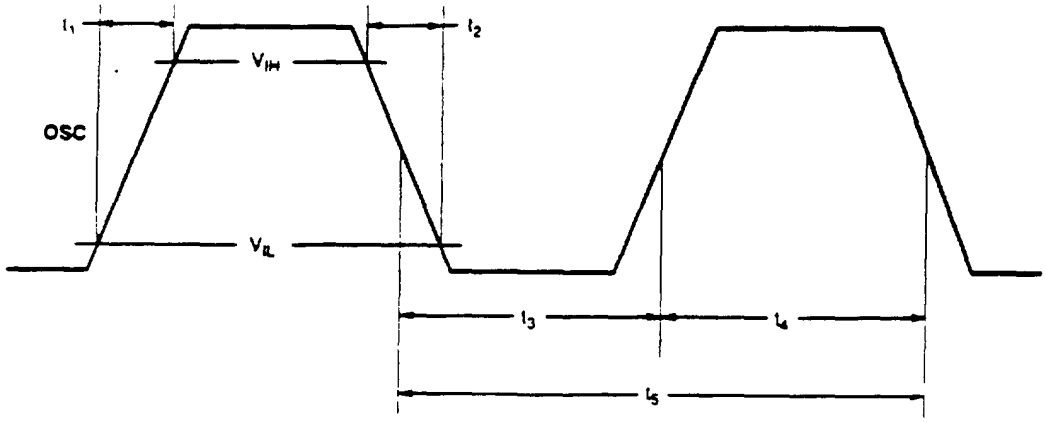


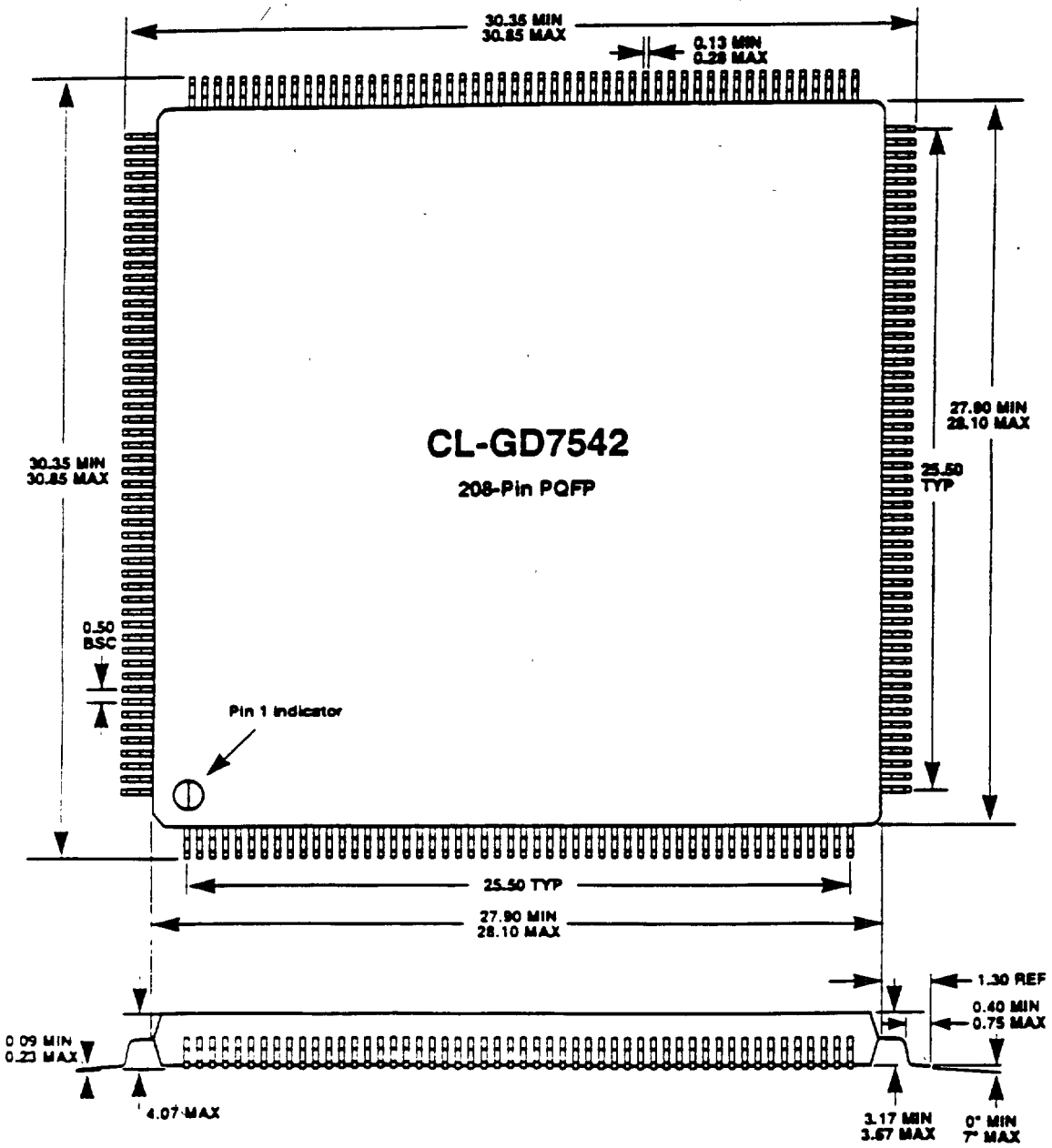
Figure 7-22. Frequency Synthesizer: Input Timing

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8. Package Dimensions



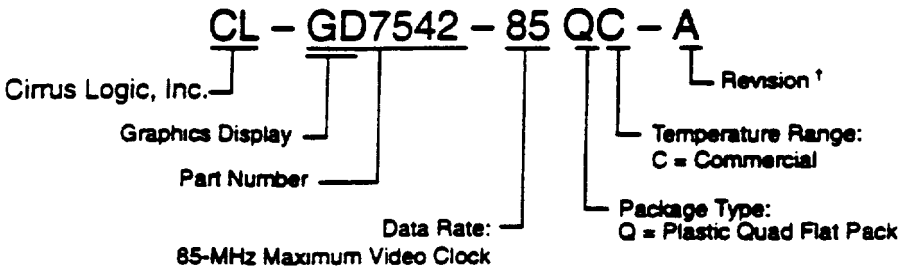
NOTES: 1) All units are in millimeters unless otherwise noted
2) BSC = Basic dimension

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9. Ordering Information

9.1 Package Marking Numbering Guide



† Contact Cirrus Logic, Inc. for up-to-date information on revisions.

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Appendix A1

BitBLT Engine

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A1. BitBLT Engine

A1.1 Introduction

BitBLT (Bit Block Transfer) is an operation in which one area (source area) of display memory or system memory is copied to another area (destination area) of display memory or system memory.

The CL-GD7542's BitBLT engine can not only move bytes from the source area to the destination area but also perform 16 logical raster operations to combine the source bytes with the destination bytes. In addition, it can expand a monochrome image into a color image and replicate a single 8-pixel-by-8-pixel pattern to fill a large area. These operations are done with minimum CPU intervention.

A1.2 Definitions

Source Area:

The source area of a BitBLT is the area from which the data are copied. The source area has the following characteristics:

- located either in display memory or system memory depending on its address.
- may be a monochrome image which is expanded into a color image.
- may be a single 8-pixel-by-8-pixel pattern that is replicated to fill a larger area.

The source area is never written into except in special cases where the source area and the destination area overlap in display memory.

Destination Area:

The destination area of a BitBLT is the area into which the data are written. The destination area may be in display or system memory.

Width:

The width of a BitBLT refers to the number of bytes (not pixels) of destination that are processed before adding the pitch values to the address values. Refer to Figure A1-1.

- When the destination area is on the active display screen (that is, when it is a rasterized area that is displayed), the width is the number of bytes (not necessarily pixels) in each scanline.
- When the destination area is off-screen (or in system memory) and the source is a rasterized area and there is no pattern copy or color expansion, the width is the number of bytes per scanline of the source.
- When neither the destination nor source is a rasterized area, width is simply the number of bytes that are processed before the pitch values are added to the address values, and has no special meaning

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Width is specified in the register pair GR20/GR21. The number written into this register pair is one less than the actual desired width. This value is 11 bits, allowing a maximum width of 2048 bytes.

Height:

The height of a BitBLT refers to the number of times the pitch values are added to the address values. Refer to Figure A1-1.

- When the destination area, source area, or both are on the screen, (that is, when either is a rasterized area that is displayed), the height is the number of scanlines in that area.
- When both areas are off-screen, height is simply the number of times the pitch values are added to the address values, and it has no special meaning. In this case, width and height are simply two numbers that are multiplied together to define the number of bytes in the destination.

Height is specified in the register pair GR22/GR23. This value is 10 bits, allowing a maximum height of 1024 scanlines. The number written into the register pair is one less than the actual desired height. The contents of the registers containing the height are not modified during the operation.

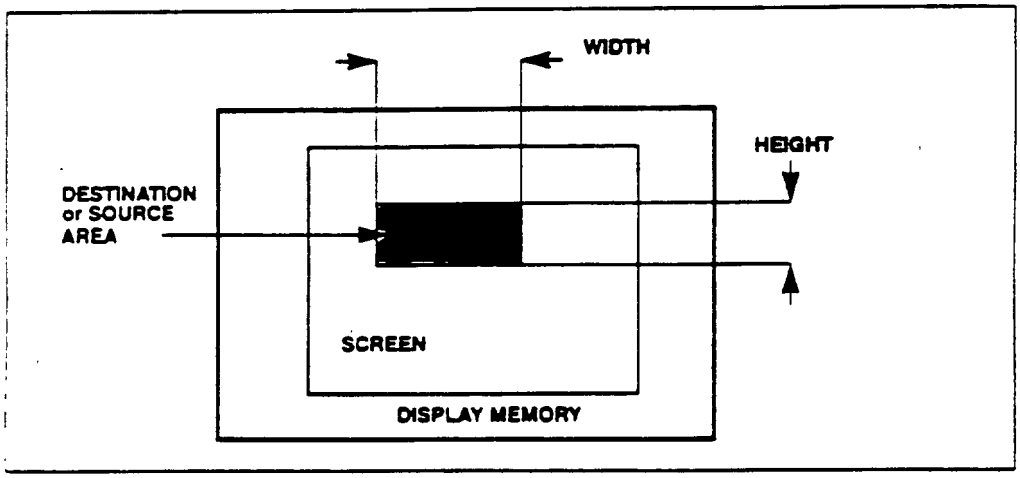


Figure A1–1. Width and Height

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Pitch:

The destination pitch and source pitch are the values that are added to the respective addresses after the bytes of each scanline in a destination area have been processed. For the case of a rasterized image, refer to Figure A1-2. The destination pitch and the source pitch are specified separately.

- When an area is a rasterized image, the respective pitch is the number of bytes between vertically adjacent pixels. This number is the number of bytes between the (first) pixels of scanline 'n' and scanline 'n+1', that is, the number that is added to the address to get from one scanline to the next.
- When an area is off-screen display memory, the scanlines are often stored in contiguous locations, which minimizes fragmentation. In this case, the respective pitch would be set equal to (width +1).
- When an area is in system memory, the respective pitch is unused and is a 'don't care'.

When executing BLTs with pattern copy or color expansion, the source area is assumed to be linear, and the source pitch is a 'don't care'.

- The source pitch is specified in register pair GR26/GR27.
- The destination pitch is specified in register pair GR24/GR25.

For the CL-GD7542, both register pairs are 12-bit values, allowing a pitch of 4095 bytes.

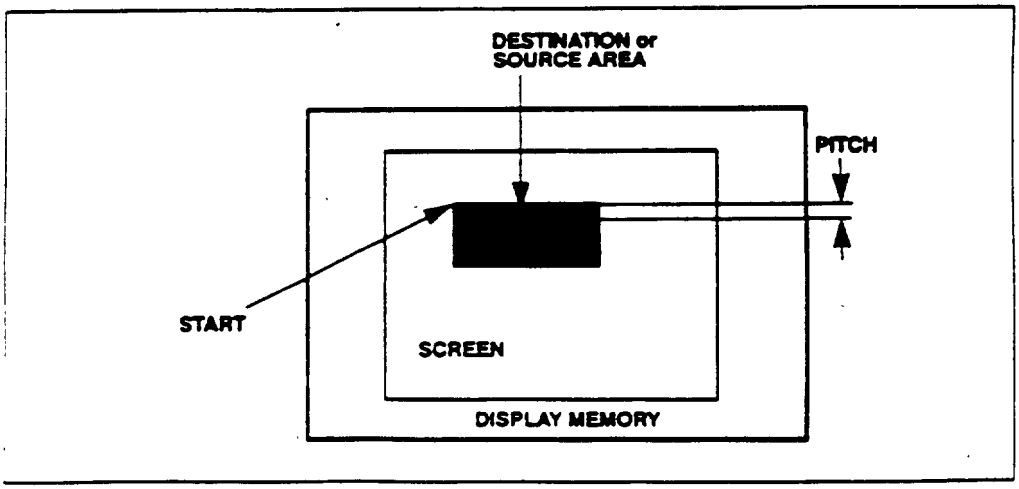


Figure A1–2. Pitch and Start

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Start:

Start refers to the address of the first byte of a destination or source area, which is a byte offset from the beginning of display memory. Refer to Figure A1-2.

- The destination area start address is specified in register triplet GR28 / GR29 / GR2A.
- The source area start address is specified in register triplet GR2C/GR2D/GR2E.

Each start address is a 21-bit value, allowing up to 2 Mbytes of display memory. The destination-start address is shown in Figure A1-2.

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A1.3 Example of Display-Memory-To-Display-Memory BitBLT

Table A1-1 shows how the BLT registers must be programmed for a very simple BLT operation of copying a 128-byte x 64-scanline area into display memory. In this example, the CL-GD7542 is assumed to be programmed in video mode 65 (800 x 600, 16-bits per pixel). Therefore, each 128-byte scanline represents 64 pixels. The source area of this operation begins at location 0. The destination area begins at location 160200 (100 scanlines from the top of the screen, 100 pixels from the left edge).

Table A1–1. Register Programming for Source Copy BitBLT Operation

Register(s)	Contents	Field	How Calculated
GR0 / GR10	Don't care	Background color	-
GR1 / GR11	Don't care	Foreground color	-
GR20 / GR21	127 (decimal)	Width	(64 x 2) -1
GR22 / GR23	63 (decimal)	Height	64 - 1
GR24 / GR25	1600 (decimal)	Destination Pitch	800 x 2
GR26 / GR27	1600 (decimal)	Source Pitch	800 x 2
GR28 / GR29 / GR2A	160200 (decimal)	Destination Start	(100 x 1600) + (100 x 2)
GR2C / GR2D / GR2E	0 (decimal)	Source Start	Beginning of display memory
GR30	00 (hex)	BLT Mode	Display to display No color expansion No pattern copy
GR31	02 (hex)	Start / Status	Set bit 1 to 1
GR32	0D (hex)	Raster Operation	Source Copy

This BLT is executed as indicated in the following fragment of pseudo-code:

```
sourceAdrs = sourceStartAdrs;
destAdrs = destStartAdrs;
for (i = 0; i < Height; i++)          /*for each scanline*/
    {
    workingSourceAdrs = sourceAdrs
    workingDestAdrs = destAdrs
    for (j =0; j < Width; j++)        /*for each byte*/
        {
        Process one byte of Destination;
        workingDestAdrs++;            /*to next byte*/
        workingSourceAdrs++;
        }
    sourceAdrs = sourceAdrs + sourcePitch; /*next scanline*/
    destAdrs = destAdrs + destPitch;
```

The BLT engine processes the bytes of a scanline in a destination area, incrementing temporary source and destination addresses after each byte. Multiple bytes are processed in parallel. At the end of each scanline, the respective pitch values are added to the addresses as they were at the beginning of the scanline, moving on to the next scanline. This operation is iterated for the "height" number of times.

All BitBLTs are processed in this general manner. However, some variations include the following:

- For color expansion, the source address is incremented as a bit address rather than a byte address.
- For pattern copies, the source address is incremented until the end of the pattern and is returned to the the source start address, so that the pattern is used over and over.
- When the decrement bit is set, the address is decremented rather than incremented.

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A1.4 Raster Operations (ROPS)

In addition to moving bytes from the source area to the destination area, the CL-GD7542's BitBLT engine can use various logical raster operations to combine the source or pattern bytes with the destination bytes. Further, bytes in either the source area or the destination area, or both, can be ignored.

Table A1-2 enumerates the 16 ways in which the source bit (or the pattern bit) and the destination bit can be logically combined. The same value for GR32 is used regardless of whether the operation uses Source or Pattern.

The CL-GD7542's BitBLT engine directly implements all 16 ways of logically combining two operands as shown in Table A1-2. Combinations of three operands can be synthesized from these in the unusual cases where this is necessary.

Table A1–2. Logical Combinations of Bits Using the BitBLT Engine

Source Operation	Microsoft® Name / Raster Operation	Pattern Operation	Microsoft® Name / Raster Operation	GR32 (Hex)
0	BLACKNESS 00000042	0	BLACKNESS 00000042	00
~S.~P	NOTSRCERASE 001100A6	~P.~S	- 000600A9	90
~S.D	- 00220326	~P.D	- 000A0329	50
~S	NOTSRCCOPY 00330008	~P	- 000F0001	D0
S.~D	SRCERASE 00440328	P.~D	- 00500325	09
~D	DSTINVERT 00550009	~D	DSTINVERT 00550009	0B
S~=D	SRCINVERT 00660046	P~=D	PATINVERT 005A0049	59
~S+D	- 007700E6	~P+D	- 005F00E9	DA
S.D	SRCAND 008800C6	P.D	- 00A000C9	05
S=D	- 00990066	P=D	- 00A50065	95
D	- 00AA0029	D	- 00AA0029	06
~S+D	MERGEPAINT 00BB0226	~P+D	- 00AF0229	D6
S	SRCCOPY 00CC0020	S	PATCOPY 00F00021	0D
S+~D	- 00DD0228	P+~D	- 00F50225	AD
S+D	SRCPAINT 00EE0086	P+D	- 00FA0089	6D
1	WHITENESS 00FF0062	1	WHITENESS 00FF0062	0E

NOTE S = Source, D = Destination, P = Pattern.

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A1.5 Color Expansion

When GR30[7] is 1, the source input to the ROPS is not actual data from the source area, but is *color-expanded* data. The source area is a monochrome image. Since the source image is a single bit per pixel, substantial performance benefits are possible, especially when the source is being expanded to 16 bits. Color expansion can be used any time a single foreground color, or a single foreground color and a single background color, are to appear in the destination.

The CL-GD7542 supports color expansion for 8-bit-per-pixel and 16-bit-per-pixel modes. The source can be monochrome data from either display memory or system memory. When the source is in display memory, it must be located on a four-byte boundary. When the source is an 8 x 8 pattern, it must be on an eight-byte boundary.

- A 1 in the source area results in the *foreground* color being written into the corresponding byte(s) of the destination area.
- A 0 in the source area results in either the *background* color being written into the corresponding byte(s) of the destination area, or no alteration to the destination area (transparency).

For color expansion, the destination must be in the display memory that is displayed and the direction must be increment. Any ROP may be used, although SRCCOPY is most common when using color expansion.

The most-significant bit of the first source byte is expanded into the ROP source data for the first pixel of the destination. Depending on the contents of GR30[4], it is expanded to one or two bytes. Table A1-3 indicates the registers that contain the expansion colors.

Table A1–3. Color Expansion Registers

GR30[4]	Width	Background Expansion (0 in Source Area)		Foreground Expansion (1 in Source Area)	
		GR0	GR10	GR1	GR11
0	8-bit	Color	Don't care	Color	Don't care
1	16-bit	Low byte	High byte	Low byte	High byte

The next bit of source data is processed for the next one or two bytes of destination, and so on, until the bytes of the scanline in the destination area have been processed. Unused source bits are discarded

The destination address is modified by the destination pitch. The source pitch is ignored since the source is taken to be a linear string of bytes The next byte of source is the first eight pixels for the next scanline

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A1.6 Color Expansion With Transparency

When GR30[3] is 1, transparency comparison is enabled. Results of a ROP are compared to the contents of the Transparent Color Registers (GR34 / 35) for each pixel. When the results are compared in all bit positions for which the Transparent Compare Mask Registers (GR38/39) are 0, the results are *not* written to display memory. In 8 bits/pixel modes (GR30[4] = 0), registers GR34 and GR35 *must* be programmed identically, as must GR38 and GR39.

When color expansion is used with an opaque foreground and a transparent background (analogous to Extended Write mode 4), the transparency feature must be used, and the transparent color must be set to the background color. The registers used for foreground color expansion with transparency are the same as the color expansion registers with 1 in the source. (Refer to Figure A1-3.)

A1.7 Pattern Fills

In some cases it is necessary to fill an area with a repeating pattern. The CL-GD7542 BitBLT engine has provisions for pattern replication with or without color expansion. The pattern size is 8 pixels x 8 pixels, chosen for compatibility with Microsoft Windows.

When GR30[6] is 1, the source is defined as an array of 8 pixels x 8 pixels. This array is repeatedly copied to the destination area, with color expansion if necessary. For any scanline, the same eight pixels of source data are used repeatedly. The source pitch is ignored. The number of bytes in the source pattern is a function of the operating mode, as indicated in Table A1-4. The starting address boundary of a source pattern is equal to the number of bytes.

Table A1-4. Pattern-Fill Data Size

Operating Mode	Number of Bytes in Source Pattern	Starting Address Boundary
Color Expansion	8 bytes of monochrome data for 64 pixels	8 bytes
8-bit pixels	64 bytes of color data for 64 pixels	64 bytes
16-bit pixels	128 bytes of color data for 64 pixels	128 bytes
32-bit pixels	256 bytes of color data for 64 pixels	256 bytes

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A1.8 BLT Direction

If source and destination areas overlap in display memory, as explained below, ensure that the BitBLT operation progresses so that the source area is not overwritten prior to being used.

Refer to Figure A1-3. If the BitBLT operation were to begin with the upper-left corner of the source and destination, the contents of the overlapped area would be overwritten before being used.

To avoid this effect, GR30[0] must be set to 1 so that the direction in which the BitBLT operation progresses is reversed. As shown in Figure A1-3, the bytes are therefore processed right to left and bottom to top, guaranteeing that bytes of the source are used prior to being changed. Note that in this case, the start addresses are the highest in the areas, not the lowest.

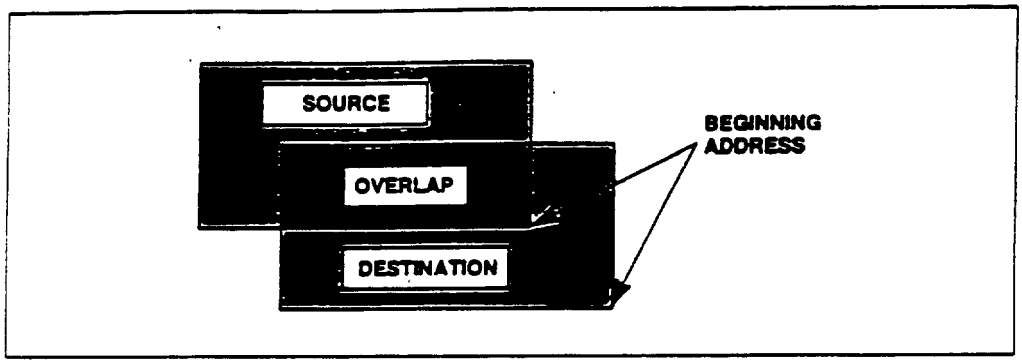


Figure A1–3. Source and Destination Memory Area Overlap – Start Address

A1.9 System Memory

The source area or the destination area, but not both, of a BitBLT can be in system memory. In either case, the CPU must perform the bus transfers in that the CL-GD7542 is never a bus master. For such transfers, the address provided by the CPU is ignored (except it must be in the range being decoded as display memory). The CPU *must* execute DWORD transfers.

- When GR30[2] is a 1, the BLT source is system memory.
  - For system-to-screen BitBLTs, up to three bytes of the last transfer for each scanline are ignored (depending on width of the source and the destination areas). The next scanline begins with the next DWORD transfer.
- When GR30[1] is a 1, the BLT destination is system memory.
  - The CL-GD7542 pads each scanline with up to three indeterminate bytes (depending on width of the source and the destination areas). BLTs involving color expansion or pattern copy cannot use this mode

A1.10 Start / Suspend / Reset Controls

Once the parameters have been loaded into the registers, the BitBLT can be started, suspended, and then resumed. It is also possible to unconditionally reset the BitBLT engine. These functions are controlled by bits in GR31.

- To start a BitBLT, program GR31[1] to 1. As long as the BLT is in progress, GR31[0] is a 1. When the BLT has completed, GR31[0] changes to a 0.

  Monitoring GR31[0] is the most straight-forward way to synchronize with the BitBLT engine. While the BLT is in progress, the CL-GD7542 display memory and BLT registers (except GR31) must not be accessed for read or write.

- To suspend a BLT, program GR31[1] to 0. Register GR31[0] must be monitored to determine when the BLT has actually been suspended, and it is safe to access display memory. When register GR31[0] is a 0, then the BLT has been successfully suspended or has been completed.

  When a BLT has been suspended, the CPU may access display memory only for write operations. If the program reads display memory during a suspended BLT, working registers are overwritten, and the first few bytes of the BLT will use invalid data, when it is resumed.

  The CPU can determine whether a suspended BLT was actually suspended, or gone to completion coincidentally with the suspension, by reading GR31[3].
  - When GR31[3] is a 1, the BLT was suspended and must be resumed.
  - When GR31[3] is a 0, the BLT was actually completed and need not be resumed.

- To resume, the BLT is resumed by programming GR31[1] to 1. BLTs can be suspended and resumed multiple times.

- To unconditionally stop the current operation, and reset the entire BitBLT engine, programGR31[2] to 1. GR31[3] and GR31[0] are forced to 0 and the operation stops after the next write. This operation may result in partial pixels being written.

  Note that BitBLT operation that is reset *cannot* be resumed.

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A1.11 Complete BLT Register Listing

Table A1-5 lists every register associated with the BitBLT engine.

Table A1–5. BLT Register Listing

Register	How Used	Size (Bits)	Modified?
GR0	Background Color byte 0	8	No
GR1	Foreground Color byte 0	8	No
GR10	Background Color byte 1	8	No
GR11	Foreground Color byte 1	8	No
GR20	Width byte 0	8	–
GR21	Width byte 1	3	–
GR22	Height byte 0	8	Yes
GR23	Height byte 1	2	Yes
GR24	Destination Pitch byte 0	8	No
GR25	Destination Pitch byte 1	4	No
GR26	Source Pitch byte 0	8	No
GR27	Source Pitch byte 1	4	No
GR28	Destination Start byte 0	8	Yes
GR29	Destination Start byte 1	8	Yes
GR2A	Destination Start byte 2	5	Yes
GR2B	Reserved		
GR2C	Source Start byte 0	8	Yes
GR2D	Source Start byte 1	8	Yes
GR2E	Source Start byte 2	5	Yes
GR2F	Destination Write Mask	3	No
GR30	BLT mode	8	No
GR31	Start/Status	4	–
GR32	Raster Operation	8	No
GR34	Transparent Color – Low Byte	8	No
GR35	Transparent Color – High Byte	8	No
GR38	Transparent Color Mask – Low Byte	8	No
GR39	Transparent Color Mask – High Byte	8	No
SR2	Plane Mask	8	No

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A1.12 BLT Registers modified While BLT Is Occuring

Some registers associated with a BLT are modified while the BLT is occurring. Therefore, they must be re-written prior to the next BLT, even when the initial values are to be the same.

A1.13 Text Expansion Example

Using color expansion, a text string is copied from system memory, resulting in faster test-write operations. The monochrome image of the string is arranged in system memory by scanline. For example, assume that the destination area is 150 pixels x 25 scanlines, 8 bits per pixel. The destination pitch is 1024 pixels. The registers must be loaded as indicated in Table A1-6. When the background pixels are not to be written, GR30[3] must be set to 1.

Table A1–6. Typical Register Settings for Color-Text Expansion

Register(s)	Register Contents (Decimal)	Register Description	How Calculated?
GR0 / GR10	Don't Care	Background Color	-
GR1 / GR11	Don't Care	Foreground Color	-
GR20 / GR21	149 (decimal)	Width	150 - 1
GR22 / GR23	24 (decimal)	Height	25 - 1
GR24 / GR25	1024 (decimal)	Destination Pitch	-
GR26 / GR27	n/a	Source Pitch	(System memory)
GR28 / GR29 / GR2A	Don't Care	Destination Start	-
GR2C / GR2D / GR2E	n/a	Source Start	(System memory)
GR30	84 (hex)	BLT Mode	Color Expansion, Source = System Memory
GR31	02 (hex)	Start / Status	Set bit 1
GR32	0D (hex)	Raster Operation	SRC COPY

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After the registers are loaded, the source bitmap must be transferred.

- The first DWORD write transfers the image for pixels 0 to 31.
- The second write transfers the image for pixels 32 to 63.
- The third transfers the image for pixels 64 to 95.
- The fourth transfers the image for pixels 96 to 127.
- The data sent in the fifth DWORD transfer is shown in Figure A1-4.

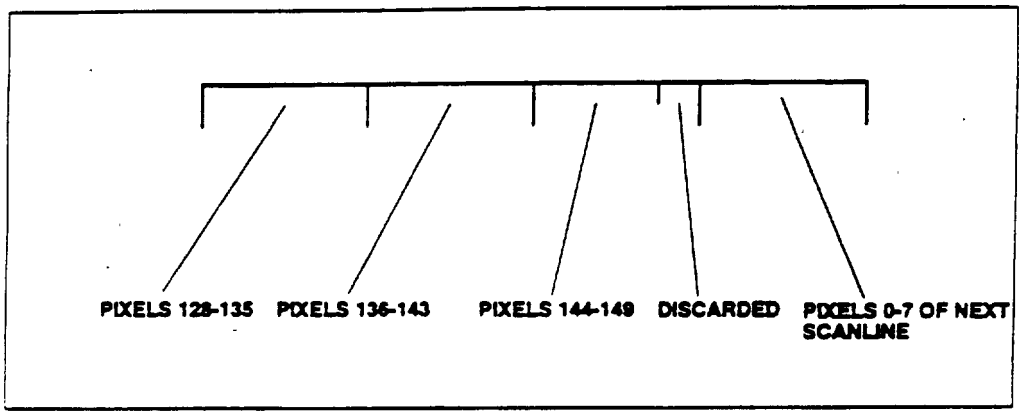


Figure A1–4. Color Expand Transfer

A total of 119 DWORD transfers are required. The last one byte of the last transfer is discarded.

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Appendix A2

Hardware Cursor

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A2. Hardware Cursor

A2.1 Introduction

The CL-GD7542 is capable of supporting a 32 x 32 or 64 x 64 hardware cursor (mouse pointer) in 16-color planar, 256-, 32K-, and 64K-color packed-pixel graphics modes.

Multiple hardware cursor patterns can be loaded into the upper display memory area, allowing application programs to select one of the patterns as an active-cursor pattern.

The hardware cursor (mouse pointer) replaces a software mouse pointer commonly used by Graphics User Interface (GUI) applications. The hardware cursor eliminates the need for application software to save and restore the screen data as the mouse pointer position changes.

After initializing the hardware cursor, the application software needs only to update the cursor position (x,y) to move the cursor on the screen. Compared to a software cursor, the hardware cursor offers a smooth-moving mouse pointer with improved performance.

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A2.2 Hardware Cursor Operation

Each pixel in the hardware cursor consists of two bits: bit 1 and bit 0. The following table shows how the two bits determine the displayed data of each cursor pixel.

Table A2–1. Hardware Cursor Bits

Bit 0	Bit 1	Displayed Data of Hardware Cursor Pixel
0	0	Transparent
0	1	Inverted VGA Display Data
1	0	Cursor color 0
1	1	Cursor color 1

The cursor colors 0 and 1 are supplied by the internal palette DAC's two extra Lookup Table (LUT) locations which are mapped into the existing LUT indexes 00h and 0Fh, respectively. As a result, the hardware cursor colors are independent of the existing LUT indexes 00h through FFh.

The CL-GD7542 extension register SR12, the Video Datapath Control Register, can be programmed:

- to enable or disable the cursor
- to select the cursor size
- to enable access to the Palette DAC cursor colors
- to enable cursor movement

The hardware cursor data is located in the top 8 Kbytes of the display memory. The number of cursor patterns that can be loaded in the display memory at one time is either 32 (for 32 x 32 bit cursors) or 8 (for 64 x 64 bit cursors). One of the cursor patterns loaded in display memory is selected as the active-cursor pattern using the Graphics Cursor Pattern Address Offset Register (SR13).

The hardware cursor position is controlled by programming the hardware cursor horizontal (X) position and hardware cursor vertical (Y) position. The 11-bit cursor X-location and Y-location values are programmed by initiating two 16-bit I/O writes to.

1 SRX (3C4h) and SR10 (3C5h): Horizontal position
2 SRX (3C4h) and SR11 (3C5h): Vertical position

where the SRX[7:5] bits of the Index Register are the least-significant bits of the 11-bit value, and the SRX[4.0] bits are the index into the horizontal and vertical position registers. Moving the cursor always requires writing to both the horizontal and vertical position registers.

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The horizontal position is written first but does not take effect until the vertical position is updated.

NOTE: The horizontal fine-position control requires one more bit for those expanded-graphics modes that use 10-dot character clocks. For these special cases (for example, 640 x 480 graphics expanded for 800 x 600 LCDs), the most-significant bit for the fine-position adjustment is in SR2E[0], which is appended to the index bits SRX[7:5]. For standard non-expanded graphics modes, SR2E[0] is always 0 and can be ignored when moving the cursor.

The following table shows the CL-GD7542 Extension Registers bits that are needed for programming the hardware cursor:

Table A2–2. Extension Registers Bits For Programming Hardware Cursor

To:	Program:			
	Index or Extension Register	I/O Port Address	Register Bits	Value
Enable hardware cursor	SR12	3C5h	[0]	1
Access graphics palette DAC colors	SR12	3C5h	[1]	1
Set hardware cursor size (32 x 32)	SR12	3C5h	[2]	0
Set hardware cursor size (64 x 64)	SR12	3C5h	[2]	1
Enable hardware cursor movement	SR12	3C5h	[3]	0
Select hardware cursor pattern (32 x 32)	SR13	3C5h	[4:0]	31..0
Select hardware cursor pattern (64 x 64)	SR13	3C5h	[4:2]	7.0
Set hardware cursor horizontal position	SRX/SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]/[7:0]	2047..0
Set hardware cursor horizontal position fine-position extension (msb) for expanded graphics	SR2E	3C5h	[0]	0:Non-Exp. 1:Expanded
Set hardware cursor vertical position	SRX/SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:5]/[7:0]	2047..0
Enable 64 x 64 hardware cursor memory mapping	SR21	3C4h/3C5h	[4]	1

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A2.3 The 32 X 32 Hardware Cursor

Each 32 x 32 cursor pattern requires 256 bytes (128 bytes per cursor pixel bit x 2 cursor pixel bits), which allows for 32 cursor patterns to be loaded into 8 Kbytes of the hardware cursor data area in the display memory. The active cursor pattern is selected by programming the Graphics Cursor Pattern Address Register bits (SR13[4:0]).

The hardware cursor data and the hardware icon data are loaded into the top 16 Kbytes of the display memory as follows:

- The hardware icon data is loaded into the top 8 Kbytes of the display memory.
- The hardware cursor data is loaded into the next 8 Kbytes of the display memory.

For more information about the hardware icon, refer to Appendix 3.

The 32 x 32 hardware cursor pattern data from cursor pixel bit 0 and cursor pixel bit 1 is loaded into the display memory as shown in the following figure:

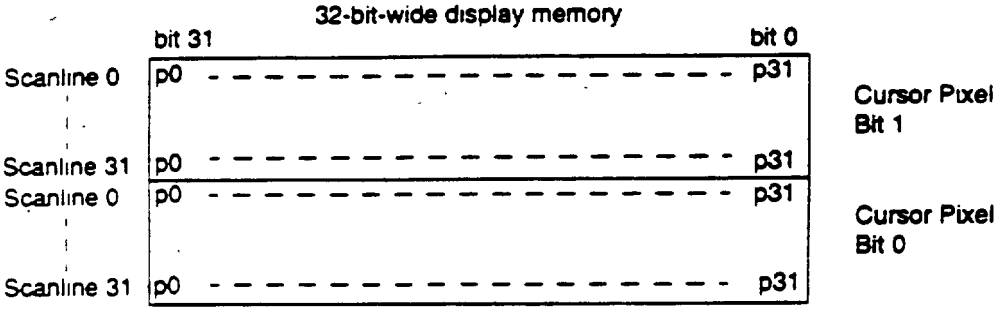


Figure A2—1. Mapping of 32 x 32 Hardware Cursor

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A2.4 The 64 x 64 Hardware Cursor

Each 64 x 64 cursor pattern requires 1024 bytes (512 bytes per cursor pixel bit x 2 cursor pixel bits), which allows for 8 cursor patterns to be loaded into 8K of the hardware cursor data area. The active hardware cursor pattern is selected by programming the Graphics Cursor Pattern Address Register bits (SR13[4:2]).

The 64 x 64 hardware cursor pattern data from cursor pixel bit 0 and cursor pixel bit 1 is loaded into display memory one cursor scanline at a time. The same action takes place until all 64 scanlines from cursor pixel bit 0 and cursor pixel bit 1 are loaded into the system memory as shown in the following figure:

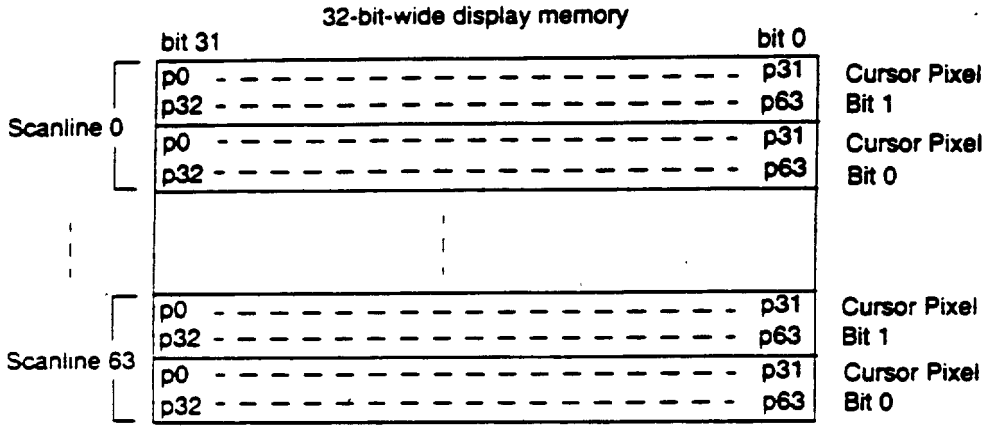


Figure A2-2. Mapping of 64 x 64 Hardware Cursor

To get proper 64 x 64 hardware cursor mapping, Extension Register SR21[4] bit must be set to 1.

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The following table shows the location of the hardware cusrsor memory map within the display memory.

Table A2–3. Hardware Icon Memory Map in 1-Mbyte Display Memory

Address	32 x 32 Hardware Cursor	64 x 64 Hardware Cursor
3FF00-3FFFF	Cursor Map #28 - Cursor Map #31	Cursor Map #7
3FE00-3FEFF	Cursor Map #24 - Cursor Map #27	Cursor Map #6
3FD00-3FDFF	Cursor Map #20 - Cursor Map #23	Cursor Map #5
3FC00-3FCFF	Cursor Map #16 - Cursor Map #19	Cursor Map #4
3FB00-3FBFF	Cursor Map #12 - Cursor Map #15	Cursor Map #3
3FA00-3FAFF	Cursor Map #8 - Cursor Map #11	Cusor Map # 2
3F900-3F9FF	Cursor Map #4 - Cursor Map #7	Cursor Map #1
3F800-3F8FF	Cursor Map #0 - Cursor Map #3	Cursor Map #0

NOTE: For the 32 x 32 hardware cursor, four hardware-cursor data patterns occupy 3Fx00 through 3FxFF. Their respective addresses (x = 8 - F) are:
3Fx00 - 3Fx3F
3Fx40 - 3Fx7F
3Fx80 - 3FxBF
3FxC0 -3FxFF

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Appendix A3

Hardware Icon

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A3. Hardware Icon

A3.1 Introduction

A hardware icon (a hardware-driven icon window), as compared to a software icon, eliminates the need for application software to save and restore the screen data as the icon position changes.

In various operational modes, the CL-GD7542 Super VGA LCD Controller is capable of supporting four hardware icons with the following features:

- One to four icons displayed simultaneously on the screen.
- Icon size is 64 x 64 pixels.
- Icon size can be doubled vertically and/or horizontally to 64 x 128- 128 x 64-, and 128 x 128- pixels.
- Up to eight icon maps may be defined in display memory for use and are associated with the displayed hardware icons in two ways:
  - Two maps for each hardware icon
  - All eight maps used with the first hardware icon.
- A single location known as a hot spot is used to define the screen position of all of the icons. This hot spot defines the upper left-hand corner of the first icon. All subsequent icons are left aligned vertically down from the first icon.
- The hot spot is positioned at a resolution of one pixel.
- Each icon independently controls the following:
  - Display Enable
  - Display Mode: 4 colors, or 3 colors + transparency
  - Blink Enable: at either blink rate, or at one-half the icon blink rate
  - Horizontal Pixel Doubling
  - Vertical Pixel Doubling
  - Memory Map Selection
- The hardware icons have the second most display priority in the video sub-system. Only the hardware cursor will appear on top of the icon.

The hardware icon memory model and programming model are very similar in usage to that of the hardware cursor. The memory used to define the icon maps is at the top of the available display memory space and is fixed by the GD7542.

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A3.2 Hardware Icon Operation

The CL-GD7542 Video Datapath Control Register (SR12), and Hardware Icon Control Registers (SR2A / SR2B / SR2C / SR2D) can be programmed for the following:

- to enable/disable the icon
- to select the icon size
- to enable access to the Palette DAC icon colors
- to enable icon movement.

The hardware icon data is located in the bottom 8 Kbytes of the of the top 16 Kbytes of available display memory. The number of icon patterns that can be loaded in the display memory at one time is eight 64x 64bit- icons (of which four can be simultaneously displayed). These patterns can be defined as either two patterns per icon, or all eight patterns can be displayed on the first icon allowing all of the patterns to be displayed at the same location without having to update the icon hot spot.

A3.2.1 Icon Color

Each hardware icon pixel consists of two bits: The icon pixel bit 0 and the icon pixel bit 1. The following table shows how the two bits determine the displayed state of each icon pixel.

Table A3–1. Hardware Icon Pixel Bits

Icon Pixel Bit 0	Icon Pixel Bit 1	Displayed Data of Hardware Icon Pixel
0	0	Transparent / Icon Color 0
0	1	Icon Color 1
1	0	Icon Color 2
1	1	Icon Color 3

The icon colors 0 and 3 are supplied by the internal palette DAC's four extra Lookup Table (LUT) locations which are mapped into the existing LUT indexes 03h, 04h, 05h, and 06h, respectively As a result, the hardware cursor colors are independent of the existing LUT indexes 00h through FFh

- When enabled by setting SR12 [1] to 1, these four additional palette locations are accessible the same way as their standard VGA counterparts.
- Clearing SR12 [1] to 0 restores standard VGA operation to the palette.

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A3.2.2 Icon Position

The hardware icon position is controlled by programming the Graphics Icon Horizontal (X) position and Graphics Icon Vertical (Y) position. The hardware icon position is programmed the same way as the hardware cursor using the same I/O addresses. The GD7542 distinguishes the difference between the two operations by the state of register bit SR12 [3].

- When SR12 [3] = 0, writing X and Y position data will control the position of the hardware cursor.
- When SR12 [3] = 1, writing X and Y position data will control the position of the hot spot of the hardware icons.

The 11-bit icon X-location and Y-location values are programmed by initiating two 16-bit I/O writes to:

- SRX (3C4h) and SR10 (3C5h): Horizontal position
- SRX (3C4h) and SR11 (3C5h): Vertical position

where SRX[7:5] of the Index Register are the least-significant bits of the 11-bit value, and SRX[4:0] is the index into the horizontal and vertical position registers. Moving the icon always requires writing to both the horizontal and vertical position registers. The horizontal position is written first, but it does not take effect until the vertical position is updated.

NOTE: The horizontal fine-position control requires one more bit for those expanded-graphics modes that use 10-dot character clocks. For these special cases (for example, 640 x 480 graphics expanded for 800 x 600 panels), the most-significant bit for the fine-position adjustment is in SR2A[6], which is appended to the index bits SRX[7:5]. For standard non-expanded graphics modes, SR2A[6] is always 0, and can be ignored when moving the icon.

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The following figure shows the hot spot and vertical alignment of the icons as they appear on the display.

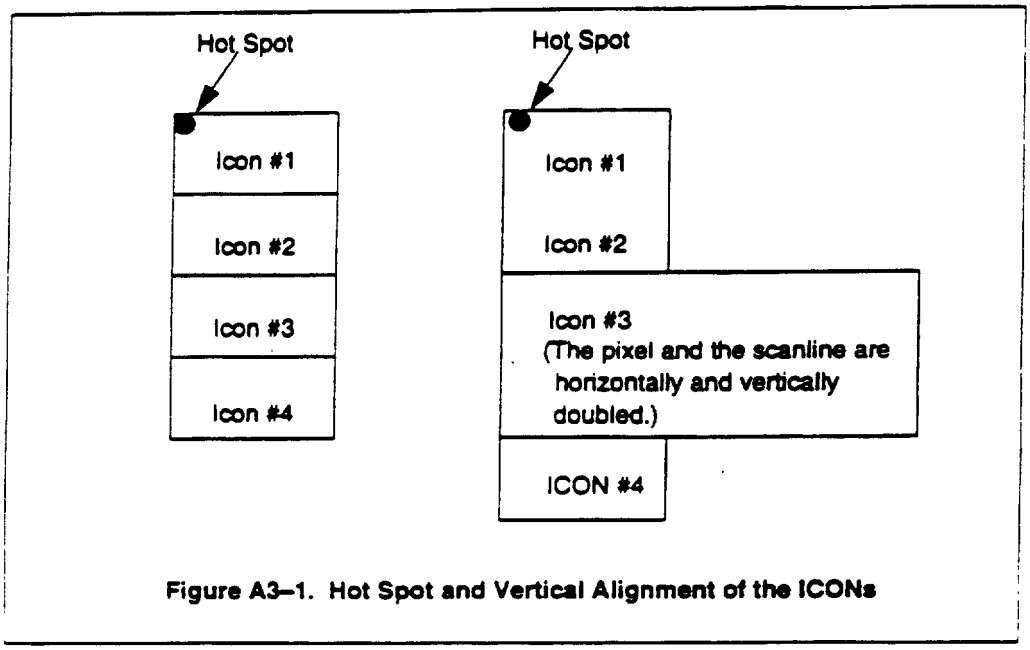


Figure A3–1. Hot Spot and Vertical Alignment of the ICONs

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The following table shows the CL-GD7542 Extension Registers bits needed for programming the hardware icon.

Table A3-2. Extension Registers Bits for Programming Hardware Icon

To:	Program:			
	Extension Register	I/O Port Address	Register Bits	Value
Enable hardware icon	SR2x[1]	3C5h	[0]	1
Display 3 colors + transparency	SR2x[1]	3C5h	[1]	1
Display 4 colors	SR2x[1]	3C5h	[1]	0
Enable blink	SR2x[1]	3C5h	[2]	1
Double horizontal pixel	SR2x[1]	3C5h	[3]	1
Double vertical scanline	SR2x[1]	3C5h	[4]	1
Select memory map	SR2x[1]	3C5h	[5]	0 or 1
Select icon #0 eight memory maps option	SR2E	3C5h	[2:1]	11, 10, 01, 00
Set hardware icon horizontal position[2]	SRX / SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]/[7:0]	2047...0
Set icon horizontal position fine-position extension (msb) for expanded graphics	SR2A	3C5h	[6]	0: Non-Exp. 1: Expanded
Set hardware icon vertical position[2]	SRX / SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:5]/[7:0]	2047...0

1 The x represents the four available icon programming registers; 2Ah, 2Bh, 2Ch, and 2Dh, which correspond to the GD7542's four hardware icons.
2 The icon position is programmed the same way as the hardware cursor using the same I/O addresses. The state of SR12[3] determines either the icon position or the cursor position are being updated.

A3.2.3 Memory Map Option

The eight CL-GD7542icon maps can be configured in two ways:

- Two maps per icon
- All eight maps available to icon #0

Register SR2E [2,1] controls this option.

- When this field is zero, the corresponding map pair that is displayed is icon #0.
- When this field is non-zero, only Icon #0 can be used, and it has accesses to all eight memory maps. The non-zero number points to the corresponding map pair that is displayed as Icon #0

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The member of the map pair that is actually displayed is selected by the state of SR2A [5]. For example, if SR2E [2:1] = 11 and SR2A[5]=0 then map #6 will be displayed as icon #0. For memory map details, refer to Table A3-3 .

When SR2E[2:1] field is non-zero, icons #1, #2, and #3 should be disabled.

A3.3 Hardware Icon Memory Map And Data Format

The following table shows the location of the hardware icon memory maps within the display memory.

Table A3–3. Hardware Icon Memory Map in 1-Mbyte Display Memory

Address	Hardware Icon Memory Map
3F700-3F7FF	Icon #3 Map #1 or Icon #0 Map #7
3F600-3F6FF	Icon #3 Map #0 or Icon #0 Map #6
3F500-3F5FF	Icon #2 Map #1 or Icon #0 Map #5
3F400-3F4FF	Icon #2 Map #0 or Icon #0 Map #4
3F300-3F3FF	Icon #1 Map #1 or Icon #0 Map #3
3F200-3F2FF	Icon #1 Map # 0 or Icon #0 Map #2
3F100-3F1FF	Icon #0 Map #1
3F000-3F0FF	Icon #0 Map #0

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The actual data that is stored in display memory to define the icon is written with two bits of data per pixel, as defined in Section A.3.2.1, "Icon Color". The following figure shows how the 64 pixels x 64 pixels icon is stored in 32-bit-wide display memory.

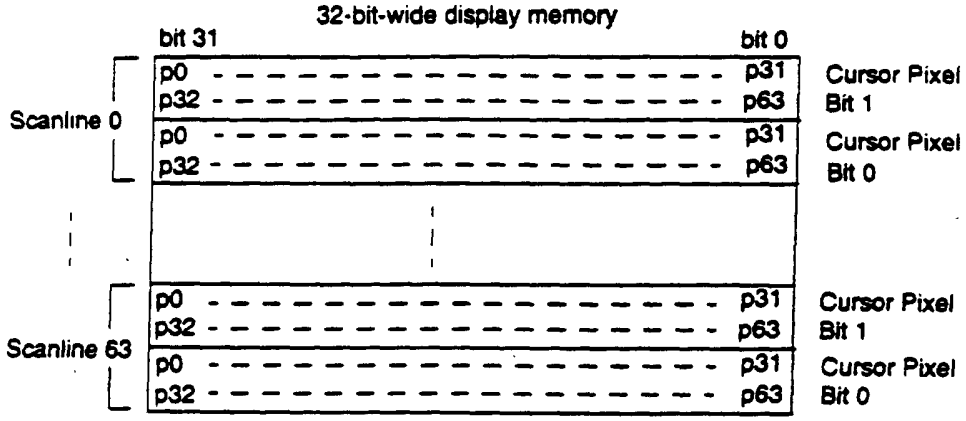


Figure A3-2. Icon (64 Pixels x 64 pixels) Stored in the Display Memory

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Appendix A4

Color Expansion and Extended Write Modes

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A4. Color Expansion And Extended-write Modes

A4.1. Introduction

The CL-GD7542 supports color expansion, using extended-write modes for faster CPU write performance. In graphics modes, these extended write modes can be used for the following operations: faster text write, pattern fill, and block move operations. In 8- or 16-bit-per-pixel graphics modes with packed-pixel addressing, these write modes operate on 8 pixels at a time.

A4.2. Color Expansion

Color expansion is the automatic conversion of a monochrome bit map, typically defining a character, icon, or pattern into foreground and background color values that are written into display memory. The foreground and background color values are held in the CL-GD7542, and only the monochrome bit maps need be transmitted across the bus. Each bit of the monochrome map is converted into an 8-bit or 16-bit pixel value: The bus traffic is reduced accordingly.

A4.3. Registers Involved In Color Expansion

The following register bits are involved in color expansion.

Table A4–1. Color Expansion Registers

Register Bit	Function
SR2[7.0]	Enable Writing Pixels
GRB[2]	1 enables Extended Write Modes
GRB[4]	1 enhances Extended Write Modes to 16-bit pixels
GR5[2:0]	100 chooses Extended Write Mode 4 101 chooses Extended Write Modes 5
GR0[7.0]	Extended Write Mode 5 Background Color Low Byte
GR1[7.0]	Extended Write Mode 4/5 Foreground Color Low Byte
GR10[7 0]	Extended Write Mode 5 Background Color High Byte
GR11[7 0]	Extended Write Mode 4/5 Foreground Color High Byte

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A4.4. Extended Write Modes

The CL-GD7542 supports two extended write modes: Extended Write Modes 4 and 5. These extended write modes can selectively update up to eight pixels of 8 or 16 bits each. For more information, refer to sections A4.8. and A4.9.

The extension register GRB, Graphics Controller Mode Extensions Register, bits [4:1] are used in combination to enable the CL-GD7542 Extended Write Modes.

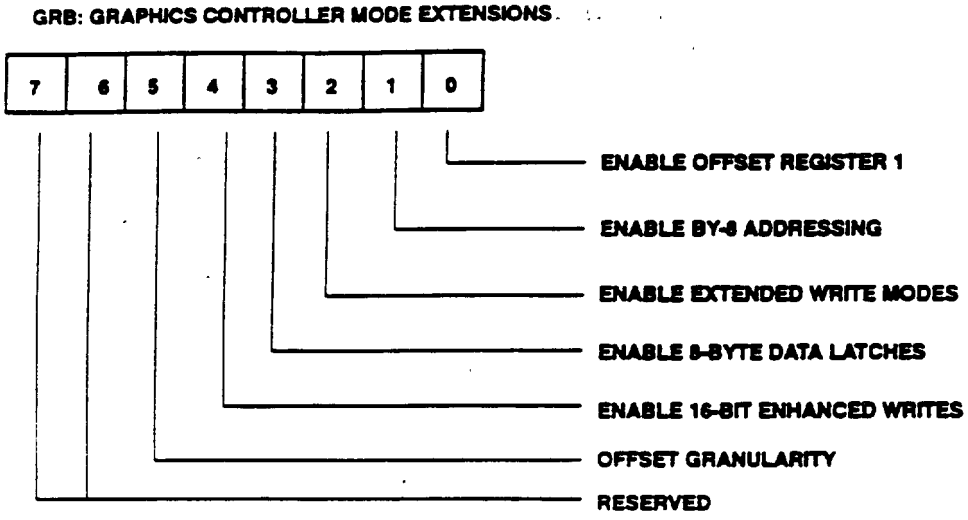


Figure A4–1. Extension Register GRB

When Extended Write Modes are enabled by setting GRB[2] to 1:

- Up to eight bytes can be transferred to display memory for every CPU byte transfer.
- GR5[2], the Mode Register bit, is enabled to select Extended Write Modes 4 and 5.
- GR0[7:0], the Set/Reset Register, extends read/write values for Extended Write Mode 5 Background Color
- GR1[7:0], the Enable Set/Reset Register, extends read/write values for Write Mode 4/5 Foreground Color
- SR2[3:0], the Map Mask Register bits, extends to SR2[7:0] for Write Modes 4 and 5.
- GRB[4], the Graphics Controller Mode Extensions Register bit, is enabled so that it can select enhanced writes for Write Modes 4 and 5.

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A4.5. By-8 Addressing

GRB[1], when set to 1, selects By-8 addressing for 8-bit-per-pixel (256-color) video modes. The system address is shifted left by three bits relative to packed-pixel addressing so that each system byte address points to a different 8 pixel (8 bytes) block in display memory.

This GRB[1] bit, in combination with GRB[2], is used for selecting extended write modes. This bit is a don't care when GRB[4] is 1.

A4.6. By-16 Addressing

GRB[4], in combination with GRB[2], is used to select Write Mode 4 and 5 for 16-bits-per-pixel graphics modes (RGB 555 or 565). The system address is shifted left by four bits relative to packed-pixel addressing so that each system byte address points to a different 8 pixels (16 bytes) block in display memoyr.

GRB[4] and GRB[2], when set to 1, select the following write mode operation:

- Enables By-16 addressing.
- Enables up to 16 bytes (eight pixels) to be transferred for each CPU byte cycle.
- Enables GR10 and GR11 as high-byte data for foreground and background color extensions. (GR0 and GR1 contain the low-byte data.)
- Enables each bit of SR2 to be used as pixel write mask for two bytes.

A4.7. Data Latches

When GRB[3] is set to 1, the memory read latches are eight bytes wide, instead of the normal four. Eight-byte wide memory read latches can be used in Write Mode 1 to write eight latched bytes back into display memory. This action allows either eight pixels in 256-color modes or four pixels in 16-bit/pixel modes to be updated in a single CPU byte cycle.

A4.8. Extended Write Mode 4

The CL-GD7542 supports Extended Write Mode 4, which is used in combination with BY-8 or BY-16 addressing modes to operate on eight pixels of data at a time (8 or 16 bytes, depending on 8-bit or 16-bit-per-pixel mode).

- In 8 bits per pixel mode, the Foreground Color Bits GR1[7:0] are used to update each pixel byte in display memory.
  - The 8-bit value is written as the foreground color when the corresponding CPU data is a 1, and the corresponding Map Mask Register bit in SR2 is also set to a 1.
  - When the CPU Data bit is a 0, the corresponding pixel in display memory is not changed by the write.
- In 16 bits per pixel mode, the Foreground Color Register bits GR11[7:0] (foreground-color high byte) and GR1[7:0] (foreground-color low byte) are used to update each pixel word in display memory
  - When the corresponding CPU data is 1 and the corresponding Map Mask Register bit in SR2 is also 1, the 16-bit value is written as the Foreground Color.
  - When the CPU data bit is 0, the corresponding pixel in display memory is not changed by the write.

This mode, for example, can be used to write text to display memory with the foreground color while preserving the background color. This action allows eight pixels of display data to be updated with a single CPU byte cycle.

A4.9. Extended Write Mode 5

The CL-GD7542 supports Write Mode 5, which is used in combination with x8 or x16 addressing mode to operate on eight pixels of data at a time (8 or 16 bytes based on 8-bit or 16-bit-per-pixel mode). This mode can be used to write text to display memory with a selected Foreground Color and a Background Color. This action allows eight pixels of display data to be updated with a single CPU byte cycle.

- In 8-bit/pixel mode, the Foreground Color bits GR1[7:0] or the Background Color Register bits GR0[7:0] are used to update each pixel byte in display memory.
  - When the corresponding CPU data is 1, the 8-bit value is written as the foreground color.
  - When the CPU data bit is 0, the corresponding pixel in display memory is written with the background color.
  - The corresponding Map-Mask Register, SR2[7:0], also inhibits writes to selected pixel in display memory.
- In 16-bit/pixel mode, the Foreground-Color bits GR11[7:0] (foreground-color high byte) and GR1[7:0] (foreground-color low byte), or the Background Color GR10[7:0] (background-color high byte) and GR0[7:0] (background-color low byte), are used to update each pixel word in display memory.
  - When the corresponding CPU data is 1, the 16-bit value is written with the foreground color.
  - When that CPU data bit is 0, the corresponding pixel in display memory is written with the background color.
  - The corresponding Map-Mask Register, SR2[7:0], also inhibits the corresponding pixel value (two bytes) to be written to display memory.

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Appendix A5

True-Color Modes

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A5. True-color Modes

A5.1 Introduction

The CL-GD7542 has a built-in true-color multi-mode palette DAC that supports the following modes:

- 8 bits per pixel (VGA-standard 256-color Palette Mode)
- 15 bits per pixel (32K color, the 5-5-5 Sierra Mode™)
- 16 bits per pixel (64K color, the 5-6-5 XGA™ Mode)
- 24 bits per pixel (16.8-million color, the 8-8-8 True-Color Mode)
- Mix Mode: Either 15 bits per pixel (5-5-5 Mode) or 8 bits per pixel(standard VGA Mode)

In the 256-color Palette Mode, the Palette DAC is VGA compatible and provides 256 simultaneous colors out of a palette of 256K on the display screen.

A5.2 Programming for a True-color Multi-mode Palette DAC

Extended Color Modes are enabled by the Hidden DAC Register (HDR at I/O Port 3C6h). At reset, this register is loaded with 00h, which programs the Palette DAC in a VGA-compatible mode. In this mode, the Palette DAC is functionally equivalent to the industry-standard Brooktree® BT476 RAMDAC™. By writing code to the Hidden DAC Register, the Palette DAC can be programmed in one of the modes mentioned above.

The following method is used to write to the Hidden DAC Register:

Step 1: Read from the Pixel-Mask Register (3C6h) four times in succession. No other reads/writes should be directed to that address.

Step 2: After the fourth read, the Pixel-Mask Register points to the Hidden DAC Register. At this time, the Hidden DAC Register can be programmed by writing to it at Port 3C6h. Any read from or write to any address, other than the Pixel-Mask Register, will reset an internal counter which 'hides' the Hidden DAC Register again. To continue, repeat Step 1.

Table A5–1. Extended Color Mode Selected with the Hidden DAC Register

HDR								Function
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0	X	X	X	X	X	X	X	Standard VGA Compatible 256-color Mode
1	1	1/0	0	0	0	0	0	5-5-5 Mode (32K colors,Sierra™)
1	1	1/0	1	0	0	0	0	5-5-5 and 256-color Mix Mode
1	1	X	0	0	0	0	1	5-6-5 Mode (64K colors, XGA™)
1	1	X	0	0	1	0	1	8-8-8 Mode (16.8-million colors, True Color Mode)

NOTE In 5-5-5 Mode (Sierra™).
- Programming HDR[5] to 0 chooses Clocking Mode 1.
- Programming HDR[5] to 1 chooses Clocking Mode 2.

When using a video overlay feature of the CL-GD7542, choose Clocking Mode 1.

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A5.2.1 5-5-5 Mode with 32K Colors

This mode supports the industry-standard 5-5-5 RGB mode with 32,768 colors. Each pixel is represented by 15 bits containing five bits of Red, Green, and Blue color information. The input sequence for each pixel is the low byte first, followed by the high byte.

The first low byte will be taken on the first rising edge of clock occuring after BLANK# has gone inactive (high).

- In Clocking Mode 2 (HDR[5] = 1), all subsequent bytes are clocked in on the rising edge of the clock.
- In Clocking Mode 1 (HDR[5] = 0), the low bytes are clocked in on the rising edige of the clock and the high bytes are clocked in on the falling edge of the clock .

This mode ignores the palette DAC's Lookup Table.

Table A5–2. Pixel Data Format in 5-5-5 Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
X	RED					GREEN					BLUE				

A5.2.2 5-6-5 Mode with 64K Colors (XGA™)

This mode supports the XGA™ 5-6-5 RGB Mode with 65,536 colors. Each pixel is represented by 16 bits containing five bits of Red, six bits of Green, and five bits of Blue color information. The input sequence for each pixel is the low byte first, followed by the high byte., by using the Clocking Mode 1 or 2. The first low byte will be taken on the first rising edge of clock occurring after BLANK# has gone inactive (high).

- In Clocking Mode 2 (HDR[5] = 1), all subsequent bytes are clocked in on the rising edge of clock.
- In Clocking Mode 1 (HDR[5] = 0), the low bytes are clocked in on the rising edge of the clock, and the high bytes are clocked in on the falling edge of the clock.

This mode ignores the palette DAC's Lookup Table..

Table A5–3. Pixel Data Format in 5-6-5 Mode with 64K Colors

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4	3	2	1	0	5	4	3	2	1	0	4	3	2	1	0
RED					GREEN						BLUE				

A5.2.3 8-8-8 Mode with 16.8 Million Colors (True Color Mode)

This mode supports the industry-standard 8-8-8 RGB Mode with 16,777,216 colors. Each pixel is represented by 24 bits containing one byte each of Red, Green, and Blue color information. The input sequence for each pixel is the low byte (Blue) first, followed by the middle byte (Green), followed by the high byte (Red).

This mode uses Clocking Mode 2 (HDR[5] = 1). The first low-byte is taken on the first rising edge of clock occurring, after BLANK# has gone inactive (high). All subsequent bytes are clocked in on the rising edge of clock. This mode ignores the palette DAC's Lookup Table. .

Table A5–4. Pixel Data Format in 8-8-8 Mode with 16.8 Million Colors

MSB HIGH BYTE								MIDDLE BYTE								LOW BYTE							LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

A5.2.4 Mix Mode

When HDR[4] is set to 1, the pixel data bit [15] will be used to select between 5-5-5 RGB Mode and the standard VGA compatible, 256-color mode.

Table A5–5. Pixel Data Format in 5-5-5 Mode of the Mix Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
5-5-5 Mode	RED					GREEN					BLUE				

Table A5–6. Pixel Data Format in 256-Color Mode of the Mix Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	7	6	5	4	3	2	1	0
256-Color Mode	Ignored							Palette DAC's Lookup-Table Input							

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Appendix A6

Memory Configurations

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A6. Memory Configurations

A6.1 Introduction

The CL-GD7542 supports scalable 32-bit-wide display-memory configurations, from 1 Mbyte to 2 Mbytes, using the following types of DRAMs.

- 512K x 8
- 256K x 16 – dual-CAS#
- 256K x 16 – dual-WE#

A6.2 Possible Memory Configurations

Table A6-1 shows the possible memory configurations that the CL-GD7542 supports.

For 256K x 16 DRAM configurations, the total display memory can be expanded from 1 M byte to 2 Mbytes. The 512K x 8 DRAM configuration must be 2 Mbytes. Some signals of the CL-GD7542 change functions according to the DRAM organization that is used.

For optimum performance, choose multiple-CAS# configurations over multiple WE# configurations.

Table A6–1. CL-GD7542 Memory Configurations

Total Display Memory Size	Memory Bus Width	DRAMs	
		Number	Type
1 Mbyte	32 bits	2	256K x 16
2 Mbytes[a]	32 bits	4	512K x 8
2 Mbytes[b]	32 bits	4	256K x 16

NOTES [a] The DRAM Control Register bit SRF[7] = 0
[b] The DRAM Control Register bit SRF[7] = 1

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A6.3 Control Signals for Various Memory Configurations

The following five tables indicate how the CL-GD7542 and the DRAMs must be connected.

Table A6–2. 2-Mbytes Display Memory: Four 512K x 8 DRAMs

DRAM Pins Connected to the CL-GD7542	The CL-GD7542 Pins Connected to the DRAMs			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
OE#	OE#	OE#	OE#	OE#
WE#	WE#	WE#	WE#	WE#
CAS#	CAS0#	CAS1#	CAS2#	CAS3#
RAS#	RAS0#	RAS0#	RAS0#	RAS0#
ADDR[9:0]	MA[9:0]	MA[9:0]	MA[9:0]	MA[9:0]
DATA	MD[7:0]	MD[15:8]	MD[23:16]	MD[31:24]
Bit Plane Stored in Each DRAM	3	2	1	0

NOTE: This configuration is Multiple-CAS#, Common-WE# (SRF[0] = 1).

Table A6–3. 1-Mbyte Display Memory: Two 256K x 16 DRAMs: — Dual-CAS# Type

DRAM Pins Connected to the CL-GD7542	The CL-GD7542 Pins Connected to the DRAMs	
	To DRAM #1	To DRAM #2
LCAS#	CAS2#	CAS0#
UCAS#	CAS3#	CAS1#
OE#	OE#	OE#
RAS#	RAS0#	RAS0#
WE#	WE#	WE#
ADDR[8:0]	MA[8:0]	MA[8:0]
ADDR[9]	not valid	not valid
DATA	MD[31:16]	MD[15:0]
Bit Planes Stored in Each DRAM	0,1	2,3

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Table A6–4. 1-Mbyte Display Memory:Two 256K x 16 DRAMs — Dual-WE# Type

DRAM Pins Connected to the CL-GD7542	The CL-GD7542Pins Connected to the DRAMs	
	To DRAM #1	To DRAM #2
LWE#	WE2#	WE0#
UWE#	WE3#	WE1#
OE#	OE#	OE#
RAS#	RAS0#	RAS0#
CAS#	CAS#	CAS#
ADDR[8:0]	MA[8:0]	MA[8:0]
ADDR[9]	not valid	not valid
DATA	MD[31:16]	MD[15:0]
Bit Plane Stored in Each DRAM	0,1	2,3

Table A6–5. 2-Mbytes Display Memory: Four 256K x 16 DRAMs — Dual-CAS# Type

DRAM Pins Connected to the CL-GD7542	The CL-GD7542 Pins Connected to the DRAMs			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
LCAS#	CAS2#	CAS0#	CAS2#	CAS0#
UCAS#	CAS3#	CAS1#	CAS3#	CAS1#
OE#	OE#	OE#	OE#	OE#
RAS#	RAS0#	RAS0#	RAS1#	RAS1#
WE#	WE#	WE#	WE#	WE#
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31 16]	MD[15:0]	MD[31:16]	MD[15:0]
Bit Planes Stored in Each DRAM	0,1	2,3	0,1	2,3

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Table A6–6. 2-Mbytes Display Memory: Four 256K x 16 DRAMs — Dual-WE# Type

DRAM Pins	The CL-GD7542Pins			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
LWE#	WE2#	WE0#	WE2#	WE0#
UWE#	WE3#	WE1#	WE3#	WE1#
OE#	OE#	OE#	OE#	OE#
RAS#	RAS0#	RAS0#	RAS1	RAS1
CAS#	CAS#	CAS#	CAS#	CAS#
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
Bit Planes Stored in Each DRAM	0,1	2,3	0,1	2,3

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Appendix A7

Clock Options

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A7. Clock Options

A7.1 Introduction

The dual-frequency synthesizer in the CL-GD7542 generates all the clocks needed for the memory timing (RAS#, CAS#, etc.), as well as the video clock timing. To derive these internal clock signals, an external reference clock must be provided to the OSC input of the CL-GD7542. For all calculations in this document, the external reference clock used is 14.31818 MHz ± 0.01% with a duty cycle of 50 ± 10%.

A7.2 Memory Clock

Memory Clock (MCLK) is used to generate all of the memory timing signals (RAS#, CAS#, etc.).

A7.2.1 Default Memory Clock (MCLK)

The CL-GD7542 default memory clock frequency is 44.744 MHz. For the equation in the next section, this frequency is equivalent to 19h (25 decimal). For information regarding the CL-GD7542's configuration, refer to Appendix A14.

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A7.2.2 MCLK Programming

The CL-GD7542 has a programmable memory clock for higher performance. The desired MCLK frequency is programmed directly into SR1F[5:0], by using the equation below. The MCLK selected at system reset(19h) is valid until SR1F is written.

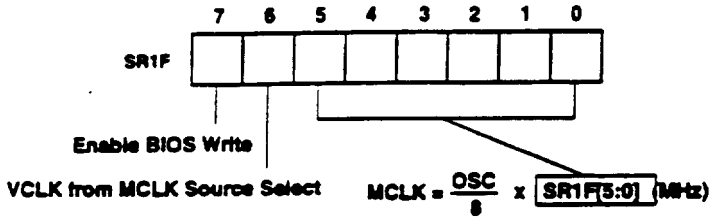


Figure A7.–1. Programmable Memory Clock

Examples of valid MCLK frequencies are shown in following table:

Table A7–1. Examples of Valid MCLK Frequencies

SR1F[5:0] (Decimal))	SR1F[5:0] (hex)	MCLK Frequency (MHz)
21	15h	37.585
23	17h	41.165
25	19h	44.744
28	1Ch	50.114

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A7.3 Video Clock

The video clock (VCLK) is the fundamental video timing clock in the system. The CRT monitor timing signals (HSYNC and VSYNC) as well as the LCD clocks are derived from VCLK.

A7.3.1 Default Video Clock Source

The VCLK source is determined by a number of factors, as indicated in Table A7-2. MCLK or MCLK/2 (one half the frequency of MCLK) as well as four VCLKs can be used as a default VCLK.:

Table A7–2. VCLK Sources and Frequencies

SR1F[6]	SR1E[0]	MISC Register 3C2[3:2]	Video Clock (Defaults)	
			Source	Frequency (MHz)
0	x	00	VCLK0	25.180
0	x	01	VCLK1	28.325
0	x	10	VCLK2	41.165
0	x	11	VCLK3	36.082
1	0	xx	MCLK	42.955
1	1	xx	MCLK/2	21.477

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A7.3.2 VCLK Programming

The four internal VCLK sources can be programmed with two registers each, as indicated in the following table.

Table A7–3. Internal VCLK Sources

Video Clock Source	Default Frequency (MHz)	Numerator			Denominator			Post-Scalar
		Register	Dec.	Hex	Register	Dec.	Hex	
VCLK0	25.180	SRB[6:0]	102	66h	SR1B[5:1]	29	3Bh	1
VCLK1	28.325	SRC[6:0]	91	5Bh	SR1C[5:1]	23	2Fh	1
VCLK2	41.165	SRD[6:0]	69	45h	SR1D[5:1]	24	30h	0
VCLK3	36.082	SRE[6:0]	126	7Eh	SR1E[5:1]	25	19h	1

For each VCLK, a 7-bit numerator (N), 5-bit denominator (D), and 1-bit post scalar (P) determines its frequency according to the equation shown in the following figure:

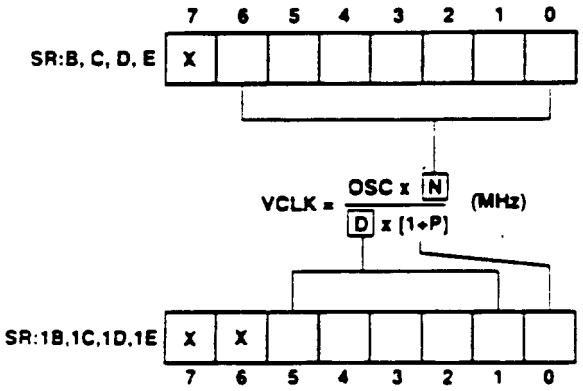


Figure A7–2. Programmable Video Clock

Typically a large number of numerator/denominator values will program a common frequency. The choice among these combinations is made empirically. Generally, better results will be obtained if the post-scalar is programmed to 1.

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A7.4 Using MCLK as VCLK

When MCLK and VCLK are programmed to frequencies very close to each other (within about 1%), or to frequencies that are nearly multiples of each other, they may interfere with each other. This interference can show up as 'jitter' on the screen. The solution is to shut down the VCLK Oscillator and use MCLK (or MCLK/2) as VCLK. The following table shows examples of frequencies for which this solution should be used. .

Table A7–4. Memory Clock Used as Video Clock

MCLK	Video Mode	VCLK		Selection Criteria		
		Frequency	Source	SR1F[5:0]	SR1F[6]	SR1E[0]
50.1	64, 66 at 60 Hz	25 MHz	MCLK/2	1Ch	'1'	'1'
50.1	58, 5C at 72 Hz	50 MHz	MCLK	1Ch	'1'	'0'

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Appendix A8

Dynamic Video Overlay

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A8. Dynamic Video Overlay

A8.1 Introduction

The CL-GD7542 supports the dynamic video overlay modes, in which the video data from the feature connector pixel data bus (Pixel Bus) is overlaid on a pixel-by-pixel basis. The dynamic video overlay modes are intended to be used when the CL-GD7542 is in Video Mode 5F (640 x 480 x 256 colors). Other 256-color modes may be used as limited by dot clock.

A8.2 Dynamic Video Overlay Features

The CL-GD7542's dynamic video overlay has the following functions:

- VESA pass-through when the FCEVIDEO# pin is driven low
- On-chip Window timing generator
- Dynamic video overlay with Color Key and OVWR#

The CL-GD7542 supports the standard VESA pass-through function, during which the FCEVIDEO# pin is statically driven low and the video is driven into the Pixel Bus. The entire frame is overlaid, and the contents of display memory are ignored. While this function is on, the CL-GD7542 supports only 8-bit-per-pixel data.

In the dynamic video overlay configurations, the video from display memory can be overlaid on a pixel-by-pixel basis. This feature makes it possible to overlay a portion of the frame and mix the VGA video with externally generated video. The term 'dynamic' applies because both the video source and the choice of pixels to be overlaid can be changed dynamically.

In large part, the dynamic video overlay is made possible by driving the Pixel Bus input pins to the valid CMOS levels, and taking video from them to the DAC only when desired. This action eliminates the bus exchange time. The CL-GD7542 supports the dynamic video overlay, but it has some restrictions regarding the Color Key feature.

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A8.3 Overview Of Dynamic Video Overlay

The Dynamic Video Overlay Modes are intended to be used when the CL-GD7542 is in video mode 5F (640 x 480 x 256 colors). Other 256-color Modes may be used as limited by dot clock. The Dynamic Overlay Modes are chosen by programming the CR1A[3:2] field according to the following table:

Table A8-1. Dynamic Video Overlay Modes

CR1A		Mode
[3]	[2]	
0	0	VGA-compatible Operation
0	1	Dynamic Video Overlay with FCEVIDEO#
1	0	Dynamic Video with OVWR# and Color Key
1	1	Dynamic Video Overlay with Color Key

The video data that is introduced into the Pixel Bus is assumed to be 5-5-5 Sierra™ or 5-6-5 XGA™ format according to the value of the Hidden DAC Register. These formats are the only ones allowed. Refer toTable A8-2. Clocking Mode 1 must be used.

NOTES: Clocking Mode 1 can be chosen by setting HDR[5] to a 0. In Clocking Mode 1, 16-bit/pixel modes will use both edges of FCDCLK to latch data: The rising edge will latch the least significant byte. The falling edge will latch the most significant byte.

Table A8-2. External Video Format

External Video Format	Hidden DAC Register Value
5-5-5	100XXXX 110X0000
5-6-5	110X0001

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A8.4 Dynamic Video Overlay With FCEVIDEO#

When the CR1A[3:2] field is programmed to 01, the Dynamic Video Overlay with FCEVIDEO# is chosen. The Pixel Bus is switched to inputs: An external video generator must always drive the bus to guarantee valid CMOS levels, even when the inputs are being ignored. Each pixel for which FCEVIDEO# is low will be taken from the Pixel Bus. There is no requirement that the pixels to be overlaid be contiguous (adjacent), either horizontally or vertically.

The following timing diagram shows the FCEVIDEO# setup and hold times that must be met with respect to FCDCLK. FCEVIDEO# has a setup and hold time requirement to guarantee both that the desired pixel will be overlaid and the adjacent pixels will not be overlaid. In addition, there is a data setup and hold requirement for both edges of FCDCLK (the DAC is in Clocking Mode 1). The rising edge of FCDCLK will clock the least-significant byte of the pixel. The falling edge of FCDCLK will clock the most-significant byte.

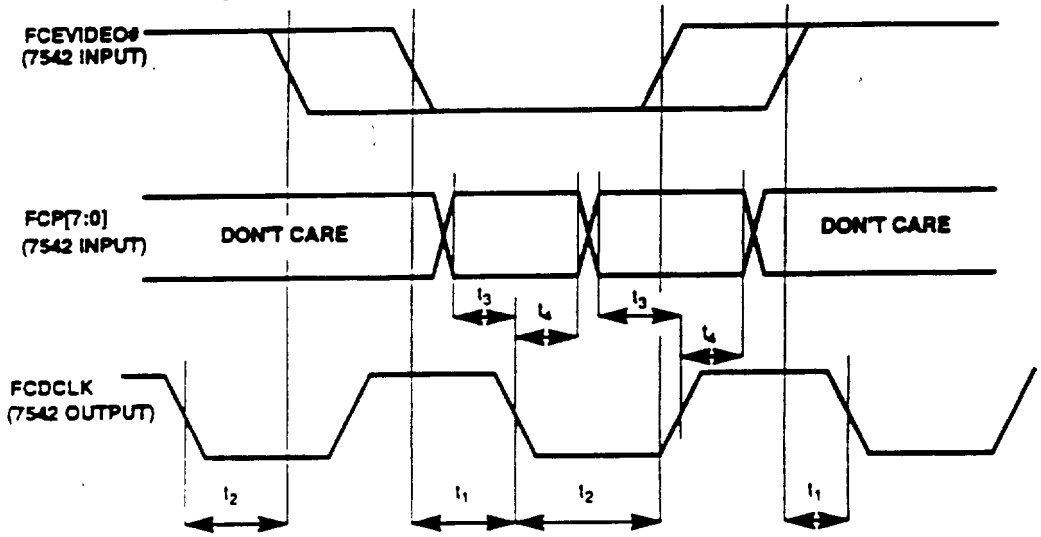


Figure A8–1. FCEVIDEO# Setup and Hold Times

NOTES
t_1 Command Setup to Clock
t_2 Command Hold from Clock
t_3 Data Setup to Clock
t_4 Data Hold from Clock

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The following pseudo-code fragment shows the registers that must be programmed:

```
Call WriteDACMode(0xC1)     'Choose 5-6-5 Mode Video (for example)
Call SetReg(CR1A,0x04)      'Overlay with FCEVIDEO#
```

Once these two registers have been programmed, each pixel either will or will not be overlaid according to the state of FCEVIDEO#

A8.5 On-chip Window Timing Generator

The CL-GD7542 contains logic to generate a single rectangular window. If this mode is enabled, the window timing comes out on OVWR#, which may be fed back into FCEVIDEO#: The chip specifies its own window.

This mode is chosen by programming CR1B[5] to a 1. When this bit is set, the blanking term to the palette DAC comes from the internal display enable signal, and there is no border. In turn, this action frees the Blank Generator Logic, which is used as a window generator.

The following timing diagram shows how the Blanking Start and Blanking End Registers are used to specify either the horizontal or vertical component of the window. The Horizontal Blanking End field is extended to eight bits and the Vertical Blanking End is extended to 10 bits.

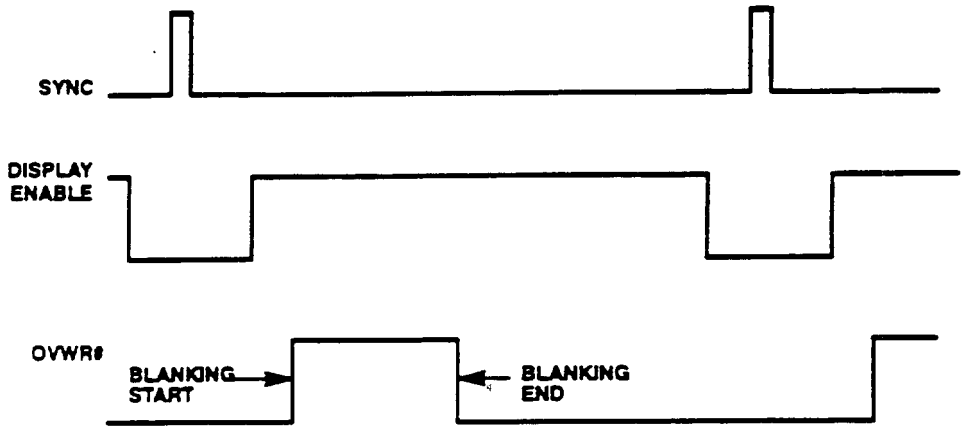


Figure A8–2. Usage of Blanking Start and Blanking End Registers

When the vertical timing and the horizontal timing thus generated coincide, OVWR# will be driven low indicating the window. OVWR# may be connected directly to FCEVIDEO# if CR1A[3,2] = 11 (dynamic video overlay mode with color key only) is never going to be chosen. If CR1A[3,2] = 10 (dynamic video overlay mode with color key and OVWR#), OVWR# must be driven into FCEVIDEO# with an external three-state buffer to avoid a potential bus collision.

This method of generating timing has four restrictions that require consideration.

- There can be no border, because the blank timing generation logic is used for window generation. This restriction is inconsequential since the VESA timing specifications do not include a border
- The resolution of the horizontal component of the window is 8 pixels, since the Horizontal Counters operate on an 8-pixel character clock. This restriction can be overcome at least in part by using FCEVIDEO# and color key overlay, as discussed later.
- There can be only a single window and it must be rectangular.

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- The first or third scanline or group of pixels can be chosen as a window boundary, but not the second scanline.

For dynamic programming of the blank registers, eight registers must be programmed to set up all four blank parameters, five of which contain bits related to other functions. The following table shows the registers that are involved:

Table A8–4. Dynamic Programming of Blank Registers

Register	Bits	Parameter
CR2	[7:0]	Horizontal Blanking Start [7:0]
CR3	[4:0]	Horizontal Blanking End [4:0]
CR5	[7]	Horizontal Blanking End [5]
CR7	[3]	Vertical Blanking Start [8]
CR9	[5]	Vertical Blanking Start [9]
CR15	[7:0]	Vertical Blanking Start [7:0]
CR16	[7:0]	Vertical Blanking End [7:0]
CR1A	[7:6]	Vertical Blanking End [9:8]
CR1A	[5:4]	Horizontal Blanking End [7:6]

All the following general scheme is used to dynamically move and resize the window.

- Obtain copies of the registers containing bits used for other functions (CR3, CR5, CR7, CR9, CR1A), and force the blank control bits to zeroes. These values are saved and used as templates in the first of two activities. This activity accepts the window co-ordinates and returns the value for each register. This routine must isolate and align each field as indicated in the table above, and then merge it with the template that was previously saved.
- Accept the values for all eight registers and load them into the hardware. This activity should be synchronized with vertical retrace.

A8.6 Dynamic Video Overlay With Color Key

Dynamic video overlay with color key is chosen when the CR1A[3:2] field is programmed to 11. In this mode, the window timing is controlled strictly by the contents of display memory. If a pixel matches the contents of the Color Key Register, it will be replaced with the video from the Pixel Bus. FCEVIDEO# is a normally a low output in this mode, that goes high for one FCVCLK period before a pixel is replaced. If multiple contiguous pixels are to be replaced, FCEVIDEO# will remain high appropriately.

GRC, the Color Key Compare Register, contains the color key which is compared with the pixel from display memory.

The following pseudo-code fragment shows the registers that must be programmed to configure the CL-GD7542 for Dynamic Video Overlay with Color Key:

```
Call WriteDACMode(0xC1)    'Choose 5-6-5 Mode Video(for example)
Call SetReg(CR1A,0x0C)     'Overlay with FCEVIDEO#
Call SetReg(GRC,ColorKey)  'Set up the Key
Call SetReg(GRD,KeyMask)   'and the mask
```

Once the CL-GD7542 has been programmed into this mode, the Pixel Bus bits are the inputs and must be driven by an external video generator to guarantee valid CMOS levels, even during those periods for which the Input Video will not be used. The Pixel Bus does not have internal pull-ups.

FCEVIDEO# may be used by an external video generator to determine when the first pixel of the window is about to occur. This would be useful if the external video is to be positioned with respect to a rectangular window, rather with respect to the frame. The following diagram shows the timing of FCEVIDEO# and the required timing for the video.

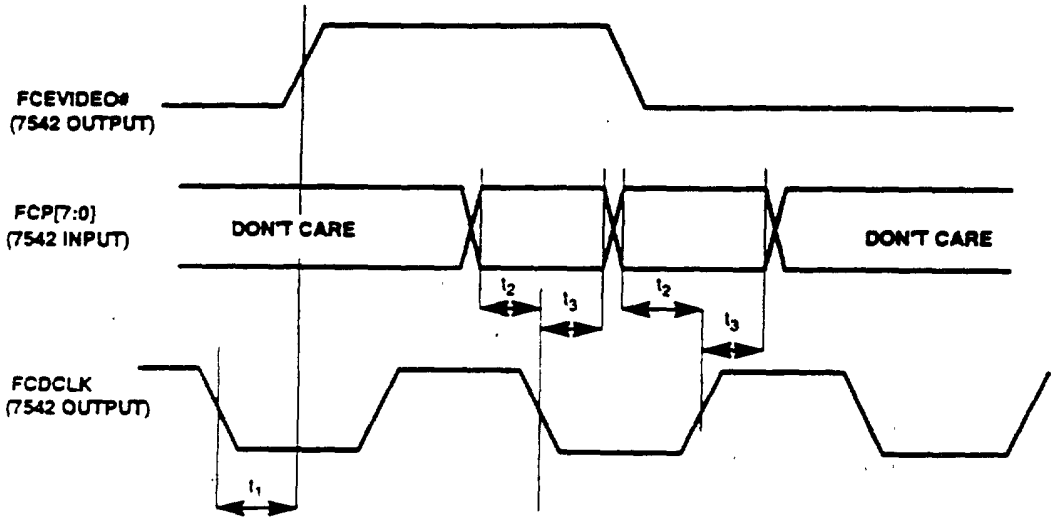


Figure A8–3. External Video Timing

NOTES:

t_1 FCDCLK to FCEVIDEO# Propagation Delay

t_2 Data Setup to FCDCLK

t_3 Data Hold from FCDCLK

A8.7 Dynamic Video Overlay with Color Key And OVWR#

Dynamic Video Overlay with Color Key and OVWR# is chosen when the CR1A[3:2] field is programmed to 10. The window time is the result of the logical AND of the Color Key Comparison and OVWR# being active. In this mode, FCEVIDEO# is an input and will be active for pixels that will be overlaid. This mode is intended to restrict the Color Key effect to a specified area.

```
User name:    SHAW (11)                    Queue:  UIDESK/UNIX_UIMKGT
File name:                                 Server: CLFPCD010
Directory:
Description: nordic_2.txt
             December 21, 1998                          6:35pm
```

EXHIBIT
RX-573 C

```
 SSS  H   H   A   W   W
S   S H   H  A A  W   W
S     H   H A   A W   W
 SSS  HHHHH A   A W W W
    S H   H AAAAA W W W
S   S H   H A   A WW WW
 SSS  H   H A   A W   W


L      SSS  TTTTT
L     S   S   T
L     S       T     : :
L      SSS    T     : :
L         S   T
L     S   S   T     : :
LLLLL  SSS    T     : :
```

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Nordic – Register Definitions

General Information, Definitioins and Notes that apply to this document

General:

1. SRxy with odd x, and 0 or 1 y are not allowed as they overlap with h/w cursor and icon registers.

Definitions:

1. In this document "h/w cursor" = "graphics cursor"

Notes:

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Prepared by: _____

Approved by: _____

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1.0 Nordic Special Registers

1.1 SR7 - Extended Sequencer Mode

Bit	Definition
[7:0]	Like in AVGA3 (not like in T1)

1.2 SRF - DRAM Control

Bit	Definition
[6]	Disable Video Memory fast-page mode for CPU cycles
[5]	CRT FIFO 16x32 Depth Selection (default: 8x32)
[7,4,3]	Video Memory Width and structure: 000 = 32bit, 4 x 512K x 8 001 = 16bit, 1 x 256k x 16 010 = 32bit, 2 x 256K x 16 (default) 011 = reserved for 64bit 100 = 32bit, 4 x 256k x 16, two banks 101:111 reserved
[2]	Short RAS Timing 3.5/2.5 (default: Long RAS Timing 4/3)
[1]	Assymetric DRAM support (default: symetric DRAM support) %
[0]	Two CAS 16bit 256Kx16 Memory Chip (default: two WE) %

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1.3 SR16

Bit	Definition
[7]	Disable driving CPU Data Bus during first T2 in VL bus or local bus. To be used with 20MHz 486DX or DX2 bus with zero wait states. Default (reset state) = 1 This bit allows to optimize chip response for slow buses, reducing the number of wait states.
[6]	RDY DLY for I/O in all buses. Default (reset state) = 1
[5:0]	As in 5428 Reference Manual.

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0.1 SR18 Signature Generator Control Register

This register is used to control and read-back the status of Nordic signature generators. *There are two signature generators in Nordic: one for the* data path, that can be applied to either VGA data path or to the MVA data path, and one on the dither, NTSC and shader - the panel data path.

Bit	Definition
[7]	**Enable Panel Signature Generator (default = 0)**
[6]	**Reserved - see 5428 Tech Ref. It should do the same thing**
[5]	Enable Data Generator for the "Video Data Path" signature generator. **Once Data Generator is Enabled, this bit becomes Signature generator read-back bit until the enable is reset by SR18[1].** **CR3D[7] selects the data path for the signature generator: VGA or MVA.**
[4:2]	Pixel Bus Select [2:0]
[1]	Reset Signature Generators: this bit resets all the signature generators in Nordic
[0]	Signal Generator Enable/Status

Only bits 7 and 6 are new in Nordic, but bit 1 has extended functionality.

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0.1 SR21 (SR1A in 62XX moved to SR21 in Nordic)

Bit	Definition
[7]	One Refresh per Scanline Select bit
[6]	Dual Scan Color STN select bit, requires CR1C panel type bits to point to STN panels[6] Dual Scan Color STN select bit, requires CR1C panel type bits to point to STN panels
[5]	Reduce CPU Latency by adjusting Half Frame Buffer FIFO Threshold with Monochrome Dual STN panels[5] Reduce CPU Latency by adjusting Half Frame Buffer FIFO Threshold with Monochrome Dual STN panels
[4]	reserved ??
[3]	reserved ??
[2]	Enable test bus to come out to LD,UD, R5 and R4.
[1:0]	Select one of the four available test bus branches to be outputed by the chip. This bits are to be used by manufacturing test.

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1.4 SR22 - h/w Configuration (read only)

Bit	Definition
[7]	32bits PCI bus no Burst h/w PU configuration on MD24. It is called "PCINBPU" (read only bit). This is a reserved configuration in case burst does not work on a PCI bus (this bit was SR2A[0]). On MD23 - PCINBPU.
[6]	8bit BIOS (default 16bit BIOS) On MD22 - BIOS8PU. In ISA bus configuration the BIOS is always supported.
[5]	46e8[3] sleep (default 3c3 sleep) Nordic-1M comes up awake. We need to clear this with the BIOS and driver group. On MD21 - S46PU.
[4]	Reserved
[3]	select external clocks: MCLK and VCLK on SW0/MCLK/XMCLK and OSC/XVCLK. (default: internal clock synthesizer, SW1 and OSC) 0 = internal clocks with the pins used as inputs for panel type switch #1 and OSC. If SR23[4] and SR23[0] are 1, VCLK and SW0/MCLK/XMCLK, respectively become VCLK and MCLK outputs respectively, for testpurposes (only if SR22[3]=0 MCLK can be seen, but VCLK can be seen even if SR22[3]=1 as long as SR23[4]=1) 1= SW0/MCLK/XMCLK and OSC/XVCLK become XMCLK and XVCLK inputs generating directly chip MCLK and VCLK without clock synthesizer. The clock synthesizers are powered down if SR22[3]=1. This is CF[4] in AVGA3. On MD19 - XCLKPU.
[2]	VESA VL bus 50MHz On MD18 - FVLPU.
[1]	Select ISA bus support (default: 33MHz or less VESA VL) On MD17 - ISAPU **If this bit is 1**, Nordic is in ISA bus configuration and EBROMn/SLEEPIn pin is EBROMn output to the BIOS ROM and the BIOS decode at C000:0 is operational. **If this bit is 0**, EBROMn/SLEEPIn pin is SLEEPIn input and can be used to put the chip to sleep (not present on the CPU bus - the same effect as 3C3 or 46E8 but from a pin).
[0]	Select PCI bus support (default: 33MHz or less VESA VL) On MD16 - PCIPU.

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1.5 SR23 - s/w configuration #1

Bit	Definition
[7]	Enable FCVCLK to drive the internal RAMDAC
[6]	SBY/ACTI select bit Default: SBY on SBY/ACTI pin.
[5]	Suspend/BLI select bit Default: 0 = Suspend pin 1 = Back-Light Input pin
[4]	Enable Output Internal VCLK on VCLK/FCDCLK Default: 0 = Output Constant Level L If SR23[4] = 1, VCLK is outputed on VCLK/FCDCLK pin independent on SR22[3] (external/internal clock selection). VCLK can be output also on the Feature Conector.DCLK, if the Feature Connector is enabled . Only there is an option to output VCLK/2 on FCDCLK.
[3]	Enable Pixel Semi. 2070 I/O Decode on LDEVn Default: 0 = I/O address 27C0:27C9 are not decoded by Nordic on LDEVn 1 = I/O address 27C0:27C9 are decoded by Nordic on LDEVn (this bit was on 32KHz/OVRW selection which is no longer needed)
[2]	48KB BIOS (default: 32KB of BIOS, when BIOS enabled)
[1]	ZERO Wait state for BIOS in ISA (default: one wait state?)
[0]	Output MCLK on SW0/MCLK/XMCLK pin if SR22[3]=0. Default: 0= SW0/MCLK/XMCLK is an input, namely SW0 = input, if SR22[3] = 0 XMCLK= input, if SR22[3] = 1

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1.6 SR24 - Panel Type Switches

Bit	Definition
[7]	VAFCPU (VESA Advanced Feature Connector External Pull-up) Read-back. Read only bit. If external pull-up (the bit read-back = 1), then all VAFC pins are configured for Video Port. Otherwise, they have other functions, or are disabled if no other function. (Disabled = the inputs are foced to the TTL and CMOST threshold, controls are off & the outputs are high-Z. It actually reads back what is latched on Reset on VAFCPU. On MD25 - VAFCPU.
[6]	Compressed Live Video Enable bit (SashaPack enable) (default: disable)
[5]	Reseved ~~(for Audio IN enable bit)(from CS4215 to Nordic). (default: disable).~~
[4]	Reserved ~~(for Audio Out enable bit) (from Nordic to CS4215). (default: disable).~~
[3]	All external Pull-Ups s/w controlled read (on a 1->0 transition) This bit is needed for restore operation if total graphics controller power off is used. Also, if the reset is too short to read the switches which have large resitence PU/PD, this bit can help. SW2:0 are directly read on the I/O bus (no latchat reset). So they do not need s/w read for save/restore.
[2:0]	SW2:0 pins read back (read only bits)

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1.7 SR25 - Timers S/W Reset, H/W Config. #2 & Packed Modes Register

Bit	Definition
[7]	This bit replaces CF2 (MD18) of 5428. If this bit is set, the internal DAC will respond to 8514 DAC Address 2EA-2ED in addition to the standard VGA DAC addresses.This bit is reset to zero (default: 0= Standard VGA DAC address).
[6]	This bit replaces CF0 (MD16) of 5428. It allows to work with an external RAM-DAC. It uses EBROM output as External RAMDAC Address Select for I/O while it still decides C000 for memory reads when in ISA. This is a feature of 5428 which we chose not to take out for the time being.This bit is reset to zero. Default = 0; Standard VGA DAC address.
[5]	Enable 1bit/pixel packed mode
[4]	Reserved for "Enable 2bit/pixel packed mode"
[3]	Enable 4bit/pel packed mode
[2]	Faster PCI bus for memory write (1mclk less to wait)
[1]	Reset Standby Timer (moved from T1 SR8[5])
[0]	Reset Backlight Timer (moved from T1 SR8[4])$$$

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1.8 SR26 - Least-Significant Byte of Shader Signature

Bit	Definition
[7:0]	

1.9 SR27 - Most-Significant Byte of Shader Signature

Bit	Definition
[7:0]	

1.10 SR28:SR29 - New Easy to Access BIOS Scratch Registers #5 & #6

Bit	Definition
[7:0]	**Notes on Scratch Registers:** 1. There are 13 18bit scratch registers available in the RAMDAC RAM. They can be accessed by programmimg SR12[1]=1. They are accessed as any RAMDAC RAM register (in groups of 3 I/O accesses). 2. Please note that SR9 and SRA are AVGA3 and T1 Scratch Registers #1 and #2. Also SR14 and SR15 are AVGA3 Scratch Registers #3 and #4 (not in T1).

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2:0 H/W Icon Registers

H/W Icon Horizontal and Vertical position are programmed exactly like the h/w cursor position
SR12[3]=1 will make this mechanism address h/w icon.
SR12[3]=0 will make this mechanism address h/w cursor.

Note: In this document "h/w cursor" = "graphics cursor"

2.1 SR10,30,50,70,90,B0,D0,F0 - H/W Icon & Cursor Horizontal Position

Bit	Definition
[7:0]	

2.2 SR11,31,51,71,91,B1,D1,F1 - H/W Icon & Cursor Vertical Start Position

Bit	Definition
[7:0]	

2.3 SR12 - Graphics Cursor Attributes Register *(Nordic added bit 3)*

Bit	Definition
[7]	Overscan Color Protect
[6]	Tristate all Video Memory Pins (address, data, RAS,CAS,WE,OE) 0 = no tri-state 1 = tri-state Can be used to share Video Memory with a second graphics controller. The memory contents may be lost when switching.
[5:4]	Reserved
[3]	This bit selects CPU access for Icon-position modification versus h/w-cursor position (both horizontal and vertical). As for h/w cursor, for h/w icon the horizontal position effect is gated by the vertical position update [7:0] Coarse Horizontal Position (in character clocks). Select CPU Access to h/w icon position update both horizontal and vertical). Default = 0 = h/w cursor CPU access. This bit does not affect SR2A[6] and SR2E[0] which are always accessible by the CPU.
[2]	Cursor Size Select (32 x 32 or 64 x 64)

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[1]	Allow CPU Access to DAC Extended Colors
[0]	Graphics Cursor Enable

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2.4 SRX - Sequencer Register Index

Bit	Definition
[7:5]	These bits select the low-order bits of vetical position; i.e., the **fine position** (in VCLK). Since h/w **cursor** works only in graphics, three bits are enough in most cases for an 8-dot character clock. However, h/w **icon** needs more fine bits, since it works in text which can be an 8, 9 or 10-dot character clock. **SR2A[6]** is the **msb** for fine position for h/w **icon**, to be used with 9 and 10-dot fonts. Actually, h/w cursor needs to be positioned within ten dots when horizontal expansion from 640-to-800 is on. **SR2E[0]** is the **msb** for fine position for h/w **cursor.** To speed up writing this register bit, no other bit of SR2E will be used.
[7:0]	Corase Vertical Position (in scan lines).

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2.5 SR2A - H/W Icon #0 Control Register

Bit	Definition
[7]	**Icon Test Bit.** When this bit = '1', it enables Icon test mode.Relevant icon control signals are placed on the test bus. Default = 0.
[6]	**Icon Horizontal Fine-Position Most-Significant Bit[3].** To be used with 9 and 10-dot character clocks, when in text or in horizontally expanded graphics. Since h/w icon position is seldom updated, no effort was made to minimize s/w needed to write this icon position bit.
[5]	**Memory Map Selection for Icon #0** '0' = map zero, '1' = map one)
[4]	**Enable Vertical-Scan-Line Doubling for Icon #0.** When enabled, the icon extends down and pushes all the other icons down. When this bit = '1', the icon #0 displays 128 scan lines, but each scan line is replicated.
[3]	**Enable Horizontal Pixel Doubling for Icon #0.** When this bit = '1', the icon #0 displays 128 pixels, but each pixel is replicated horizontally. The icon extends towards right as we look at it.
[2]	**Enable Blink for Icon #0** '1' = blink at half text-cursor blink rate.
[1]	**Display mode selection for Icon #0:** 3colors + transpency or 4 colors '0' = four colors, '1' = three colors + transparent, '00' = transparent The h/w icon is always two bits per pixel. This bit controls how these two bits are used.
[0]	Icon #0 Display Enable: Default = '0'

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2.6 SR2B - H/W Icon #1 Control Register

Bit	Definition
[7:6]	Reserved
[5]	**Memory Map Selection for Icon #1** '0'= map zero, '1' = map one)
[4]	**Enable Vertical-Scan-Line Doubling for Icon #1.** When enabled, the icon extends down and pushes all the other icon down. When this bit = '1', the icon displays 128 scan lines for icon #1, but each scan line is replicated.
[3]	**Enable Horizontal-Pixel Doubling for Icon #1.** When this bit = '1', the icon displays 128 scan lines for icon #1, but each pixel is replicated horizontally. The icon extends towards right as we look at it.
[2]	**Enable Blink for Icon #1**
[1]	**Display Mode Selection for Icon #1:** 3colors + transpency or 4 colors '0' = four colors, '1' = three colors + transparent, '00' = transparent The h/w icon is always two bits per pixel. This bit controls how these two bits are used.
[0]	**Icon #1 Display Enable**: Default = '0'

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2.7 SR2C - H/W Icon #2 & PCI Byte Swap Control Register

Bit	Definition
[7]	Enable PCI bus base register 14H, bits 31:24 as defining a valid address range for Nordic. Valid only with PCI bus. 0= 14H base address contents is not decoded as a valid address range 1= 14H base address is decoded as a valid address range
[6]	Enable byte swap in the address space specified by PCI base address 14H bits 31:24. Byte zero becomes byte 1 and byte 2 becomes byte 3 and vice-versa (byte 1 becomes byte 0 and byte 3 becomes byte 2). Valid only with PCI bus.
[5]	**Memory Map Selection for Icon #2** '0' = map zero, '1' = map one)
[4]	**Enable Vertical Scan Line Doubling for Icon #2.** When enabled, the icon extends down and pushes all the other icons down. When this bit = '1', the icon displays 128 scan lines for icon #2, but each scan line is replicated.
[3]	**Enable Horizontal Pixel Doubling for Icon #2.** When this bit = '1', the icon displays 128 pixels for icon #2, but each pixel is replicated horizontally. The icon extends towards right as we look at it.
[2]	**Enable Blink for Icon #2**
[1]	**Display Mode Selection for Icon #2:** 3colors + transpency, or 4 colors '0' = four colors, '1' = three colors + transparent, '00' = transparent. The h/w icon is always two bits per pixel. This bit controls how these two bits are used.
[0]	**Icon #2 Display Enable:** Default = '0'

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2.8 SR2D - H/W Icon #3 Control Register

Bit	Definition
[7:6]	Reserved
[5]	**Memory Map Selection for Icon #3** '0' = map zero, '1' = map one)
[4]	**Enable Vertical Scan Line Doubling for Icon #3.** When enabled, the icon extends down and pushes all theother icons down. When this bit = '1', the icon displays 128 scan lines for icon #3, but each scan line is replicated.
[3]	**Enable Horizontal Pixel Doubling for Icon #3.** When this bit = '1', the icon displays 128 pixels for icon #3, but each pixel is replicated horizontally. The icon extends towards right as we look at it.
[2]	**Enable Blink for Icon #3**
[1]	**Display mode selection for Icon #3:** 3colors + transpency or 4 colors (0 = four colors, 1 = three colors + transparent, 00 = transparent) The h/w icon is always two bits per pixel. This bit controls how these two bits are used.
[0]	**Icon #3 Display Enable:** Default = '0'

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2.9 SR2E - Graphic-Cursor Horizontal-Position Extension Register

Bit	Definition
[7:1]	Not Used: These bits should not be used for anything but additional fine position bits for graphic cursor. This way, no masking has to be done in order to write bit [0] of this register. Since the cursor is written all the time, it is important to leave these register bits not used.
[0]	Bit[3] of Horizontal Fine Position for Graphic Cursor Together with SRX[7.5] as bits[2:0] this bits define the horizontal fine position. This bit should be used with 10 bit character clock (normally used with 800 x 600 panels when expanding horizontally a 640 dots image).

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3.0 Panel Format and Control Registers

R0x and R1x are reserved (not used like in 62xx)

Horizontal CRTC Registers Shadowing

In order to run VGA programs on 800x600 panels, Nordic needs to shadow the horizontal timing registers except the display enable end, which is application dependent.
(T1 has shadows only for horizontal total.)
This is because all horizontal timing registers but HDE have to be set-up for 800x600 in order to run an 800x600 panel. Symulscan with 800x600 panels runs even the CRT as an 800x600 display in all graphics modes.
In T1 as well as in Nordic, vertical panel registers are mapped at R2x, R3x,... accesible when CR2D[7] = 1. In nordic these registers remain there.
IN T1 there are two registers: **R0x and R1x** which represent HTot shadows, accessible with **CR2D[7]**. They are no longer used in Nordic, **but there is a replacement for them, independent of CR2D[7].**

In Nordic, H Total, H Retrace Start and End, H Blank Start and End are shadowed. Each entity has two values to chose from: a value for dclk/2 and a value for dclk not divided by two. The effect selection is done automatically based on SR1[3] value, but for access there is a selection bit: CR2C[4] to control which of the two sets of registers gets read or written.
Here is a summary of the horizontal shadow registers and its controls:
CR2C[5] write protect for horizontal shadow:
1 -> write both the shadow registers and the correwsponding standard VGA registers fields (some registers are not accessed entierly but only in their timing part)
read back the shadow registers

0 -> write only the standard horiz. timing VGA registers (the shadow registers are write protected). Changing onlt the value of these registers does not have any effect over the CRTC timing.
read back the standard VGA horiz. timing registers

CR2C[4] Select the set of horizontal timing shadow registers to be used (low rez or normal). This bit is reutilsed from T1: it was low power RAMDAC mode - tie now the logic L) .
0 -> select Ry for access
1 -> select Rz for access

To diferentiate from the Rx registers which still exist as in T1, and are vertical panel registers, we'll call the two sets of horizontal shadows mapped in the same address space Ry and Rz (Ry = normal, Rz = dclk/2 case)
The effect of Ty and Rz is controlled by SR1[3] (dclk/2 bit).

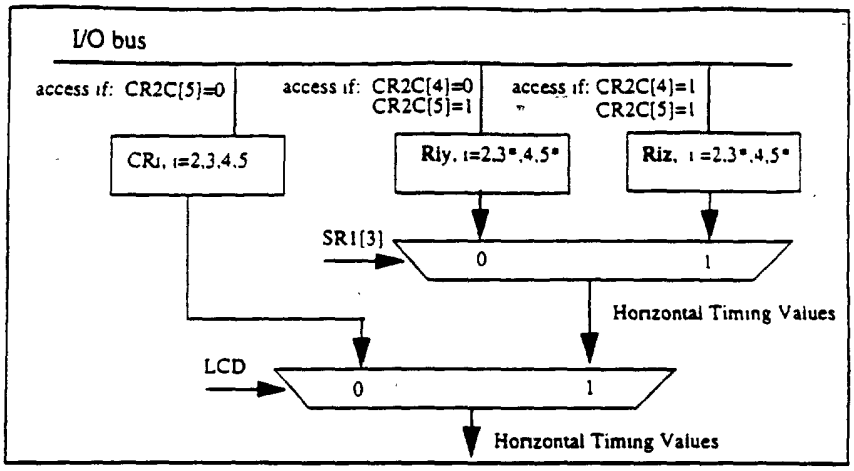
The Horizontal Timing shadow registers are:
R0y,z R02y,z R03y,z (only lower bits) R04y,z R05y,z (only lower bits)

When CR2D[7] =1 we can access only the panel registers: R2x,... RBx. In this case we cannot access either the VGA standard registers or the horizontal timing shadow registers. **Please note that R0x and R1x are reserved in Nordic. Their function is replaced by R0y,z.**

Standard VGA CR0,2,3,4,5 horizontal timing registers (only the timing fields) do not have any effect on the CRTC: only the shadow registers have effect.

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See also CR2D and CR2C description.



3.1 R9x - TFT Panel Data Format & Panel Size

Bit	Definition
[7]	Reserved
[6:4]	Select a 0 to 7 shift-clock delay from the internal character clock counter (8 VCLK/ Character Clock) to TFT panel HSYNC (LLCLK) signal; as in T1.
[3:2]	Panel Size: '00' = 640 x 480 '01' = 800 x 600 '10' = 1024 x 768 '11' = 1280 x 1024 Please note that Nordic supports only 640 x 480 and 800 x 600 STN and TFT panels.
[1:0]	TFT Panel Type: '00' = 9-bit (333); as in T1 '10' = 12-bit (444); as in T1 '01' = 18-bit (666); was x1 in T1 covering both '01' and '10' !! '11' = 24-bit (888); new in Nordic

3.2 The following registers, RCx, RDx, REx are additions for 800x600 panels, to R3x, R4x and R5x "LFS Vertical Counter Value Compare" and help with vertical automatic centering on these panels.

RCx - LFS Vertical Offset Register for 600 lines modes

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Bit	Definition
[7:0]	LFS signal least significant bits for 600 lines panel & 600 lines mode or any mode-

	that is vertically expanded to 600 lines. Write protected by CR2D[7].

3.3

RDx - LFS Vertical Offset Register for 525 lines modes

Bit	Definition
[7:0]	LFS signal least significant bits for 600 lines panel & 525 lines mode or any mode vertically expanded to 525 lines (like modes 10 and F that have 350 lines). Write protected by CR2D[7].

3.4

REx - Overflow bits for RCx and RDx

Bit	Definition
[3:2]	Most Significant Bits for RDx. Write protected by CR2D[7].
[1:0]	Most Significant Bits for RCx. Write protected by CR2D[7].

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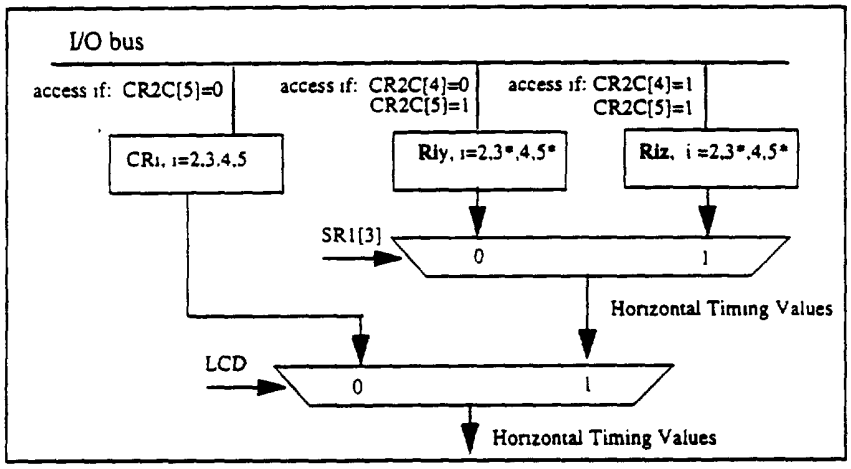
Bit	Definition
[7:6]	Shade Mapping 00 -> 18bit output of LUT upped to 24bit or direct/true color used for dithering and shading 01 -> green output of the combined 8bit data channel (LUT or True color) goes to dither and shader 10 -> Direct display of Attribute Palette address, bypassing dither ,going through shader. To be selected in text modes as well as one and two bit per pixel packed modes . Works with CR20[0] for text. 11 -> Pixel Address (6bit output of Attribute controller) bypasses dither to go to shader.
[5]	Reverse Video for Text Modes
[4]	Reverse Video for Graphics Modes
[3:2]	**Reserved**
[1]	**Text Contrast Enhancement. With R8X[4] defines the same matrix as in 62XX.**
[0]	**Enable Dithering (0=disable)**

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CR2C - Flat Panel Interface Register (was CR1C in T1)

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Bit	Definition
[7:6]	LCD Flat Panel Class Select 00 -> STN Mono Panel 01 -> grey scal plasma or EL 10 -> STN color panels 11 -> TFT color panels
[5] new	**Access Hoizontal Timing Shadow Registers Ry and Rz** **0= no access to horizontal shadow registers** **1= access both standard VGA horizontal timing and the horizontal shadow registers** At any time, the shadow registers control the CRTC. **In standard VGA on a CRT, this bit is 1 and what is written in VGA registers is also written in shadow register, so it looks as if standard VGA registers control the CRTC but they do not.**
[4] new	**In T1 this register enabled extra LLCLK for Epson panels — this feature is no longer needed in Nordic, so the bit changed function:** **SElect which set of horizontal timing shadow registers is accessed by CPU: y (normal) or z (for dot-clock divided by 2).** **0 -> Rly , i=0,2,3,4,5** **1 -> Riz**



[3]	**Protect CRTC Registers for LCD**
[2]	**MCLK Suspend Mode Power Down**
[1]	**Invert LLCLK Control**
[0]	**Invert LFS Control**

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3.5 CR2E - High-Resolution Panel Control Register

Bit	Definition
[7:6]	Actual Display Size 00 = VGA modes 01 = 800x600 actual display 10,11 = reserved for 1024x768 and 1280x1024 The value programmed in this registers affects the expansion mechanism on an 800x600 panel. If an 800x600 panel is selected at R9X[3:2] (=01) and CR2E[7:6]=01 then the expansion is disabled in graphics modes even if CR2E[3,1] expansion bits are on. With this mechanism the BIOS does not need to save the status of CR2E[3,1] every time it sets mode 800x600 so that it could restore when going back to 640x480 modes.
[5]	**Enable Horizontal Centering on Panels**: For 800 x 600 and 1024 x 768 panels
[4]	**Enable 10-dot true fonts.** Has effect only in text. Default = '0'; disabled
[3]	**Enable Horizontal Graphics Expansion** – that replicates each fourth pixel. Active only if the controller is in graphics mode. This expansion is used to expand 640 to 800 in 800 x 600 and 1024 x 768 panels. Default = '0'; disabled
[2]	**Enable Horizontal Expansion** – of an 8-wide true font to 10 dots instead of the normal VGA expansion which is to 9 dots. Has effect only in text mode. Default = '0'; disabled
[1]	**Enable Vertical Graphics Expansion**: For 800 x 600 panels: doubling of every odd scan-line in graphics in 350 and 400 line modes – replicate every forth line in 480 line modes. Default = '0';disabled When this bit = '1', and the controller is in graphics mode, the 800 x 600 expansion is enabled, and, depending on CR12 contents (with appropriate expansion bits in CR07), either odd line replication is enabled, or one line out of four replication is enabled. The comparizon with CR12 should be for smaller or equal!! This kind of expansion is used in 800 x 600 and 1024 x 768 panels when running VGA programs, and its purpose is to fill the screen as much as possible.
[0]	**Enable 800x600 panel text expansion:** Odd scan-line doubling (for 9 x 14 or 8 x 16 font) or every scan-line tripling (for 8x8 font). Default = '0'; disabled When this bit = '1', and the controller is in text mode, the odd scan-line replication is enabled. This kind of expansion is used in 800 x 600 and 1024 x 768 panels when running VGA programs and its purpose is to fill the screen as much as possible.

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CR2F - Microsoft Windows Chip ID

Bit	Definition
[7:0]	Read only register. It reads back a code to remain the same for Nordic through its entire life. Any application like MS Windows or OS/2 should ID Nordic by reading this register. For Nordic the read-back code is "CDH".

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4.0 TV-OUT Registers

4.1 CR30 - TV Out Control Register

Bit	Definition
[7:4]	Reserved
[3]	Configure Nordic and Enable the TV-OUT mode for Analogl Encoders This bit comes out on TV-ON pin If this bit is 0, NTSC/PAL pins and CSYNC pin are forced L
[2]	NTSC/PAL pin value if CR30[3] is 1 If CR30[3]=0, the value of this bit does not affect the NTSC/PAL pin.
[1:0]	Skew Control for CSYNC generation 00 = no skew 01 = skew by two dot-clocks on horiz sync start and one dotclock on half line for interlaced 10 = skew by four dot-clocks on horiz sync start and two dotclocks on half line for interlaced 11 = skew by six dot-clocks on horiz sync start and three dotclocks on half line for interlaced

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5.0 Registers for Motion Video Architecture

5.1 CR34 - MVW XS Register

Bit	Definition
[7:0]	**MVW Horizontal Start Coordinate XS** (in surrounding pel depth memory cycles) The horizontal position is programmed with 8 pixel resolution (0,8,16, .. pixels starting from the left side of the screen) (up to 1K pels in increments of 8 pels). To get an early warning, we will require **XS** to be programmed 8 pixels less than the actual position: 0 = zero, 1 = 16 pels, 2 = 24 pels, etc.

5.2 CR35 - MVW Horizontal Width XW Register

Bit	Definition
[7:0]	MVW Horizontal Width XW (MVW pel depth memory cycles) (up to 1K pels in increments of 8 pels). To get an early warning, we will require XW to be programmed 8 pixels less than the actual width: 0 = zero, 1 = 16 pels, 2 = 24 pels, etc. width.

5.3 CR36 - Vertical MVW High Position Register

Bit	Definition
[7]	Reserved
[6]	Cinepak type YUV to RGB conversion. If this bit = 0, YUV to RGB conversion is done according to the standard algorithm If this bit = 1, the YUV to RGB conversion is done based on Cinepak algoritm.
[5]	Excess 128 for YUV to RGB conversion. U and V are integer values expressed as two-th complement or excess 128. If this bit = 0, the YUV to RGB converter assumes that U and V are expressed in 2-th complement format (as in Philips SAA715B and SAA9051 TV Decoders). If this bit = 1, the YUV to RGB converter assumes that U and V are expressed in excess 128 format.
[4]	**MVW Memory Address Offset** (WMAdOf MSB)
[3:2]	**Vertical MVW End MSBs** (see CR37)
[1:0]	**Vertical MVW Start MSBs** (see CR38)

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5.4 CR37 - Vertical MVW Start Register

Bit	Definition
[7:0]	**Vertical MVW Start YS:** (in true scan-lines not affected by scan-line doubling or panel vertical expansion) 10 bits in CR36[1:0] (msbs) and CR37[7:0] (lsbs).

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5.5 CR38 - Vertical MVW End YE Register

Bit	Definition
[7:0]	**Vertical MVW End YE:** (all bits are programmed, in true scan lines) 10 bits in CR36[3:2] (msb-s) and CR38[7:0] (lsb-s).

5.6 CR39 - Surrounding Address Offset Register

Bit	Definition
[7:0]	**Surrounding Address Offset:** SAdOf (a number to be added every line to the surrounding CRT Address Counter value to allow it to jump over the MVW without counting through it. This allows calculating the surounding restart address.) This number depends on the surrounding mode resolution. Assuming a maximum line of 1024 pels, in increments of 4 pels per address (8-bits/pel), 256 addresses is enough for eight bits

5.7 CR3A - MVW Memory Address Start Register

Bit	Definition
[6:0]	**MVW Memory Address Start:** WMAdS in increments of 16KB = 4KW (a phisical address 00000:3FFFF for 1MB or 00000:7FFFF for 2MB Video Memory).

5.8 CR3B - MVW Memory Address Offset Register

Bit	Definition
[7:0]	**MVW Memory Address Offset** WMAdOf (A number to be added to the current MVW Start Address to get the next MVW start Address). Having this s/w model allows panning through a large image for the MVW. The actual image stored in memory may be as large as 2K pixels at 16 bits per pixel (two per word) -> 10bits. 10bits -> in CR36[5:4] (msb) and CR3B[7:0] (lsb).

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5.9 CR3C - MVW Pixel Format Register

Bit	Definition
[7]	**MVW horizontal zoom** (doubling)
[6]	**MVW vertical zoom** (doubling)
[5]	**Enable Live Video in Full Screen**
[4]	**Enable Motion Video Window**
[3:0]	Encode format for the first Motion Video Window 0h = 0000 = 8 bit RGB 3:3:2 going through the palette 1h = 0001 = 16 bit RGB Sierra (5:5:5) 2h = 0010 = 16 bit RGB XGA (5:6:5) 3h = 0011 = 4:2:2 YUV Y0UY1V 4h = 0100 = 4:1:1 YUV linear Y0Y1Y2Y3UV 5h = 0101 = 4:1:1 YUV array Y0Y1Y2Y3UV but Y2Y3 are in next scan line 6h = 0110 = Sashapak 6 bits for U/L 7h = 0111 = Sashapak 8 bits for U/L 8h:Fh = 0111:1111 = *reserved for future formats*

5.10 CR3D - Motion Video Window Horizontal Size Register

Bit	Definition
[7]	**MVA Data Bus Signature Generation Selection bit.** **0 = selects VGA Data Path for signatire generation** **1 = selects MVA Data Path for signature generation**
[6:0]	Motion Video Wondow width in 8 pixel units This register is used to specify the horizontal width of the MVW in 8 dot-clock units. The MVW has to be a multiple of 8 pixels. The value programmed in this register is used to terminate the MVW on each scan line.

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6.0 Registers for Panel Horizontal Timing Control

This set of four registers are used to generate horizontal panel timing with 640x480 or 800x600 panels and to center horizontally a 640dots or 720dots picture on an 800x600 panel.

6.1 CR40 - No Center Panel HDE Start Register

Bit	Definition
[7:0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. This register is used to program Panel Line Clock Start and Panel Display Enable Start with both 640x400 and 800x600 panels any time no horizontal centering is needed. Used automatically by h/w if CR41 and CR42 are not used.

6.2 CR41 - Panel HDE Start Register to Center 720 dots

Bit	Definition
[7:0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 720 dot mode (text or graphics - RIX mode only) is centered on an 800x600 panel. If horizontal expansion is on, CR40 is used. Used automatically by h/w if : 800x600 panel & No 800x600 graphics mode & 8 dot character clock & no horizontal expansion

6.3 CR42 - Panel HDE Start Register to Center 640 dots

Bit	Definition
[7:0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 640 dot mode (text or graphics) is centered on an 800x600 panel. If horizontal expansion is on, CR40 is used. Used automatically by h/w if : 800x600 panel & No 800x600 graphics mode & (9 dot character clock + horizontal display enable >= 50H) & no expansion no horizontal expansion

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6.4 CR43 - Panel HDE Dot-Clock Skew Control Register

By programming this skew, it is possible to compensate internal delays on Panel HDE for diferent types of panels. If all delays are matched the skew fields should be zero to align with character clock.

Automatic switching between these three registers will be done based on CRTC and Sequencer programming and the type of panel used
(640 x 480 or 800 x 600).

Bit	Definition
[7:6]	**Panel Line Clock Width:** '00' = 4 dot-clocks '01' = 8 dot-clocks '10' = reserved '11' = reserved
[5:4]	**CR42 value fine (dot-clock) skew:** '00' = no skew '01' = delay Panel HDE start by one dot-clock '10' = delay Panel HDE start by two dot-clocks '11' = delay Panel HDE start by three dot-clocks
[3:2]	**CR41 value fine (dot-clock) skew:** '00' = no skew '01' = delay Panel HDE start by one dot-clock '10' = delay Panel HDE start by two dot-clocks '11' = delay Panel HDE start by three dot-clocks
[1:0]	**CR40 value fine (dot-clock) skew:** '00' = no skew '01' = delay Panel HDE start by one dot-clock '10' = delay Panel HDE start by two dot-clocks '11' = delay Panel HDE start by three dot-clocks

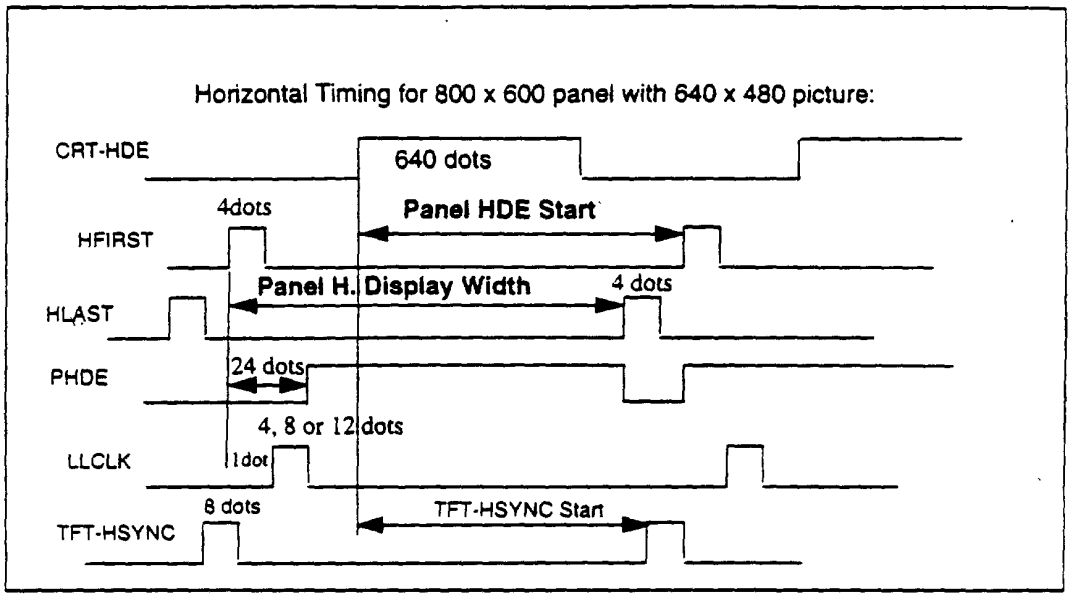
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6.5 CR44 Horizontal Panel Display Width Register

The value in this register is expressed in 4 dot-clocks (never divided by two).

Bit	Definition
[7:0]	Panel Display Width in hex expressed in four dot-clock chunks. As it is used to compensate or internal delays, this value is close but not exactly 640/4 or 800/4



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6.6 CR45 and CR46 are reserved registers. They are in the data base and can be used for future needs as control registers. They were put here in case we need one more set of honzontal registers for automatic switching between diferent modes.

CR47 - TFT HSYNC Horizontal Position Register

TFT HSYNC is about 144 dot-clocks ahead of Panel Display Enable Start. This register allows to program the exact position in dot-clock/4 from CRT-HDE start to TFT HSYNC Start. This set-up is independent of character clock width and dot-clock divide by two control. TFT HSYNC pulse width is 8 dot-clkocks.

Bit	Definition
[7:0]	TFT HSYNC start position in doc-clock/4, relative to actual panel honzontal display enable start.

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6.7 CR48 - TFT HSYNC and Panel Height Overflow Register

Bit	Definition
[7]	Reserved
[6]	Reserved for 1024 panels
[5:4]	Bits 9 and 10 of CR4A (Single Scan Panel Size and Dual Scan Lower Panel Size)
[3]	Reserved for 1024 panels
[2]	Bit 9 of CR49 - mid dual scan panel size (upper half size in scan-lines)
[1:0]	TFT HSYNC dot-clock skew 0:3 This register allows to position TFT HSYNC with dot-clock resolution.

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6.8 CR49 - Dual STN Panels Upper Half Vertical Size Register

Bit	Definition
[7:0]	Least Significant 8 bits of the Upper Half Vertical Size (in scan lines). This is relative to the start of the Vertical First pulse - the start of the panel vertical display, which in centering is ahead of the actual vertical display. Bit 9 is CR48[2]. This allows up to 511 lines to be displayed in the upper half. Please note that this are actual displayed lines (unlike the extra lines programmed in CR4B. Program mid -1 in this register (239lines programmed for 240 lines displayed).

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6.9 CR4A - Dual STN Panels Lower Half Vertical Size Register

Bit	Definition
[7:0]	Least Significant 8 bits of the Lower Half Vertical Size as well as of the Single Scan Panel Vertical Size (in scan lines). This is relative to the start of the Vertical Mid (dual-scan) or First (single scan) pulse. Bits 10 and 9 are in CR48[5:4]. This allows up to 1024 lines to be displayed in the upper half. Please note that this are actual displayed lines (unlike the extra lines programmed in CR4B. Normally the two panel halfs have the same number of scan-lines. Program last -2 in this register (478 programmed for 480 lines panel).

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6.10 CR4B - Extra Line Clocks Register

Bit	Definition
[7:4]	Extra Line Clocks added in the Upper Half 0:15 By adding extra line clocks, panel generated MOD will be affected This register should be 0 in simulscan. The line clocks added are off by one actual scan-line.
[3:0]	Extra Line Clocks added in the Lower Half 0:15 By adding extra line clocks, panel generated MOD will be affected. The line clocks added are off by one actual scan-line.

CR4C - Input Resolution Override Register for Dithering

Bit	Definition
[7]	Enable Input Resolution Override (default disable) Normally the graphics mode resolution is decoded and fed to the dither block. For all graphics modes that go through the RAMDAC RAM - 6bits/gun is automatically the input resolution. For 5:5:5 RGB or 5:6:5 RGB or 8:8:8 RGB we use a diferent input resolution: 5 for 5:5:5 and 5:6:5 and 8 for 8:8:8 RGB. In all cases the proper input resolution is automatically selected. If there is a need to overide this value, than we wiill use this bit to enable the override and write the new value in bits 3:0. For 8 bit per gun we write 8 (1000), for 6 bits per gun -> 6 (0110) and for 5 bits per gun -> 5 (0101).
[6:4]	Reserved
[3:0]	The binary value of the override input resolution. 1000 -> 8bit/gun 0110 -> 6bit/gun 0101 -> 5bit/gun

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CR4D - Output Resolution Register for Dithering

Bit	Definition
[7:4]	Reserved
[3:0]	The binary value of the output resolution for dithenng 1000 -> 8bit/gun (TFT) 0110 -> 6bit/gun (TFT) 0100 -> 4bit/gun (TFT or 16 shades STN) 0011 -> 3bit/gun (TFT or 8 shades STN) 0010 -> 2bit/gun (4 shades STN) 0001 -> 1bit/gun (2 shades STN)

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7.0 Registers for the AUDIO of NORDIC-1M.

7.1 GR60 Wave Port Control 1

Bit	Definition
[7]	Reserved
[6]	Reserved
[5]	Enable audio for host accesses.
[4]	Select 4215
[3]	Stereo for reciever (i:e STEREO CODEC)
[2]	Stereo for transmitter (i:e STEREO NORDIC)
[1:0]	Data Format select '00' 16 bit '01' 8 bit '10' 4 bit '11' reserved.

7.2 GR61 Waveport control 2

Bit	Definition
[7]	Reserved
[6]	**Power-down Conttrol:** '0' will force 'low' on PDN.
[5]	**Enable command mode.** The 4215 Audio Controller must have been placed in COMMAND mode by forcing 'low' on D/C* pin.
[4]	**Input level in SDI:** in command mode.
[3]	**Output level on SDO:** in command mode.
[2]	**Output level on SCLK:** in command mode.
[1]	**Output level on FSYNC:** in command mode.
[0]	**Output state of D/C* pin.**

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7.3 GR62 - Input Audio Threshold setting.

Bit	Definition
[7:0]	Available only for 16-bit mode. Only +VE data is compared; i.e, if msb of left data is '1', no compare is performed.

7.4 GR65

Bit	Definition
[7]	Enable Threshold detect mode.
[6:0]	Reserved

7.5 GR66 - Audio Input Codec Write Pointer - high byte

Bit	Definition
[7:0]	Audio Input Codec write pointer - high byte

7.6 GR67 - Audio Input Enable and Codec Write Pointer - low byte

Bit	Definition
[7]	Enable input from codec to audio buffer.
[6:0]	Audio Input Codec Write Pointer (low 7 bits of 15 bit pointer)

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7.7 GR6A - Audio Output Codec Read pointer - high byte

Bit	Definition
[7:0]	Audio Output Codec Read pointer high byte

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7.8 GR6B - Audio Output Codec Read pointer low byte

Bit	Definition
[7]	Enable output to codec from audio buffer.
[6:0]	Audio Output Codec read pointer (low 7 bits of 15 bit pointer).

7.9 GR6C - Interrupt Control.

Bit	Definition
[7:6]	Reserved.
[5]	Standard VGA Interrupt disable. '0' = Allow VGA interrupt '1' = Disable VGA interrupt.
[4:2]	Reserved.
[1]	Audio Input interrupt control ----> DURING RECORD SESSION. '0' = Disable this interrupt source. '1' = Enable input buffer full OR programmed full interrupts.
[0]	Audio Output interrupt control ----> DURING PLAY SESSION. '0' = Disable this interrupt source. '1' = Enable Output buffer empty OR programmed empty interrupts.

7.10 GR6D - Interrupt Status.

Indicates any active enabled interrupt. Reading this register will clear the interrupt state and reset the status. No effect on the standard VGA interrupt status or interrupt. For all of the following bit positions, a '1' in the bit means PENDING INTERRUPT.

Bit	Definition
[7:6]	Reserved.
[5]	Standard VGA Vsync interrupt (state of 3C2(7)).
[4]	Reserved.
[3]	Record Buffer FULL (OVERRUN).
[2]	Record Buffer PROGRAMMED FULL.
[1]	Play Buffer EMPTY. (UNDERRUN)
[0]	Play Buffer PROGRAMMED EMPTY.

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7.11 GR6E - AUX1 and AUX2 control

Bit	Definition
[7]	Enable Aux Sel 1 low-true output on adress match 530-53Fh.
[6]	Enable Aux Sel 2 low-true output on adress match 388-397h.
[5:0]	Reserved.

7.12 GR6F - Codec status.

Bit	Definition
[7:4]	Reserved
[3]	Timer status (ADI) time slot 6 bit 7
[2]	Overrange (OVR) time slot 7 bit5
[1]	PIO1 input status. time slot 7 bit 7
[0]	PIO0 input status. time slot 7 bit 6

7.13 GR70 - Codec control DWORD from Nordic to codec. byte D7:0

Bit	Definition
[7:0]	Codec control DWORD from Nordic to codec. byte D7:0

7.14 GR71 - Codec control DWORD from Nordic to codec. byte D15:8

Bit	Definition
[7:0]	Codec control DWORD from Nordic to codec. byte D15:8

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7.15 GR72 - Codec control DWORD from Nordic to codec. byte D23:16

Bit	Definition
[7:0]	Codec control DWORD from Nordic to codec. byte D23:16

7.16 GR73 - Codec control DWORD from Nordic to codec. byte D31:24

Bit	Definition
[7:0]	Codec control DWORD from Nordic to codec. byte D31:24

7.17 GR74:75 - Interrupt value for audio IN buffer.

Bit	Definition
[7:0]	Interrupt value for audio IN buffer. When the CODEC reaches the programmed adress -1, an interrupt is generated during the record session.

7.18 GR76:77 Interrupt value for audio OUT buffer.

Bit	Definition
[7:0]	Interrupt value for audio OUT buffer. When CODEC read pointer reaches the programmed adress -1, an interrupt is generated during the play session.

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8.0 Registers that Overlap in T1 and AVGA3, now moved to other locations.

8.1 CR1B[7,4:2] - Bits are Reserved in Nordic

Bit	Definition
[7,4:2]	R1B in schematics All these bits do not seem to be actually used. I do not think that they are needed in Nordic.

8.2 CR1C(T1) - Moves to CR2C

8.3 CR1D(T1) - Moves to CR2D

8.4 SR7(T1) [6:4] Not used, keep the function of AVGA3.

8.5 SR8(T1) - Moves bits as follows:

Bit	Definition
[7]	moved to SR23[7] but with reversed polarity (assymtric DRAM)
[6]	remains in SR8[6] (disable MCS16* for Video Memory)
[3]	Reserved in Nordic - Suspend inpout is active 'high' (no selectable active polarity like in T1)
[2:0]	moved to SR24[2:0] (SW2:0 read-back)

8.6 SRF[7](T1) - Not used, becomes a constant '0'.

8.7 SR16(T1) - Moves to SR20; Pads Threshold and Power Control

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8.8 SR1A(T1) - Moves to SR21 Test Register, in case it is needed.

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9.0 Register Bits of AVGA3 which are not used in Nordic

The following register bits are not used in Nordic, though they are in AVGA3 data base. In most cases (if not specified otherwise) they can be taken out together with the logic related to them When specified, they will be preserved in the data base together with the related logic.

9.1 SR8[7,5:0] - Used for EEPROM programming - not a Nordic feature

9.2 GRE[0] - DCLK/2 to Feature Connector

10.0 Register Bits in T1 not used in Nordic

10.1 SR7[6:4]

Switch read back from MD pull-ups in 486 bus, is not used in Nordic. SR7 will have the same function as in AVGA3.

10.2 SR8[3]

Supend Input active polarity in T1. This is not used in Nordic, since in Nordic SUSPI is always active 'high' polarity.

10.3 SRF[1:0]

MCLK frequency select in T1 are not used in Nordic: only SR1F is used. See new definition of SRF.

10.4 CR1C[2:0]

"MCLK Suspend mode power down", "Invert LLCLK", "Invert LFS" are not used in Nordic. Instead, Nordic will always stop MCLK and VCLK in Suspend, and will have a positive polarity on LLCLK and LFS.

11.0 Register Bits with Similar, but Different, Functionality in Nordic vs. T1

11.1 CR20[2:1] - Refresh Select

Refresh Select is almost the same in Nordic as in T1, but, when '11', not only RAS and CAS are set to high-impedance, but all Nordic outputs going to the Memory (MA, MD, WE, OE, CAS, RAS) are set to high-impedance. To be used with NEC's GDC option.

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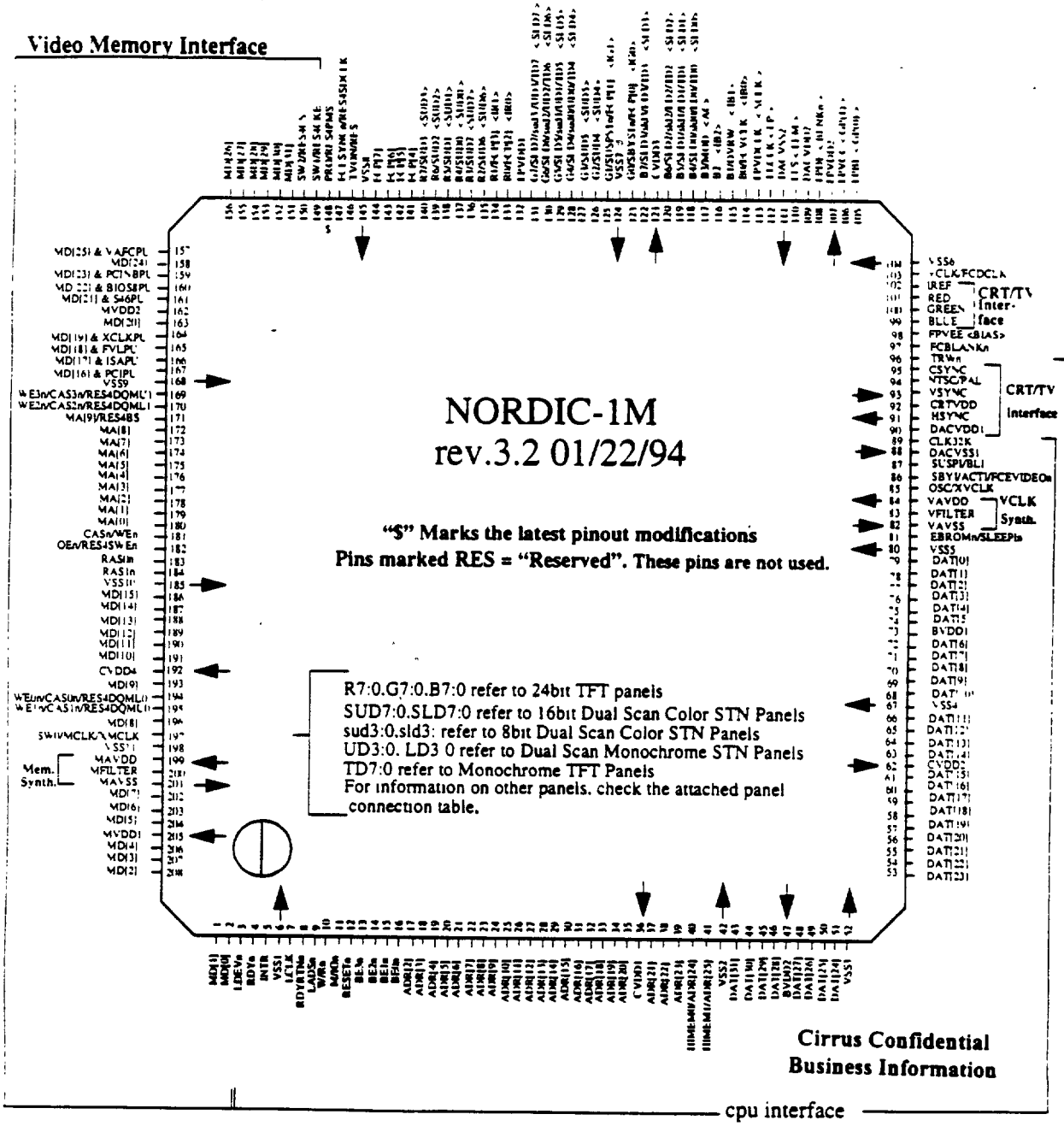
```
User name:    SHAW (11)                    Queue:  UIDESK/UNIX_UIMKGT
File name:                                 Server: CLFPCD010
Directory:
Description: NORDIC40.
             December 21, 1998                                  5:46pm
```

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RX-577 C

```
                          SSS  H   H   A   W   W
                         S   S H   H  A A  W   W
                         S     H   H A   A W   W
                          SSS  HHHHH A   A W W W
                             S H   H AAAAA W W W
                         S   S H   H A   A WW WW
                          SSS  H   H A   A W   W


                         L      SSS  TTTTT
                         L     S   S   T
                         L     S       T    : :
                         L      SSS    T    : :
                         L         S   T
                         L     S   S   T    : :
                         LLLLL  SSS    T    : :
```

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Panel & FC interface
Video Memory Interface
NORDIC-1M
rev.3.2 01/22/94
"$" Marks the latest pinout modifications
Pins marked RES = "Reserved". These pins are not used.
R7:0.G7:0.B7:0 refer to 24bit TFT panels
SUD7:0.SLD7:0 refer to 16bit Dual Scan Color STN Panels
sud3:0.sld3: refer to 8bit Dual Scan Color STN Panels
UD3:0. LD3 0 refer to Dual Scan Monochrome STN Panels
TD7:0 refer to Monochrome TFT Panels
For information on other panels, check the attached panel connection table.
CRT/TV Interface
VCLK Synth.
Mem. Synth.
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cpu interface

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DELTA LIST OVER PREVIOUS PINOUT RELEASED ON :

08/26/93:

- no POUT on SW2/POUT
- XVCLK moved from SW1/VCLK/XVCLK to OSC/XVCLK. This way SW1/VCLK/XVCLK became SW1/VCLK.

09/06/93

- All panel pins whose names were not starting with the color panel name were changed such that the names start now with the color panel pin (R7, G7, B7 and so on). So it was only a pin name change.

09/12/93 rev. 1.0 and 1.1

1. Took-out Whisper Support Pins: WWRn, WRdn, WAD[3:0], FPCn.

2. Reduced the number of CPU Address Pins: ADR[24:27] went-away. Use HIMEM to place the chip outside 16MB of memory for linear addressing.

3. Killed CRTVDD and placed CRT Interface on Host Bus VDD.

4. Introduced VAFC pins in a unique pinout configuration in both VESA VL and PCI.
Added VAFCPU a pull-up to enable VAFC (VESA Advanced Feature Connector).
ADR[27:24] become VAFC pins. and R[7:4], G[7:6] , CLK32K, SUSPI/BLI, SBYI/ACTI get a configuration for VAFC -> total 14 pins.
SW0/VCLK will be used as VAFC DCLK, losing SW0 pin as panel type when VAFCPU is used.
In PCI bus, no ADR pin will be shared with VAFC.
ASW0PU will be added on MD pins to replace SW0 pin when VAFC is enabled by VAFCPU. SW0PU will read-back in the same register bit as SW0, so the BIOS will not feel any modification in the reporting scheme The chip will draw more power in suspend with VAFC.

5 Moved SW2, SW1/MCLK/XMCLK, the two RESERVED pins and TRWn on MVDD to prepare for SDRAM pin compatible option in the next Nordic that supports SDRAMs. It looks that we need only 3 more memory pins to support SDRAM-s so TRWn will not be used. It was moved so it is on the right VDD bus if needed.

6. Moved CVDD3, VSS3, VCLK Synth. H/VSYNC, EROMn, SW0 per Thomas Hung's request to fit the floor plan.

09/21/93

1. Added AUXS1 on D/Cn as an option to be used with CS4231S as CS.
2. Added AUXS2 on EROMn/VADRn as an option to be used for Sound Synthesizer Chip Select.
3. Rearanged 5428 FC pins due to a previous error : R5 and R4 should not be used with FC.
   - FCP[1:0] are shared with G7 and G6.
   - SW2 and the two pins reserved for SDRAM were moved in between Video Memory pins and Panel pins and one of them is used as FCESYNCn.
   - OVRWis shared with CLK32K, FCBLANKn is shared with SUSPI and FCEVIDEn is on SBYI.
4. Renamed the External Clock PU XCLKPU instead of XMCPU.

10/11/93 rev. 1.3

1. Moved some external pull-ups.
2. Added alternate pin functions on panel pins as well as actual schematic name for engineering

10/27/93

1. Added TV-OUT (called also NTSC-OUT) pins on the panel pins

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10/28/93 rev. 1.5 Modifications

1. Added TVG on EBROMn/AUXS2 and took out VADR as an option on this pin.
2. Put back FCESYNCn on RES4SDCLK as an option (deleted by mistake).

11/11/93 rev.2.0 Modifications

1. Reset became RESETn, active L to correspond with the defined reset signal for VESA VL and PCI.
2. TFT Panels Data Pins R7:R0, G7:G0, B7:B0 changed and all pins got rotated to get them ordered from right to left. Due to this change now Ri=TVRi, Gi=TVGi and Bi=TVBi.

01/06/94 rev. 3.0 Modifications

1 Update Panel Data Pins based on Robin's Table.
2. Move MOD pin on a Panel Data Pin used in 18bit TFT.
3. Move OVRW on a 24bit Panel Data Pin.
4. Removed pin configuration for TV-OUT support with digital encoders. All pins marked TV... were removed. As a result, some pins like LLCLK, LFS, FPDE, FPVDCLK have one function now.
5. Removed WavePort pins, including AUDVDD: total 7 pins freed.
   AUX2 and TVG muxed on EBROMn are no longer needed either.
6. Added one more CPU address pin: instead of HIMEM, Nordic has now HIMEM0 and HIMEM1, corresponding to CPU Address 24 and 25 or any other external decode of the high order CPU address bits. In the process of adding this pin, most CPU Interface pins on the right side were moved to the right by one pin.
7 Added CRTVDD supplying HSYNC, VSYNC, CSYNC, NTSC/PAL CRT and TV Interfaces output buffers.
8 EBROMn is shared with TVON, the power-on signal for AD720. So, in ISA bus with on chip BIOS support, AD720 power on cannot be directly controlled by Nordic.
9 Added pins for Analog TV Encoder support - AD720 and MC1377 :
   a. CSYNC = Composite Sync signal
   b. NTSC/PAL = 1 -> NTSC, 0-> PAL (for AD720, but it is TV Encoder Dependent)
   c. EBROMn/TVON (see #8).
10 ASW0PU "Alternate Switch 0 Pull-Up" pull-up on pin 155. MD[26] was removed, as SW0 is now not multiplexed.
11. De-multiplexed some of the pins previously multiplexed:
   a. Pin 168 TWRn/RES4PMS is now RES4PMS, a pin reserved for synchronous DRAM support.
   b. SUSPI/BLI/FCBLANKn is now SUSPI/BLI, not affected by the Feature Connector Enable Configuration
   c. As a consequence of b, pin 97 is FCBLANKn (not muxed with anything). Please note that FCEVIDEOn is still muxed with SBYI/ACTI as before, as Standby Input and Keyboard Activity are less important functions in a system.
   d. SW0 is no longer muxed on VCLK/FCDCLK. So VLK/FCDCLK is a pin but it moved to pin 103 in the PVDD area, to be consistent with FC power supply.
12. SW1, muxed on MCLK/XMCLK (pin197) became SW0. This is just a name change to have the switches placed in a more consistent manner.

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13. SW1 is now muxed with a reserved pin: RES4CKE. pin 148. which before was totally reserved. The idea here is to go for pu/pd with SDRAM-s for SW2 and SW1. while keeping SW0 on MCLK even with SDRAM-s.
14. Pin 147 is Reserved. It is actually one of the WavePort pins. but placed in-between Memory and Panel VDD busses (on MVDD) for maximum flexibility To acheive this. the pins on its right were moved to the right by one FPVEE <BIAS> moved down to pin 98 (it was 105)
15. TRWn is now by itself on pin 96. on FPVDD.
16. The names of all flat panel data pins reflect the panel type table attached to this document.

01/13/94 rev. 3.1 Modifications

1. On EBROMn/TVON -> EBROMn/SLEEPIn with SLEEPIn an input which if L puts Nordic to sleep (as 3C3[0] and 46E8(3).
2. TVON is now on RES, but TVON/RES is pin 146 and FCESYNCn/RES4SDCLK is pin 147.

01/22/94 rev. 3.2 Modifications

1. Pin 148, RES4PMS which was a pin resurved for synchronous DRAM-s, got a function: it is now a programable output PRO and it is on FPVDD instead of MVDD. The intention is to optionally use this pin to control a switch between 5V and 3.3V, in which case a H level of 5V is desirable. My primary choice for this function is actually NTSC/PAL pin which is on CRTVDD, but if the TV-OUT option is used in a system and a switch between 5 and 3.3V is provided, PRO may be used.

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Panel Interface Data Formats (compatible with 62xx family except 18/24 bit TFT)

TFT 24/ 18/ 12/ 9 bit Name	Pin	DB44#	STN Color 16bit/8bit	Monochrome dual STN / single TFT
R7/R5/R3/R2	141	(13)	SUD3 / ---	---
R6/R4/R2/R1	140	(14)	SUD2 / ---	---
R5/R3/R1/R0	139	(15)	SUD1 / ---	---
R4/R2/R0	138	(16)	SUD0 / ---	---
R3/R1	137	(9)	SUD7 / ---	---
R2/R0	136	(10)	SUD6 / ---	---
R1	135		---	---
R0	134		---	---
G7/G5/G3/G2	132	(8)	SLD7 / sud3	UD3 / TD7
G6/G4/G2/G1	131	(7)	SLD6 / sud2	UD2 / TD6
G5/G3/G1/G0	130	(6)	SLD5 / sud1	UD1 / TD5
G4/G2/G0	129	(5)	SLD4 / sud0	UD0 / TD4
G3/G1	128	(11)	SUD5 / ---	---
G2/G0	127	(12)	SUD4 / ---	---
G1	126		---	---
G0	125		---	---
B7/B5/B3/B2	123	(4)	SLD3 / sld3	LD3 / TD3
B6/B4/B2/B1	121	(3)	SLD2 / sld2	LD2 / TD2
B5/B3/B1/B0	120	(2)	SLD1 / sld1	LD1 / TD1
B4/B2/B0	119	(1)	SLD0 / sld0	LD0 / TD0
B3/B1	118		---	---
B2/B0	117		---	---
B1	116	(23)	MOD	MOD
B0	115		---	---
FPVDCLK	114	(18)	SCLK / XCLKL	SCLK
LLCLK	113	(35)	LP	LP
LFS	111	(22)	FLM	FLM
FPDE	109	(26)	--- / XCLKU	/ DE

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RX-578 C

NORDIC-1M Design Specification

by Vlad Bril, Robin Han, Sasha Eglit, Rakesh Bindlish, Dwarka Partani.
Jeff Ort
rev.3.9 October 10, 1993

1.0 Introduction & Table of Contents

Nordic is Cirrus Logic's Fourth Generation Flat Panel VGA Controller to be marketted in first half of 1994.
Nordic-1M is a mid-end member of the Nordic family. It is a GUI Accellerator with PCI support and Multi-Media Features.
Nordic-1M is targetted for the mid to high end of the **Note-book Computer Market** and for for the energy efficient **desk-top computers mother-boards**.
Nordic-1M is **not** targetted to the adapter market.

1.1 Table of Contents

This Specification will address the following:

1. Introduction and Table of Contents
2. Basic Feature Set
3. Detailed List of Features
4. Pinout and Pin Description
5. Architecture Specification
6. Register Specification
7. Product Implementation Plan

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2.0 Nordic-1M Basic Feature Set

1. **Flat Panel VGA Compatible GUI Accellerator register and feature compatible to 5428 and Alpine I A/V. Priority: A (= highest).**
2. **32bit CPU, 32bit Video Memory, 32bit BLT and 32bit CPU to Video Memory Data Path. Priority: A (= highest).**
3. **208 pin QFP package.**
4. **Targeted to sample CY Q1'94, production CY Q2 '94. Priority: A (= highest).**
5. **Target cost: $12 to $10 -> less than 400mil [/] in C8 Foster City.**

6. **Multimedia Features**

- Part of a well defined **System Solution** for high performance **CD-ROM video and audio playback** for the portable market. **Priority: B**
- Part of a well defined **System Solution** for mid performance **low cost live NTSC Video and Audio with the NTSC decoder on a PCMCIA card. Priority: B**
- **Audio Port to Display Memory**: Audio Buffer to Serial Interface for CS4248 Audio Codec. **Priority:** C (CS4215 is not fit for notebook computers).
- **Video Playback decompression accelleration for CinePak** including Color Space Conversion (YUV -> RGB). **Priority: B**
- **Live Video in a 320x240 or 640x480 Window** from a propnetaryly compressed TV decoded data source (at 30Hz) on TFT color panels. Data is stored compressed and it is decompressed to 18bit/pel or 24bit/pel in real time at display time. NTSC decoder and data compressor is on the PCMCIA card or the PCMCIA controller. Please note that due to live video bandwidth requirements on PCMCIA bus , a relatively non-expensive way to achieve the second feature is to implement this compression algorithm. **Priority: B**
- Color Key Live Video Overlay based on a 5428-like Feature Connector with PCI bus (only).

7. **Integrated in Nordic 1-M**

- Color Space Converter for CinePak. **Priority: B**
- 18bit DAC with direct color capability **Priority: A**
- *24bit RAMDAC with true color capability* **Priority: C**
- Clock Synthesizers for Video and Memory Clock (65MHz/3V, 110MHz/4.5V). **Priority: A**

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- DAC IRef Current Source on chip. **Priority: C.** *Boyd and ManShek are working on it*

8. **Direct Bus Interface**:

- 32bit VESA-VL bus (and 486 local bus) **Priority: A**
- 32bit PCI bus. No on chip BIOS ROM support in PCI. **Priority:** A
- 16bit ISA bus for demonstration and easy system validation. **Priority: B**
- 32K or 48KB BIOS ROM support in ISA and VESA VL bus. **Priority: B** (only for BIOS/ system debug)
- At least 5 scratch pad registers: optimum 8 scratch pad registers. **Priority:** A.

9. **Performance Enhancements** to achieve 15-20MWinmarks at 1Kx768 8b/pel:

- 32bit BitBLT with memory mapped I/O BitBLT registers (as in 5428 ?or Alpine) Priority:A
- BLT buffer of 8 (~~or 16~~) bytes for Source (and Destination ?) data. (5428 buffer is 8bytes, Alpine is 16bytes) (as 5428)
- *X/Y offset for Pattern BLT (as in Alpine)* **Priority:** C
- h/w graphic cursor 64x64 (as in 5428)
- color expansion (as in 5428)
- linear memory addressing (as in 5428)
- 4 stage 32bit wide write buffer and capability to page CPU cycles if accumulated in the write buffer (this is already in 5428)

10. **Display Memory:**

- *0.5MB (16bit wide),* 1MB or 2MB memory addressing 32bit wide (as in 5428)
- *1 or* 2 256Kx16 one bank or 4 256Kx16 two banks (2 CAS symetric, 2 WE asymetric) (as in 5428)
- maximum memory clock frequency: 50MHz/3V, 65MHz/4.5V **Priority:** C

11.**Flat Panel Support: [Priority: A]**

- Color TFT (24bit, 18bit, 12bit, 9bit)
- Color Dual Scan and *Single Scan STN* (16 and 8 bit, including dual clock panels)
- Monochrome TFT (8bit),
- Monochrome Dual Scan STN (8bit),
- Monochrome Single Scan (4 and 8bit) support

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- Simulscan with all Fast Panels (6.3MHz or equivalent) with 32bit wide memory.
  No simulscan with 16bit wide memory with dual scan color panels.
  No simulscan for 3MHz monochrome dual scan panels.
- 640x480 single and dual scan support (Priority:A)
- 800x600 TFT *and no single and dual mono and color STN panel support (Priority: C)*
- 1024x768 TFT *and no single and dual scan STN panel support . (Priority: D)*

12.Display Features

- High quality monochrome and color shading, at least as good as 6440. Priority: A
- Shading option for fast panels. Priority: B
- Up to 8, 64x64 Hardware Icons independently mapped color+transparent background. **Priority: C**
- *Whisper Cross-Talk Reduction (If panels will be available in the time frame and if we can accomodate it with the shading algorithm). **Priority: C***
- ***"Office Productivity Booster Dual Display"*** 640x480 (panel) & 640x480 (CRT) 4 or 8b/pel or 640x480 (panel) & 1024x768 (CRT) 4 or 8b/pel ***Priority: E***
- Vertical Expansion in text and graphics (as in 6235 or 6440)
- Automatic Centering if not expanded (as in 6235)
- *Grey-Shades Maping options ?? Is this needed ? Priority: D*
- Text Contrast Enhancement options. (as in 6235 or 6440)
- *Inking Plane ?? Priority: D*
- *180 and 90 degree image rotation ?? Priority: D*
- *12 and 16dots wide font support ?? Priority: D*
- *h/w offset on h/w cursor ?? Priority: D*

13.Resolutions Supported:

- the same as 5428 at 5V (4.5Vmin)
- up-to 45MHz dotclk (1024x768, 60Hz interlaced) at 3.3V

14.Power Management

- Mixed 3.3V and 5V operation: memory, host and flat panel independent VDD
- Green-PC spec support. **Priority: B**
- Stand-by Mode with internal stand-by timer (as in 6235)

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- Suspend Mode I/O or pin in all modes (LCD, CRT,Simulscan)
- *Light Sleep ?? - better not for this chip as it requires too much h/w. Priority: F*
- Panel Power Sequencing: automatic or under I/O control (as in 6235)
- Reduced Active Power in Panel Only Operation: < 60mAmp @3.3V. **Priority:A**
- Reduced Suspend Current: < 0.5mAmp. **Priority: A**

2.1 Inputs from the Nordic-1M Features Meeting of 09/10/93

- 24bit DAC if not too expensive (VAR)
- mclk @5V max 65MHz, @3V max 50MHz
- vclk and fpvdclk @5V max 85MHz, @3V max 65MHz
- **panels:**
  - TFT 1280x1024? ##, **1kx768 ##, 800x600 ##**, 640x480
    24bit,18bit, 12bit, 9bit color, 6bit mono
    NEC analog output? ##
  - STN 800x600 dual scan color, 640x480 ds color 16bit
    640x480 ss color 8bit
    640x480 mono bit 8bit and 4bit
  - horiz ## and vertical centering
  - normal 9dot font in 800x600 text ##
  - simulscan for 800x600 and 1kx768 panels ## (need to run all modes at 800x600 or 1024x768 rezolutions -> option to clock panel till h&v Blank)
  - support for two alternate fonts 10x24 for 800x600 (10x18 actual with spacing) and 12x25 for 1kx768 ## difficult !!
  - h&v text expansion in 800x600 and 1kx768 panels ## ?
  - color text enhancement ## : bright white instead of white
  - *on chip cross-talk reduction ##* ? - any improvement ?
  - *shading look-up tables ##* ? - only if not too large
- ***NO Whisper support even on the bus side - out !***
- ***NO one 256Kx16 DRAM support - out !***
- **h/w icon support:** with h/w cursor, up to 4 simultaneously. Horizontal position controlled in increments of 64 pixels.
  Icon attributes: off/on, 4 colors/3colors + transparent, no_blink/blink, (simple/double).
  H/W cursor goes over the h/w icon (visually). Uses independenly mapped color in RAMDAC RAM. Start at scan-line 64.
- PC98 integration? ## - to be negotiated
- reserve pins for SDRAM-s and CDRAM-s ##
- ***NO true dual display!***

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2.2 Inputs from Compaq 09/10/93

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- 50MHz 486DX bus
- 75Hz refresh rate
- **need one 256Kx16 support with Audio and some video for Contura - build one motherboard for Contura and LT Lite. Two DRAM-s only on LT Lite.**

- think that 8KB/buffer of audio buffer is not enough
- want to use Analog Devices for Audio
- No clear winner on conpression. They are watching. Need Indeo driver.
- Play-back zoom is required. At least pixel replication.
- Very interested in Compressed Live Video. WAnt to talk more.
- need h/w icon 64x64 with 3col+transparency or 4 color, with pixel replicanon to 128x128.

2.3 Inputs from AST 09/15/93

- They prefer horizontal icon

2.4 New Features as of 10/04/93

- 4bit/pel packed support for Windows Chicago
- 8bit/pel video out to the Feature Connector for conversion to NTSC-out with Nordic running 640x480 interlaced mode.
  Another idea was to use some of the panel outputs in this case and extend the data out to 16bits.
- The h/w icon can be horizontal or vertical using the Motion Video Window as implementation vechicle -> is it worth?
- IBM Raleigh asked for 12 and 16dots wide fonts for h/w assisted Kanji. 10/04/93
- IBM Raleigh asked for 8bit monochrome TFT panel support. 10/04/93

3.0 Important Additions to 5428 Data Base

1. **32 bit CPU Data bus in VESA VL bus support**
2. **PCI bus support**
3. **Mono and color, STN and TFT Flat Panel support (incl. hfb).**
4. **Live video in a true color window with Windows running in planar VGA mode, without a video port (using PCMCIA standard bus and Sasha's decompression technique).**
5. **CINE PAK decompression accelleration**
6. **Audio Port support for CS4215**
7. **Power Management: panel power sequencing, stand-by mode, suspend mode**
8. **Mixed Voltage, 3.3V operation and low active/suspend/standby power**
9. **h/w icon support, with a h/w cursor support**
10. **BLT performance improvements: Memory Mapped BLT I/O, patternning, 16 byte Source buffer**

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5428-1-0004-00

11. *[dual display 1024x768 on CRT with 640x480 on LCD, using the same RAMDAC] - if decided to do now*

4.0 Detailed List of Features

4.1 WAS: On the Cross Talk Reduction Technique -> not in -1M

This part was deleted from Nordic-1M spec starting rev. 3.8 (09/11/93).

4.2 Green PC Spec Support (Based on VESA DPMS Proposal 1.0p rev. 0.53p)

This specification refferes to CRT Monitor power management. Additionally, Nordic will

TABLE 1. Display Power Management Summary

State	HSYNC	VSYNC	Video RGB	Compliance	Power Savings	Recovery Time
CRT On	Pulsese	Pulsees	Active	Mandatory	None	NA
CRT Stand-by	No Pulses	Pulses	Blanked	Optional	Minimal	Short
CRT Sus-pend	Pulses	No Pulses	Blanked	Mandatory	Substantial	Longer
CRT Off	No Pulses	No Pulses	Blanked	Mandatory	Maximum	System Dependednt

control DAC power consumption. These power management CRT Monitor states are not necessarily related to the graphics controller power management states.

We'll define 2 bits - GRE[2:1] (the same as Alpine) that control HSYNC, VSYNC and DAC Power Off signal (or Blankn to the DAC).

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TABLE 2. GRE[2:1] Effect

GRE[2:1]	CRT State	Vsync	Hsync	DAC Power	Nordic Power Management State
0	On	pulsing	pulsing	on	active
1	Stand-by	pulsing	static at MISC[6] inactive level	off	active
2	Suspend	static at MISC[7] inactive level	pulsing	off	active or stand-by
3	Off	static at MISC[7] inactive level	static at MISC[6] inactive level	off	active, stand-by or suspend

If Nordic is in its own Suspend mode, the BIOS should program GRE[2:1]=3 to put the monitor (if any) in the Off state.

If Nordic is in its own Stand-by mode, CRT Suspend mode should be forced bt the h/w, as stand-by is a timer driven mode and no s/w gets to play.

If Nordic is in LCD only, the BIOS should set GRE[2:1] to 3 to power off the CRT that may be connected to the notebook computer.

If CRT only mode and CRT is in stand-by or suspend, the BIOS may reduce the video clock and even memory clock frequencies after saving the current values.

Except for the above restrictions, CRT Power Management modes are not related to Nordic power management modes: they can be independently programmed.

If MISC bit is programmed for positive polarity, the SYNC signal will be stopped L, otherwise it will be stopped H.

4.3 Play-back Decompression Accelleration (applicable to Cinepak as well as other compression standards) - old, kept here only for reference

4.3.0 The problem

a) When playback data is compressed on a CD ROM, it is encoded in 24bit/pel YUV with crominance sub-sampling. Due to CDROM reduced bandwidth the display window is 160x120 or 320x240. If this compressed data is decompressed at full pixel depth, it should be displayed as 24bit/pel RGB window under MS Windows. As the play-back data is sent to the graphics controller from the CPU bus, it has to be placed in Video Memory in 320KB.

A standard VGA controller or even GD5428 are able to display the 24bit/pel play-back window only if MS Windows is run in 24bit/pel mode (for instance 1024x768 24bit/pel or 640x480 24bit/pel) by the driver. Under these conditions, the CPU will have to write the un-compressed 24bit/pel play-back data in the appropriate position in Video Memory, contigouus to the entire displayed data.
So, in order to display 24bit/pel in a play-back window, GD5428 needs the driver to run 24bit/pel at the maximum display resolution.
But, in order to run 640x480 at 24bit/pel we need 921.6KB of Video Memory and in order to run 1024x768 24bit/pel we need 2359.296KB of video memory. (Please note that 2M of memory has 2097.152KB).
Also, when running windows in 24bit/pel mode the performance will decrease 3 or 4 times relative to 8bit/pel mode, especially when using DRAM as Video Memory.

b) When running through MS Windows GDI, the driver can play-back data at 15fps or less (with a 486 33MHz). It is desirable to play-back data at 30fps.
This can be accomplished today only if the driver does not go through GDI.

c) If a picyure was stored on CDROM at low resolution (160x120 or 320x240) and it needs to be "zoomed", it has to be interpolated both horizontally and vertically for good picture quality. Vertical interpolation is expensive in h/w.

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4.3.1 The Generic Solution - old, here for reference only

Today's Windows Accellerators run MS Windows, including the play-back window with the same pixel depth (8bit/pel), normally going through the RAMDAC, but using a split palette approach with 16 colors reserved for MS Windows and 240 colors reserved for the play-back window. The Cinepak driver writes data in video memory in 3:3:2 RGB format

(8bits/pel) which is created by the driver. Because of the s/w overhead involved in decompression as well as the GDI overhead, it is hard to go beyond 320x240 clips at 15fps, though the display quality is much lower than what Cinepak could achieve (240 colors versus 16 million colors).
To run Cinepak with 24pit/pel resolution, today's graphics controllers would require to run MS Windows in 24bit/pel mode, requiring almost 1MB in 640x480 and over 2MB-s in 1024x768 modes.

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A graphics controller that could run MS Windows in 8 or 16bit/pel mode while displaying only the play-back window in 24bit/pel mode would increase significantly picture quality without degrading too much MS Windows performance with play-back. would reduce significantly the amount of Video Memory required for the same picture quality and would allow a higher frame rate for the play-back.

Further, if the play-back data is stored in Video Memory in a semi-compressed format that requires less than 24bit/pel this would further decrease the Video Memory requirements and it may even reduce the video memory band-width requirements.

When zooming the play-back window from 160x120 to 320x240 or higher it is important to interpolate. Vertical interpolation can be done in s/w but with a relatively large overhead. It may be possible to do vertical interpolation on key frames, but there is no practical way of doing vertical interpolation on inter-frames either in s/w or with h/w assist on the CPU write side of the graphics controller. If s/w driven vertical interpolation on key frames is not a solution, then verical interpolation can be only achived in h/w on the CRT read side and this requires either one or two 16bit/pel line buffers or a big penalty on video memory bandwidth (the equivalent of reading 32 or 48bits/pel).

Horizontal interpolation can be done before play-back data is displayed, without s/w help.

Please note that there are multiple ways to solve the play-back problems. In Nordic-1M we'll try to strike a ballance between the complexity of the h/w solution and the quality of the play-back image.

To a large extent, the solution adopted in Nordic-1M will be generic, not tied to Cinepak, though it will be first applied to Cinepak.

4.3.2 Nordic-1M old Play-back Accelleration Solution -> canned, kept here for reference

a)Nordic-1M will run Cinepak at 1:1 scale exactly the same way as today's graphics controllers: in 8bit/pel MS Windows with 8bit/pel (3:3:2 RGB) play-back window.

b)Nordic-1M will run 1:2 scale (zoom) in 8bit/pel 1024x768 MS Windows with 24bit/pel (8:8:8 RGB) pixel depth in the play-back window, horizontally interpolated and vertically doubled. Play-back data will be stored in video memory as 16bit/pel (Y0 U01 Y1 U01).

c)Nordic-1M will run at 1:1 scale in 16bit/pel 1024x768 MS Windows with 24bit/pel pixel depth in the play-back window. Play-back data will be stored in video memory as 16bit/pel (Y0 U01 Y1 U01). This mode is good for programs that store data in 320x240 format.

Because today large play-back windows look bad, while small ones look OK, this solution will improve picture quality to a large extent.

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Concerns:

Many play-back programs today don't even have a zoom option. To this extent, mode "b" may not be needed.

Mode c could be implemented today with 16bit/pel RGB (555) in s/w and the only improvement we provide is 24bit/pel capability and h/w color conversion (some level of accelleration). So mode "c" may not be needed as a special h/w.

If this is the case, maybe we do not need to do anything in h/w for Cinepak !

One idea: should we run 24bit/pel MS windows stored in 4:2:2 (Y0 U01 Y1 U01) format? This will allow us to run 24bit/pel MS Windows and use 16bit/pel memory space with no loss of quality. The windows driver could compress the data and the h/w could decompress it.

4.4 Nordic-1M Motion Video Architecture

4.4.0 The Problems to Solve & Generic Solutions

Nordic-1M is supposed to support CDROM play-back and live-video under Microsoft's Video for Windows. With all of today's VGA Compatible Graphics Controllers, the play-back picture pixel depth has to be the same as the surrownding MS Windows pixel depth. In other words, we have to run MS Windows in a 24bit/pel mode in order to display 24bit/pel in the play-back window.
The only way we can run today live video is from a Video Port (= Feature Connector). In this case we'll use an overlay or a color key to define the live video window.
Due to CDROM player, s/w interface complexity, CPU bus and Video Memory limitations, only small clips at 15fps or less can be playd-back today. So today we need a lot of Video Memory to run small clips in slow motion at low rezolution. Nordic-1M will try to use less Video Memory, increase the clips size, their resolution and speed.

Nordic-1M is supposed to support:

- accellerated play-back for all popular CDROM compression standards, especially Cinepak and Indeo
- live video from a PCMCIA card in a system with a standard PCMCIA host adapter, for a "Multimedia-Ready Notebook Computer"
- live video from a Feature Connector, preferably VESA Advanced Feature Connector compatible, for a Multimedia Notebook Computer with direct NTSC input (full motherboard solution).

What will Nordic-1M bring to the Video plate:

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A. Nordic-1M will break the dependency between the pixel depth of MS Windows and the pixel depth of the live-video / play-back window. By doing so, Nordic-1M will be able to run 24bit/pel LV/PB while running MS Windows in 8bit/pel or 4bit/pel (even planar). This will lead to high quality live-video and play-back, while minimizing Video Memory requirements.
B. Nordic-1M will further reduce Video Memory requirements as well as Video Memory Bandwidth requirements by storing data in compressed form: 4:2:2 YUV (16bit/pel), 4:1:1 YUV (12bit/pel) or Sashapak YUV (2.6bit/pel)
C. Nordic-1M will define one architecture and work-frame to run both play-back and live-video in a unitary way for both s/w and h/w.
D. Nordic-1M will support up to two active LV/PB windows at the same time.
E. By providing h/w YUV->RGB conversion and 1:2 zoom Nordic-1M will accellerate playback for most standards, but mostly for standards that allow us access to their decompressor like Cinepack (for whose decompressor we have a licence).

Nordic-1M will not provide Cinepak specific accelleration (custom BLT).

On the Live Video from Feature Connector (or Video Port)

Due to pin-out limitations, the VAFC implementation has to be limited to 8 pins of data requiring external muxing of 16bit data to Nordic. Further, the VAFC solution will be restricted to 5428 type support: overlay and color key (no memory video port). The only additions to the 5428 support will be the internal YUV-> RGB converter able to accept sequential 4:2:2 YUV (16bit/pel in avarage: Y0,U,Y1,V) and display it as a 24bit/pel RGB in the overlay/color-key window. We may also support horizontal 1:2 zoom with avaraging. Nordic-1M will be back-wards compatible to 5428 and it will support also 16bit 5-5-5 RGB Sierra and 5-6-5 RGB XGA pixel formats. As in 5428, live video from the Feature Connector can be executed only from mode 5F (640x480 256 colors).

In the following we will refer mostly to the other two modes of operation: play-back and live video from a PCMCIA card, which we'll call compressed live video, because due to PCMCIA bus bandwidth limitations, we assume that video data received by Nordic is compressed with Sashapak (see Sashapak detailes further in this spec). Please note that due to its huge advantages, it makes sense to use Sashapak as a mother-board solution too. The main reason we continue to support the Feature Connector based live video is the availability of drivers for 5428 which will give Nordic an early start in the live video arena.

Video Memory Band-width Constraints

Please note that, even with a 32bit wide Video Memory, there are severe memory band-width limitations when running 16bit/pel and 24bit/pel graphics modes.

Assumming that Nordic-1M does 8 CRT fetches in a row and 1 CPU cycle, for a CRT or TFT panel, here are the minimum frequency requirements for memory clock frequency at different rezolutions and pixel depths:

24bit/pel:

R+7P+R=12m+14m=26m with 1 CPU cycle per CRT FIFO fill fetches data for 32B/3B=10pixels

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R+7P = 6m+14m = 20m with no CPU cycle during non-display time
min mclk freq = 65MHz / 50MHz @ 640x480 -> Nordic-1M upper limit at 5V CVDD
= 104MHz / 80MHz @ 800x600 -> too high
= 169MHz / 133MHz @ 1024x768 60Hz -> too high

16bit/pel:
R+7P+R=12m+14m=26m / R+7P = 20m fetches data for 32B/2B=16pixels
min mclk freq = 40.6MHz / 36MHz @ 640x480 -> OK even at 3V
= 65MHz / 50MHz @ 800x600 -> Nordic-1M upper limit at 5V CVDD
= 105MHz / 83MHz @ 1024x768 60Hz -> too high

12bit/pel:
R+7P+R=12m+14m=26m / R+7P=20m fetches data for 32B/1.5B=21pixels
min mclk freq = 30.9MHz / 23MHz @ 640x480 -> OK even at 3V
= 49.5MHz / 380MHz @ 800x600 -> OK even at 3V
= 80.4MHz / 64MHz @ 1024x768 60Hz -> too high

8bit/pel:
R+7P+R=12m+14m=26m fetches data for 32B/1B=32pixels
min mclk freq = 20.3MHz @ 640x480 -> OK even at 3V
= 40.6MHz @ 800x600 -> OK even at 3V
= 52.8MHz @ 1024x768 60Hz -> OK at 5V

We may conclude that Nordic-1M will be able to run 24bit/pel only at 640x480 rezolution, 16bit/pel up to 800x600, 12bit/pel up to 800x600 and 8bit/pel up to 1024x768 rezolution. These results apply only to CRT or TFT and single scan STN panels.
Please note that for dual scan STN panels the memory requirements increase significantly.

These severe memory bandwidth limitations lead us to attempt to minimize video memory traffic. If we store **Cinepak data in 4:2:2, with an avarage of 16bit/pel**, independent of Cinepak window size, **Nordic-1M will not be able to run Cinepak above 800x600.**
Any attempt to execute vertical zoom with interpolation, even with two points interpolation will further aggravate this memory band-width bottleneck. The next step should be 100MHz SDRAM-s with a large CRT FIFO (32x32) or 64bit wide memory data bus.
These considerations apply to any playback compression standard that stores data in video-memory as 16bit/pel in avarage. The key to a successful compression standard would be one that does decompresssion on the CRT memory read and stores data in memory as 8bit/pel or less, in avarage.

As we store live video at 2.6bit/pel and fetch it as if it was 8bit/pel with Sashapak. Nordic-1M should be able to run live video even at 1024x768.

If we defined a new CDROM play-back standard based on Sashapak, then we could run even 1024x768 with 24bit/pel accuracy and keep it memory as an 8bit/pel. **Keith and Ken are actually working on it, with Sasha's help.**

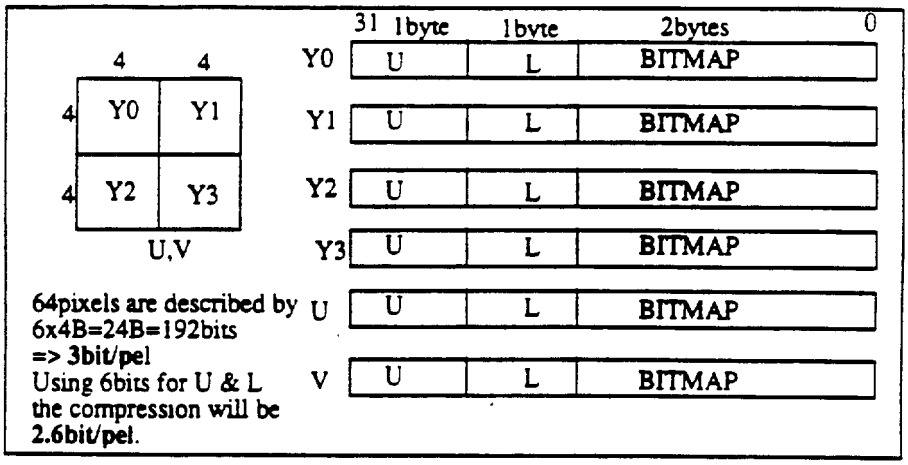
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4.4.1 On Sashapak

Sashapak is a highly assymetric, lossy "Block Truncation" compression algorithm optimized for visually equivalent image processing.
Data is proccessed as Y,U,V one byte each. U and V are sub-sampled, characterizing one 8

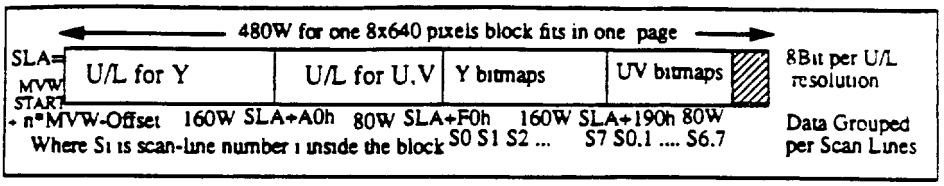
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by 8 pixel array, while Y is characterizing a 4x4 pixel aray. Actually one of two values is assigned to each pixel inside the 4x4 (for Y) and 8x8 (for U and V).
At compression time, the compression chip determines a threshold and two values U&L for each group of sixteen (4x4) pixels. This way all pixels above threshold will be assigned the value U, all pixels below threshold will be assigned the value L.



At decompression, the bitmap will control a mux between the U and L values. This way the decompression is straightforward.
The main drawback of this approach is that a BITMAP contains Y data from 4 scan lines and U,V data from 8 scan lines. When data is read from memory to be displayed only data from one scan line is used. Similarly the U/L values apply to several scan-lines and the same value will be read in each scan line. The same data will be read again and again in each scan line raising the actual memory bandwidth requirements to an equivalent of 16bit/pel map.
In order to overcome this problem and reduce memory bandwidth requirements, Sasha proposed a **scan line oriented, segregated mode of data organization**. This would require the Sashapak compression chip to write compressed data in a specific way putting the strain on the compresion chip address generator. The basic principles of the new organizations are:
1. Data is organised in the MV Window in chunks of 32 sequential pixels.
a)For **8bit U/L resolution**, as one Y covers 4 pixels, 8 U/L sequential values are needed, 16bits each -> **8x16/32=4W** (8x12/32=3W for 6bit res. U/L) (where W is a 32bit word).
b)U and V U/L data is packed together in the same word (16bits for U U/L and 16 bits for V U/L -> total 32bits=1W) and as one pair of U and V applies to 8pixels, 4 such values are needed for 32 sequential pixels -> **4x32=4W**. (4x12x2/32=3W for 6bit res. U/L)
c) The mask data is also scan-line oriented: all 32bits of Y mask of sequential 32pixels are placed in one 32bit word and due to sub-sampling on U and V, all 32bits of U and V mask of sequential 32pixels are placed in one 32bit word. So in 2W data for 32 sequential pixels on one scan line is packed. -> **2W** (the same for 6bit resolution for U/L)
d) For 640x480 window size, even at 8bit U/L resolution, data for 8 scan-lines fits in one DRAM page (symetric DRAM-s assumed): 320WY+80WU+80WV=480W < 512W page

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f) The key to memory bandwidth optimization is the fact the the compression chip will organize data sequentially over 32 pixels instead of 8. This will be done for the mask bits which will be organized sequentially by scan line and for the U/L data. This way a 32bit word of Mask data contains only information for the current scan line and no extra memory fetches are required. The main reason we segregate U/L for Y and U/V is the fact that we want to use 6bit U/L. In this case it is easier to identify the proper U/L info chained within 32bit words if the words are sequential and we have a fix relationship between their address and the 6bit U/L quantities.

g) If we calculate now the amount of data we need to fetch to display 32 sequential pixels:

- for 8bit per U/L: 4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B
  --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
- for 6bit per U/L: 3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B
  --> 32B/32pixels = 8bit/pixel

This is a very good data fetch ratio, much better than the 16bit/pel we'd get without the optimization.

g) When reading data from the Motion Video Window the controller will generate the following sequence of addresses, all of them in the same DRAM page (8bit per U/L):

- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset, +1, +2, +3
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h, +1, +2, +3
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h
- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset+4, +5, +6, +7
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h+4, +5, +6, +7
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h+1
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h+1
- now the MVW FIFO is full.
- chunks of ten 32bit words will be proccessed for every 32pixels displayed
- the MVW FIFO gets empty after the first 10 words being read for decompression and display.

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Please note that all data for every 8 scanlines starting from the top of the MVW is in the same DRAM page.

Because we have to fetch the MVW Data before we start displaying it, and because at that

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time the CRT FIFO does not empty as fast as it is needed (unless MS Windows is running at the same pixel depth as the MV Window), it is necessary to have a separate FIFO for the MVW or at least half the FIFO (at least 10W for 8bit per U/L and at least 8W for 6bits per U/L).
h) When we run 6bit per U/L, because the Video Memory band-width requirements are as if we were running 8bit/pel, we could do vertical zoom with avaraging. But there should not be a need for zoom with Live Video because there is enough CPU and memory band-width to run 640x480 windows even when MS Windows is run as 1024x768 4 or 8bit/pel.

Conclusion: With Sashapak we can get data organized in memory such that the memory bandwidth is as for 10bit/pel (8bit U/L) or 8bit/pel (6bit U/L) pixel depth. The actual memory area will be close to 3bit/pel or 2.6bit/pel depending on the resolution of U/L values - 8 or 6bits per value.
Please note that the memory area will be slightly larger due to the fact that we use only 480 words in a page of 512.

4.4.2 YUV to RGB Conversion Algorithm

The ideal YUV to RGB transformation is:
R=Y+1.37V
B=Y+1.73U
G=Y-0.699V-0.336U

After defining an objective way of measuring color error, Sasha came up with the following Conversion algorithm:
R=Y+1.375V=Y+1 3/8 V
B=Y+1.75U=Y+1 3/4U
G=Y-0.375U-0.75V= Y-(3/8U+3/4V).

This algorithm can be implemented with 8 9bit adders.

4.4.2 Motion Video Architecture Functional Blocks

Instead of treating play-back and live-video as two separate modules, we'll isolate several generic functions to be used by both:

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- Display Window Generation Block:
  allows s/w to define one or two play-back or live video window(s).
  The MV Window is defined in 4bit/pel equivalent CRT Addresses:
    - MVW Start Address (19bit)
    - MVW Width (max 640pixels => 80 addresses) -> CRT address after MVW on each scan line.
    - The number of memory cycles to be executed at MVW pixel depth on each MVW scan-line (max 320 cycles for 16bit/pel storage at 32bit/pel pixel depth) -> scan line end.
    - MVW OFFSET to the start of the next MVW Scan Line (19bit)
    - MVW End Address (19bit) or MVW number of scan-lines (9 bits).

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Scan-line doubling for "zoom" should be taken into account when designing DWG.

- Off-screen MV Memory Addressing and Access Control. This includes data type tag generation based on MV memory Address and the circuitry placing the tags in the CRT-FIFO. This also includes the MV prefetch cache that makes sure that there is enough prefetched MV data before starting and MV scan line display. This block has provisions for scan line replication by repeating the MV address generated on the previous scan line of the MV window (only).
- One tag bit is generated based on CRT Address and is 1 if the data in the CRT FIFO and the pre-fetch buffer is from the MVW, other-wise is 0. This tag bit, called the steering bit will be delayed through the entire data path and end up controlling the final video data mux just before the DAC

- MV Data Path and CRT-FIFO Control. This is area wise the largest piece. It consists of a new 16bit wide data-path with the same delay as the VGA data path, that takes MV data from the MV prefetch cache and the CRT FIFO, treats it appropriately depending on the MV data format encoded in the MV tags and converts it to 24 bit YUV first and 24bit RGB second. Horizontal zoom with avaraging (or maybe 5 levels of interpolation) is in this block too.

- Pre-fetch MVW Buffer - is needed in order to pre-fetch scan line data for the Motion Video Window every scan-line. Because the MS Windows pixel depth and MVW pixel depth don't match, it is necessary to fill in a separate buffer every
MVW scan line before the CRT-Address Counter reaches the window boundary.
The buffer will be filled first during vertical non-display time and later after each VMW scan-line display. For Sashapak this buffer has to store data for 32pixels
(10x32bit for 8bit per U/L or 8x32bit for 6bit per U/L).
This function can be implemented as a dinamic size modification in of the CRT-FIFO. If the CRT-FIFO has 24 stages instead of 16 but only 16 stages are used before the MVW but it is switched to 24 when MVW fetches start, there will be 8 more stages to fill at that time ensuring more prefetched data in the CRT-FIFO at the beginning of each MVW scan-line.

- Steering logic decode the tags comming out of the special addition to the CRT-FIFO and the pre-fetch buffer and controls the decompression, formatting and serialization.
(they tell the formatter what data is Y, U or V).

- While switching to display the MVW the CRT Address counter continues to count at the pace set by the graphics mode outside the MVW (4 or 8 bit per pixel normally). The counter contents is compared with the MVW boundaries to detect the end of the MVW.

- What about the video serializer load and the CRT FIFO read signal? What hapens to them when in VMW? They are one signal today.
WHEN the data path switched to display VMW data, what hapens with the VGA Video Data Path is don't care as we do not display that data, except for the h/w cursor anf the h/w icon that do not go through the standard VGA serializer. So we'll probably stop the VGA data path untill the point h/w cursor and h/w icon are combined into it, to save power, as we will stop the VMW data path when not in use, for the same reason.

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So, the Video Serializer Load may be stopped while VMW data is displayed, but the CRT FIFO read will be going on, with a frequency and shape depending on the data format loaded in the CRT FIFO for didplay.
At the beginning of each VMW scan-line, the CRT-FIFO signal read will be applied only to the pre-fetch buffer and not to the CRT-FIFO itself (the CRT-FIFO read pointer won't change). Subsequently, when the pre-fetch buffer is empty (format dependent), the CRT-FIFO read will be applied to the CRT-FIFO read pointer after the data the pointer is pointing to was loaded into the VMW formatter and serializer.
In RGB 3:3:2 8bit/pel direct color mode CRT-FIFO read will be generated every 4 vclks.
In standard RGB 5:5:5 or 5:6:5 16bit/pel modes CRT-FIFO read will be generated every two vclks.
In YUV 4:2:2 24bit/pel (Y0 U Y1 V on one scan line) the CRT-FIFO read will be generated also every two vclks.
IN Sashapak 10 (for 8bit per U/L) or 8 (for 6bit per U/L) CRT-FIFO read pulses will be generated every 32 vclks.
- The VMW Address Counter, loaded at the beginning of each VMW scan-line with a start address calculated based on the Start VMW Address and the VMW Address Offset, will count at format dependent rate for as long as the CRT-FIFO is not full. Because the CRT-FIFO will be emptied faster in the VMW (in general the pixel depth will be higher in the VMW) there will be requests for more memory cycles when displaying in the VMW.

- If either h/w cursor or h/w icon are on, they should be displayed even if the direct data path is used. In this case both video data pathes will clock and the steer tag will point to the VGA data path when either h/w cursor or h/w icon or both are displayed, even on top of a MV window. Please note that neither the h/w cursor, not the h/w icon data go through the CRT FIFO or the VGA Data path except for the final pixel address block and the RAMDAC RAM, though they have a special path in the RAM. So we could stop most of VGA data path (including the internal palette) but not all of it even if we are in 16bit/pel mode (the new one that goes through a separate 16bit data path).

- If we are in a 16bit/pel mode with no h/w cursor or h/w icon, or in a 640x480 MVW mode filling the screen, we can stop the VGA data path to save power.

- The off-screen MVW memory will be a fix memory array towards the end of the memory, but before h/w cursor, h/w icon and the half frame buffer, even the color one. The start of the MVW memory will be fix for a memory size but it will be moving with the memory size: **2MB configuration will support enough memory to support:**
- one 640x480 3bit/pel window or up to two 320x240 3bit/pel (Sashapak) -> 32KW
- one 640x480 16bit/pel window or two 320x240 16bit/pel windows
(153.6KW=614.4kB out of 256KW or 512KW available depending on the memory configuration).
- all of the above at the same time up to a total of two windows though.

1MB configuration will support:

- one 640x480 3bit/pel Sashapak window or two 320x240 Sashapak windows or
- two 320x240 16bit/pel windows.

In general, the MVW off-screen memory start address is fix, but it can grow into hfb memory if there is no hfb.

We may decide to place the start of the MVW memory array at either one of two locations to optimize for TFT panels versus STN color.
PLease note that about 56KW are needed for 800x600 DS Color STN HFB, the h/w cursors and h/w icons while about 36KW are needed for 640x480 DS Color STN HFB and that

- 640x480 4bit/pel requires 38.4KW
- 800x600 4bit/pel requires 60KW
- 1024x768 4bit/pel requires 98.3KW
- 640x480 8bit/pel requires 76.8KW
- 800x600 8bit/pel requires 120KW
- 1024x768 8bit/pel requires 196.608KW

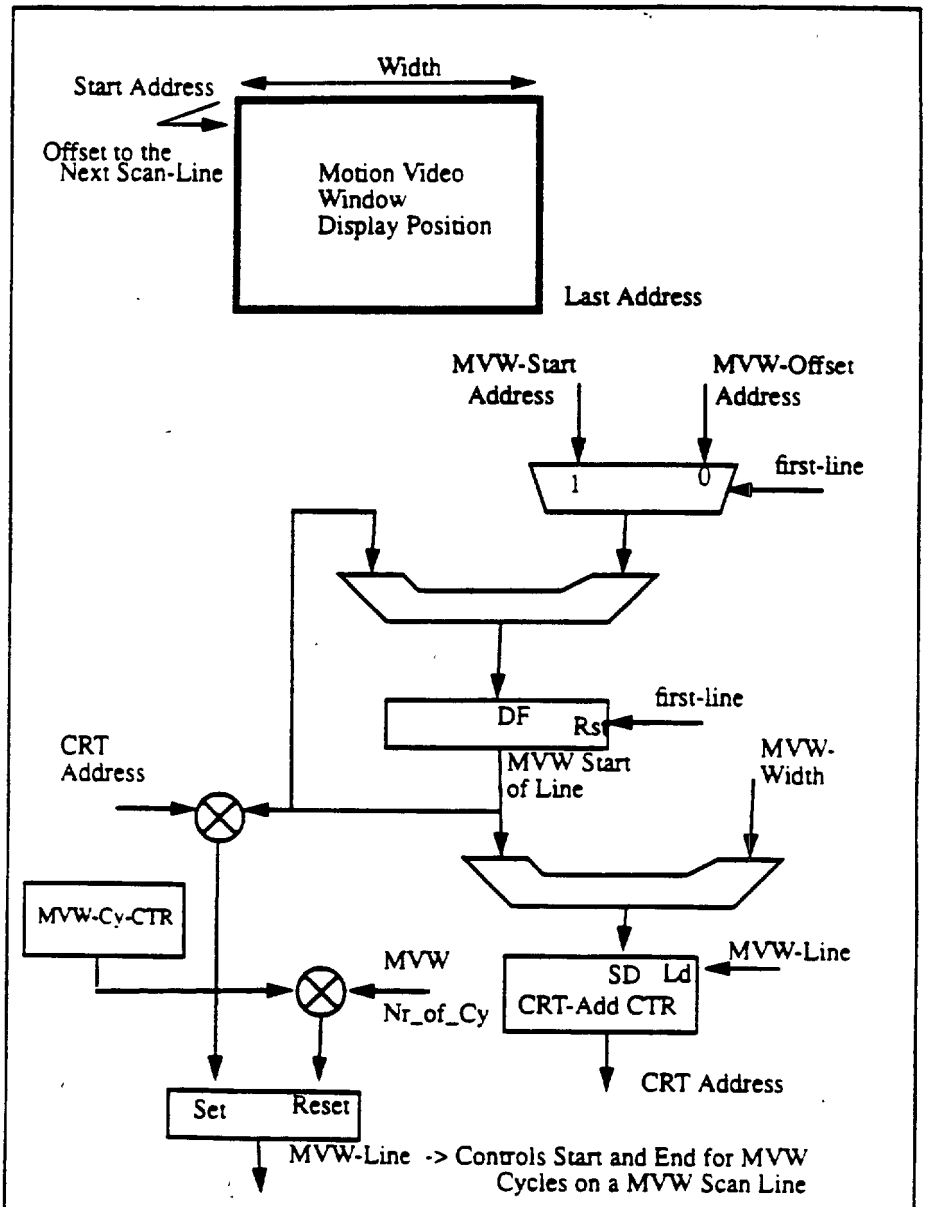
Video Motion Formats supported are:
- 8bit RGB not going through the palette (RGB 3:3:2)
- 16bit RGB (5:5:5 Sierra and 5:6:5 XGA) not going through the palette -> this is a 16bit/pel that does not require double dotclock !!
- 4:2:2 YUV Y0,U,Y1,V for Cinepak (or 4:1:1 if proven more useful)
- Sashapak format (Y0-ULM, Y1-ULM, Y2-ULM, Y3-ULM, U-ULM, V-ULM)

The tags that accompany the motion video data through the CRT-FIFO mark both the data format and the type of data inside the format (U/L for Y or U,V or mask for Y or U,V in Sashapak, Y0, Y1,U or V in 4:2:2).

Note: It may prove simpler to design a system in which the MVW is defined on the Horizontal and Vertical Counters instead of the CRT-Address. In this case, for the system tobe simple we should fetch both normal CRT data and MVW data on the scan-lines on which there is MVW data. Other-wise we have to prefetch CRT data during the window.
The system would have two separate FIFO-s. A MVW will be detected during the horizontal non-display time of the previous scan line and a MVW FIFO fill will occur. Once the MVW FIFO is empty, a refill will be in order. The CRT FIFO will be refilled before the MVW ends unless the CRT FIFO cycles continue normally during the MVW, which requires a lot of memory bandwidth.

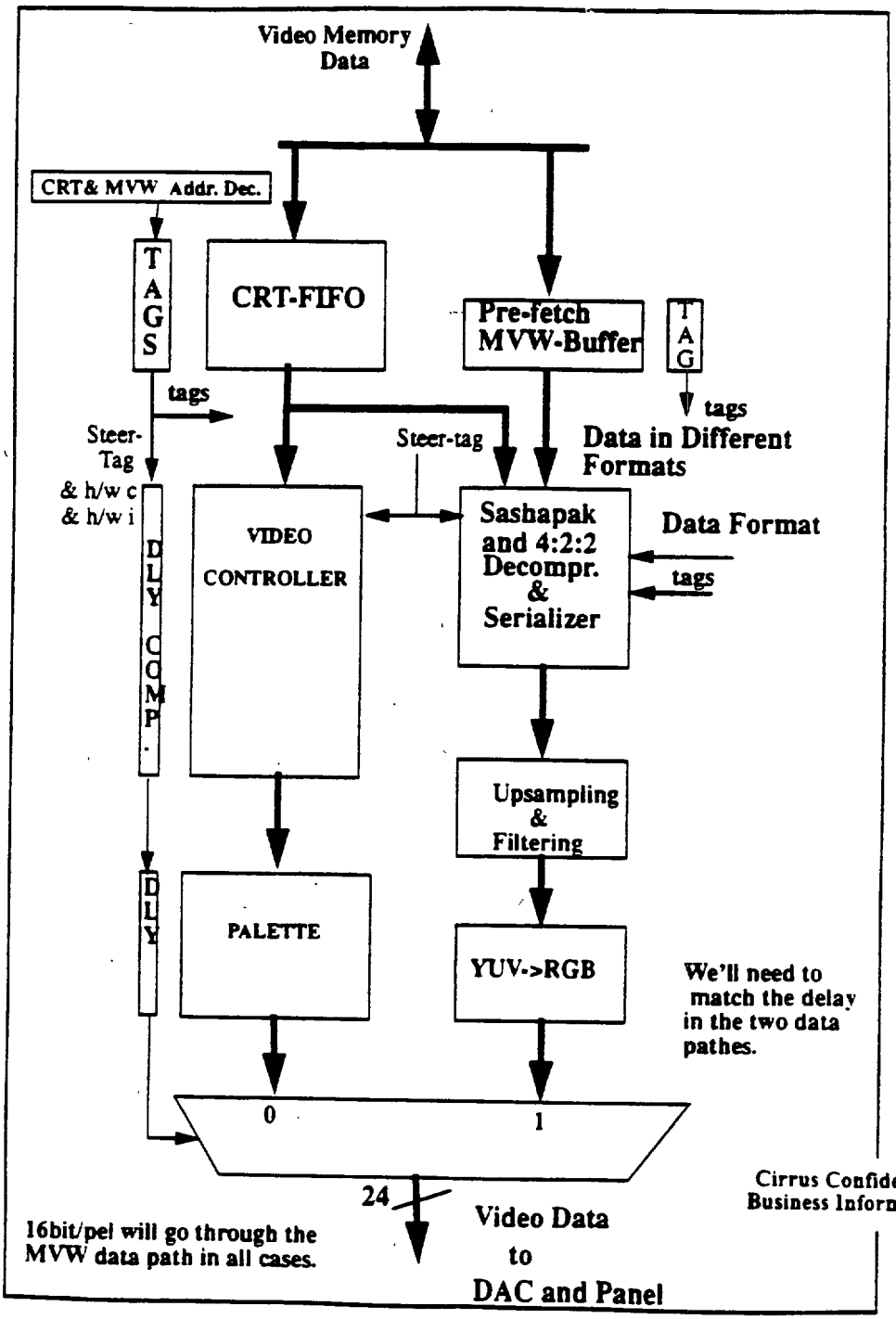
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Note: For timing considerations MVW-Start Address and MVW-Last-Address will be programmed as minus 1 or even minus 2 if required, to allow early detection of a window boundary.

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Video Memory Data
CRT& MVW Addr. Dec.
TAGS
CRT-FIFO
Pre-fetch MVW-Buffer
TAG
tags
tags
Steer-Tag
& h/w c
& h/w i
Steer-tag
Data in Different Formats
DLY COMP.
VIDEO CONTROLLER
Sashapak and 4:2:2 Decompr. & Serializer
Data Format
tags
Upsampling & Filtering
DLY
PALETTE
YUV->RGB
We'll need to match the delay in the two data pathes.
0
1
24
Video Data to DAC and Panel
16bit/pel will go through the MVW data path in all cases.
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4.5 Feature Connector Support

Nordic-1M will support 5428 Feature Connector so that it is compatible to Media Manager.
Nordic-1M will support VAFC (Vesa Advanced Feature Connector) in the 8bit VSVPC passthrough compatibility mode.
The main difference beteen 5428 FC and Nordic FC is the fact that 5428 FC has one EDCLKn control pin controlling the direction of the DCLK pin, while Nordic-1M as well as VAFC have a FCDCLK output pin and a FCVCLK input pin.
Dave Keene believes that 5428 FC is VAFC compatible. To ease the design, I kept 5428 FC pin names (not VAFC pin names).
On VAFC compatibility here are some comments:
- GENCLK can be applied on XVCLK if SR22[3]=1.
But, if SR22[3]=1 (select xclk) & SR24[7]=1 (VAFC enabled), then XMCLK should get OSC and MCLK Synthesizer operates normally, except that the reference frequency comes from XMCLK instead of OSC pin. If SR22[3]=1 & SR24[7]=0, then MCLK comes directly from XMCLK pin and the MCLK and VCLK Synthesizers are powered-down !!
- GRDY signal is similar to OVRW.
- VRDY is similar to EVIDEO if EVIDEO is dinamically switched as a valid data in signal.
- EGENn is not needed if we configure Nordic-1M in the right configuration with SR22[3] (XCLKPU) and SR24[7] (VAFCPU).
- As VAFC maximum FCVCLK frequency is 37.5MHz, VAFC supports a mode in which data is sent at 37.5MHz to the DAC and it each pixel will be displayed twice if the chip is running at 75MHz pixel clock. This allows only 8bit/pel data to be displayed. To display 16bit/pel data we should use both phases of the FCVCLK and pack the data into one pixel. I think that this is already done in 5428, if not Man-Shek and Fong-Jim are modifiying the 5429 RAMDAC to support this mode -> we need to support it too.
- VAFC requires FCDCLK to be switchable under s/w control beteen 1x and 1/2x the pixel clock. If we took this out of Nordic-1M data base, we should put it back, but the divide by two should affect only FCDCLK going out of the chip.

Check VESA VAFC Proposal 1.0p rev. 0.31 07/15/93 for VAFC timing info.

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Nordic-1M FC Pins Functional Description

Most of this is from 542X Data Sheet page 3-26:

VSYNC and HSYNC	TO	The standard CRT pins tri-stated when FCESYNCn is L. Thes pins have programable polarity.
FCBLANKn	I/O	BLANKn in 5428. If FCESYNCn is H, this is an output and it supplies the actual composite BLANKn CRTC signal. VAFC requires this to be the composite Display Enable (no borders). If this is the case, we'll need a bit for VAFC that puts DE = HDE & VDE inverted on BLANKn.

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If FCESYNCn is L, FCBLANKn is an input and it forces RAMDAC RAM outputs to 0 (black), but it should force them black before they go to the panel.
It seems that by connecting OVRW output to BLANKn as input we can display FC data in a window - this will work though only if OVRW, internally controls the pixel address mux between normal VGA data and the FC data.

FCP[7:0] I/O P[7:0] in 5428.
If FCEVIDEOn is H, these pins are outputs and represent the pixel address of the RAMDAC.
IF FCEVIDEOn is L, these pins are inputs and represent the pixel address to the RAMDAC.
CR1A[3:2] control the way the FCP[7:0] are muxed with the normal data.

FCDCLK O (the actual pin is I/O) outputs VCLK or VCLK/2 if selected through s/w.

FCESYNCn I ESYNCn in 5428. Controls HSYNC, VSYNC and FCBLANKn (H-> outputs, L-> H/VSYNC are tri-stated, FCBLANKn is tri-stated.).

Nordic does not have EDCLKn input as FCDCLK and FCVCLK are not shared.

OVRW O OVRW in 5428 = Overlay Window. **This active Low** signal, is generated by the BLANKn VT and HT logic (shared) and is supposed to be used to create an Overlay Window in which data from the Feature Connector is displayed. *I don't know why we output this signal. It should be controlling the MUX between the normal pixel address and the FC originated pixel address.*

4.6 On WavePort Architecture and Audio Driver

Starting from Dave Keene's WavePort Specification, Rakesh, Sasha and Vlad came-up with some ideas which could greatly simplify the design work for WavePort, reduction the complexity and the number of gates of the WavePort.
We'll start with the small issues and move towards more important issues.

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4.6.1 AUXS1 and AUXS2 Pin

A. Dave proposed to share this pin with PDN (Power Down) WavePort Pin and configure it as AUXS2 when using 4231S.
We noticed that 4231S does have a PDN pin which we'd like to use to save power.
We'll put AUXS2 on another pin.

B. Dave proposed to have a fully programmable location for AUXS1 and AUXS2 CPU I/O map with a default at 530H and 388H. This is costly (4 registers and fast comparators) and very difficult to design at required speed: will slow down address range decode for I/O a lot affecting command to command parameters.
We suggest to have a fix address for these ports: 530H and 388H.
Two register bits (one per address) can disable the chip from answering to these I/O

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addresses.
If we are not sure where to place these ports, we can leave it as a metal option for future modification or have one more alternative for each, but the address should be fix for fast decode.
GR58:GR5B are no longer needed if this option is accepted. We'll need two bits to disable 530H and 388H address decode and eventually two other bits to select other two alternate I/O addresses. We should always decode 16 addresses: 530:53F and 388:397 (not 4 or 16)

4.6.2 WavePort R/W Buffer Location and Size

To simplify the h/w and reduce verification work-load , WavePort R/W Buffer Size should be fix: 32KB for each, enough for at least 180msec of operation -> 90msec for half buffer. Every 90msec the CPU will have to fill and/or empty half Audio Buffer (write or read respectively).
It is also possible to place the WavePort memory buffer in a fix memory location, common for both desktop and portable architectures. We could place it in Memory in the upper part (in high address area), just before the h/w cursor. If the h/w cursor takes the upper 16KB of the memory, we could use the next 64KB for the WavePort buffer.
Going down in memory, in Nordic we'd place the h/w icon in the next 16KB (only 4KB needed now... but leave some room for expansion) and the Half Frame Buffer for mono-chrome and color panels in the next 32KB and 96KB respectively.

Total:

96KB for CRT/TFT/SS STN panels,
128KB for monochrome panels and
192KB for dual scan color STN panels.

out of 1MB or 2MB memory available.
When the memory is expanded, all these fix components should move automatically in the upper side (towards the end of memory).

This places the WavePort buffer at:

- for **1MB** of memory by 32 (256Kx32 -> 00000:3FFFF) **3B000:3EFFF**
- for **2MB** of memory by 32 (512Kx32 -> 00000:7FFFF) **7B000:7EFFF**

If we adopt this solution, GR43 is not needed.

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4.6.3 On Host Access to WavePort Buffer

In order to ensure independence between the Graphics s/w Driver and the Audio Driver, taking into account AVGA limitation of no CPU accesses during BLT operation, Dave proposed a separate path for WavePort Host Accesses. This involves a separate 4 stage by 32bit write and read buffer and separate arbitration for the Audio cycles. The buffer is shared by WavePort read and write operations and an I/O to an extension register bit is needed in order to switch from a read operation to a write operation or vice-versa.
Dave also proposed that the host address be dependent on GR6 CPU address map bits such that the video and audio address maps don't overlap.
Please note that this approach prevents debug with a Hercules card when in graphics.

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In the following an alternate scheme is proposed:
- There is one register bit that enables WavePort memory write accesses and one register bit that enables WavePort memory read accesses. When one of these bits is asserted ,the chip expects only host accesses for the WavePort: the host address will be automatically translated to a memory address inside the WavePort buffer. The access will be fully linear, 32bit only, **graphics mode independent** (like in extended 8bit/pel). The Graphics block will be forced to this mode and all planes will be automatically enabled. On the Host side, the WavePort buffer will be placed always at A000:0000 - A000:FFFF -> 64KB with 32KB for read buffer (the upper side) and 32KB for write buffer (the lower side of this 64KB segment).
- The CPU Data Path is the same as for any other CPU cycle: no special FIFO, no special arbitration are required. The Audio Driver and The Graphics Driver communicate through interrupts: There is an interrupt for BLT completed (Dave's idea when presented with this proposal) and an interrupt for Audio Buffer Full (or Audio Transfer Completed). When the BLT is completed, if Audio is enabled on the chip, the BLT Completed interrupt allows the Audio Driver to check if there is any need to service the Audio and vice-versa.
If possible, the Graphics driver should restrict the extent of the BLT operations to less than 160msec or so (leaving at least 20msec to start filling the WavePort buffer).

- There is no on chip CPU WavePort address generation. The CPU address in the range A0000:AFFFF (incremented by 4 every cycle for DW accesses) is translated to physical memory address 3B000:3EFFF. If host side WavePort pointers are used, the host address is latched and translated for comparison with the Codec pointers generated on chip.

Adopting this scheme would greatly simplify the extent of the design and verification work for WavePort: 8 weeks at least will be saved.

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4.6.4 On the Audio Driver

Dave proposed that the Graphics Controller has h/w to compare the WavePort pointers and generate interrupts. The Codec pointers are I/O readable by the host as well as several buffer status bits (Audio-IN buffer Full, Audio-In buffer half-full, Audio-Out buffer half-empty, Audio-Out buffer empty,...).

Nordic-1M will support Dave's proposed interrupt driven interface.
In this case the only important difference for the driver will be that it will have to generate the buffers address and not rely on the h/w to do this (Dave suggests that CPU will write and read always the same address A000:0 or B000:0 and the actual address on the host side is generated on the chip - we sugest to change this and let CPU generate the address).

Because CPU has to wait untill the a BLT operation is complete and the BLT has to wait for Audio buffer to be full or the transfer completed, two more interrupts are needed: BLT operation completed and Audio transfer completed. This way the Audio Driver and the Video driver can communicate with each other.

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The Read and Write CPU side pointers will be generated by latching the last read and write WavePort CPU address (lower 16bits only) after translation to physical memory address. Comparators on the host and codec pointers will generate Buffer Full and Buffer Empty signals.

Jeff Ort drew our attention to the fact that the driver transfers a certain size block and needs an interrupt anytime half of what was placed in the Audio buffer was read by the Codec (the play-back buffer is half empty). To make things simple for the h/w, we propose to give Jeff an interrupt when the CODEC side playback buffer read pointer reached a pre-programmed value, value the driver programs everytime it transfers a block of a certain size in the playback buffer. For instance, if the driver put 2KB of data in the playback buffer starting from phisical address 3B000 (host address A000:0) and wants on interrupt when the first 1KB was read by the CODEC, it should program 3B0FF in the playback interrupt register, as 1KB = 256 32bit words. The register will have 16bits and the driver will program B0FF to get an interrupt when the CODEC reads 3B0FF or 7B0FF playback buffer address.

Similarly, on the record side, there will be a programable interrupt on the CODEC side to be used to tell the driver when the Record buffer is half full.
So we'll need two 16bit indexed registers for these programable interrupts. For each WavePort interrupt we also need a status bit to say that the interrupt happened, an enable bit to enable the particular interrupt. As Dave proposed, GR4D is the Interrupt Status register but bits [0] and [2] will be the programable interrupts status bits. The interrupts and the status bits will be cleared after this register is read (automatic clear in h/w).

We could use registers GR58:5B as high and low byte for the programable interrupt on Record and Play-back buffers respectively.

The write-buffer (or Audio-Out =the one in which the CPU writes) is empty one WavePort write cycle to memory after

WRBUF-Write-Pointer = WRBUF-Read-Pointer+1

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(this condition will activate set an empty flag).
The write-buffer is full one WavePort write cycle to memory after

WRBUF-Read-Pointer = WRBUF-Write-Pointer + 1

The same equations apply to the WavePort read-buffer, only this time the read-pointer is on the host side and the write-pointer on the Codec side.
Shouldn't be a Audio-Out buffer full interrupt and a status bit for it?

Threshold detect mechanism will require to increment host pointers, but the CPU is supposed to read this pointer and generate the proper address when going above the threshold. The idea of the threshold detector is that by incrementing the Audio-In read pointer everytime the write pinter is incremented if the Audio data is under the threshold value, the delta between the pointer remains the same and the buffer does not fill in with sub-threshold value. This was true if the half-full detection had been generated based on the delta between pointers. After talking to Dave, there are some clarifications to be made on the threshold detect mechanism for record:

For one record sesion, this is a one time event mechanism: if the threshold was passed once after being enabled, its effect is lost - even if the sound level goes below the threshold the record buffer read pointer works normally. The threshold will help only in the initial stage before the first actual voice pattern is detected, but it does not have any effect after the initial triggering event - once the sound leved passed once the threshold.

With this driver approach, GR43 and GR58:5B will not be needed.
Five registers are saved. Twenty One register are still needed (plus two reserved = 23).

Another possible approach for the driver uses extensively the Vertical Interrupt:
In this case every Vertical Interrupt, the Audio Driver reads the Codec side pointers, compares them with the Host side pointers, the driver generates based on the CPU address it last wrote to or read from and makes its own decisions. The driver will also check the BLT completed status bit.
In other words, every 18msec (@60Hz) , on the Vertical Interrupt the Audio driver can process data from the Codec pointers, calculate based on the last address if the WavePort buffer is full or empty and decide how many more WavePort accesses to execute. As at least 180msec worth of data is in a full Waveport Buffer, the driver has 6 opportunities to find out that the buffer is empty and start filling it before half WavePort buffer is empty. On chip h/w is still needed to stop sending data to the Codec after sending all data and to read all data from the WavePort read memory buffer on the host side. Because the CPU decides when the buffers are full, half full or empty there is no need for registers for the pointers on the CPU side, but the CPU address will still be latched to generate the host side pointers.
The "BLT operation completed" and the "Audio transfer completed" interrupts are needed anyway bacuse we share the data-path for BLT and CPU cycles.

By adopting this mechanism in the driver, no special h/w is needed to preserve pointers on the Host side, to compare the Host side pointers (read and write) with the Codec pointers and to generate interrupts and status bits. The only interrupts needed are Standard VGA Vertical Interrupt as a time base, BLT completed Interrupt and Audio Completed interrupt.

We can still implement the threshold detect.

GR44,GR45, GR48 and GR49 won't be needed.
Nine registers are saved. Seventeen register are still needed (19 with two reserved registers).

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Conclusion
The above proposal, if OK for the WavePort driver, would reduce significantly the amount of design and verification work on the WavePort. This document was written in order to get feed-back and reach an agreement ASAP. Our goal is to have a unique s/w model for the WavePort, but we'd like to cut the amount of work if possible.

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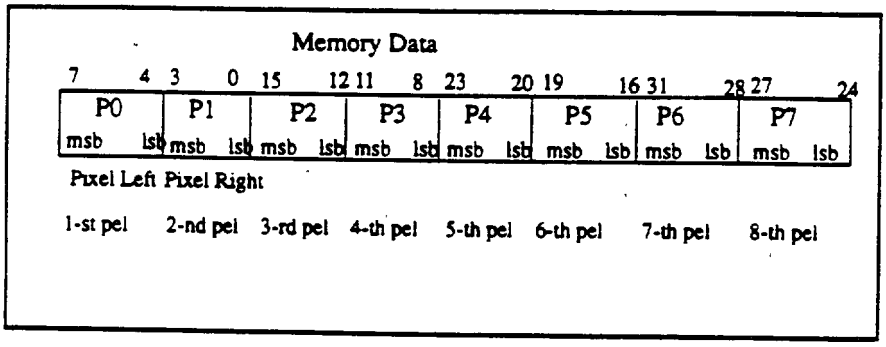
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4.7 Four Bit per Pel Packed Format

To fully support Windows Chicago, Nodric-1M should support 4bit/pel packed format. CPU will be able to write only 8bits or more at a time. To modify only 4bits the CPU will do read modify write and mask four bits (bring them from CPU latches).
The following picture shows the actual format:



In order to get Nordic-1M to support this mode, we need to place the VGA Video Data Path in 8bit per pixel mode with pixel doubling (mode 13) but disable the mechanism that concatenates adjaisant 4bits to make one 8bit pixel displayed twice (at a divided by two RAMDAC VCLK) and disable as well dividing by two the RAMDAC VCLK.

On the CPU side chain 4 address scrambling should be disabled and data should be shifted right like in extended 256 color modes.
In nordic-regs-rev9.lst we assigned SR26[0] to enable this graphics mode.

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4.8 Robin's Ideas on High Resolution Panels for Nordic-1M

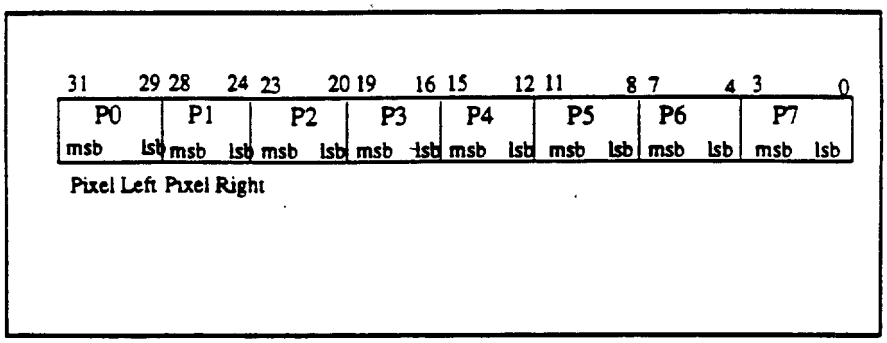
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Nordic's objective is to be able to center and fill the screen on 800x600 panels and to center an 800x600 picture on 1024x768 panels. The main focus is 800x600 panel support TFT and dual scan STN.
In TEXT there will be three options:

- horizontal and vertical centering with 9x16 fonts (disable 640x480 force to 8dots font)

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Nordic's objective is to be able to center and fill the screen on 800x600 panels and to center an 800x600 picture on 1024x768 panels. The main focus is 800x600 panel support TFT and dual scan STN.
In TEXT there will be three options:
- horizontal and vertical centering with 9x16 fonts (disable 640x480 force to 8dots font)
- auto-expand the font to fill the screen
- special font to fill the screen

In Graphics there will be tree options:
- horizontal and vertical centering
- use a driver to run at maximum resolution
- automatic expand to 800x600 (only if s/w verification shows it being OK).

In all cases horizontal and vertical options will be decoupled (different enable bits).

Here's a list of what needs to be done:
a. Expand horizontal and vertical centering capability from 640x480 to 1024x768.

b. Shadow all H/V CRTC registers except HDE and VDE.

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The vertical registers are shadowed now, but the horizontal registers are not.
We need to shadow CR0, 2, 3, 4 and 5. These registers will be written by the BIOS at POST.

c. Support 10dot character-clock and CRT-FIFO-Read / Shift/Load (Video-Serializer Load). Now only 8dot and 9dot character-clocks are supported. For smooth-scrolling the pel-pan has to be expanded to 10 pisitions (0:9).

d. TEXT auto-expand will be as follows:
- horizontal: replicate the last pixel once for 9 dots wide fonts and twice for 8 dots wide fonts.
- vertical: replicate all odd scan-lines

TABLE 3. Font Expansion for Different Panel Sizes

Font-Size/Panel-Size	480	600	768
8x14	8x19	10x21	10x21 + center
8x8 with scan-ln. doubling	8x19	10x24	10x24 + center
9x16	8x19	10x24	10x24 + center

Please note that in text vertical expansion is done on the scan-line counter as well as the vertical display line counter, but it does not affect the vertical non-display line counter.

e. Graphics modes expansion (to be implemented only after s/w verification)
Graphics expansion is less important as it is assumed that important applications will run at maximum panel resolution with a driver.
We'll need to supply drivers for many applications with high res. panels !!
Vertical expansion:
- 350lines -> replicate all odd scan-lines
- 400lines -> replicate all odd scan-lines
- 480 lines -> replicate every 4-th line

Horizontal:
- center
- duplicate every 4-th pixel
- duplicate every 4-th pixel with diagonal shift

(scan-line 0 -> 1st pel, scan-line 1 -> 2nd pel, scan-line 2 -> 3rd pel, scan-line 3 -> 4th pel).

5.0 Nordic-1M Pinout Specification 208 pin package:

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System Interface (reference is VESA VL bus): 73

(on BVDD)

DAT31:0
HIMEM (normally used as ADR24, but it can be used as ADR31 and leave 2GB of upper address space reserved for MPEG/JPEG boards)
ADR23:2
BE3n,BE2n,BE1n,BE0n
LADSn,LDEVn,RDYn
M/IOn, W/Rn
RESET, LCLK
RDYRTNn,
EBROMn/VADRn/AUXS2 (Enable BIOS ROM Buffers on all busses or Valid Address - CPU Address in Nordic valid address range I/O or memory or Auxiliary Select 2 to be used to select the Audio Synthesizer or some other audio chip)
INTR, CLK32K/OVRW, OSC/XVCLK (14.318MHz)
SUSPIn/BLIn/FCBLANKn, SBYIn/ACTIn/FCEVIDEOn
(32KHz clock input / FC Overlay Window Output controlled by VAFCPU, Supend Input/ Back-Light Input/VAFC BLANKn I/O signal controlled by VAFCPU - pin configuration -and FCESYNCn - FCBLANKn direction and HSYNC/VSYNC HI-Z or not;
Stand-by Input/Activity Input/VAFC External Video Control Input - controlls the direction of FCP[7:0]. Pin configuration controlled by VAFCPU).

Configurations: - VL/PCI/ISA bus, support/not BIOS, 8/16bit BIOS.
- Need a register bit to select SUSPEND Input or Back-Light Input. Default is SUSPEND Input.
- Need a register bit to select Stand-By Input or Activity Input. Default is Stand-By Input.
- SUSPIn, BLIn, SBYIn, ACTIn are level triggered, active L inputs. In Nordic there is no Suspend pin polarity bit as in T1 (SR8[4]).

Note: a.In PCI bus, Alpine used ADR17:2 as BIOSA15:0. We assume that all portable systems will use a motherboard video BIOS and do not support an adapter BIOS in PCI. We do support an adapter BIOS in VESA VL bus and ISA to facilitate demo board design.

b. EBROMn is active on all bus types: in ISA is generated on Address Decode and MEMRn, while in VL and PCI is unlatched address decode. In PCI bus the BIOS should be relocatable, an option we do not support. That is why we say that we do not support BIOS in PCI. We do support IOCHRDYn and RDYn/TRDYn for BIOS accesses too. All this logic should already be in 5428 (ISA and VL) and Alpine (PCI).

c. The 5428 Feature Connector pins are available in all buses. A register bit enables them early in the logic to save power when not in use.

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DRAM Interface (for assymetric, dual WEn 256Kx16 DRAM-s): 50
(on DVDD)

MA9:0
MD31:0
RAS0n,RAS1n,CASn/WEn, OEn
WE0n/CAS0n,WE1n/CAS1n,WE2n/CAS2n,WE3n/CAS3n

Configurations: symetric/assymetric DRAM, dual WEn/CASn

Note: a) For dual CASn DRAMs, the WE0n:WE3n pins become CAS0n:CAS3n, while CASn becomes WEn.
b) Two RAS-es are used for two banks.
c) OEn is not actually needed as we use early write.

Clock Synthesizers: 6
(MAVDD, MAVSS feed mclk clock synthesizer, VAVDD, VAVSS feed dclk clock synthesizer)

MAVSS, VAVSS, MAVDD, VAVDD,
MFILTER, VFILTER
(Can we design a clock synthesizer without an external filter?)

CRT Interface and RAMDAC related pins: 10
(DAVDD, DAVSS feed all RAMDAC custom layout)

R,G,B (analog)
IRef, DCVDD1, DCVDD2, DCVSS1, DCVSS2
HSYNC , VSYNC TO (these two pins are on BVDD)

FLAT PANEL and Power Management Interface (on PVDD): 31

R7/FCP[3], R6/FCP[2], R5:0, G7/SUSPSTn/FCP[1]
G6/SBYSTn/FCP[0], G5:0, B7/MOD, B6/FCVCLK, B5:0
(use slow edge pads and stagger them modulo 4)
FPVDCLK, LLCLK, LFS, FPDE, (use slow edge output pads)
FPVCC, FPBL, FPVEE

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Notes:

b. R7:6, G7:6, B7:6 (24 bit TFT panel extra video data out pins)
c. We need also bits for SUSPST and STANDBYST, PANEL-ON/OFF, PANEL-IN-POWER-UP-or-DOWN.
d. We assume that the 24bit TFT panels do not need external MOD.

e. No NPD pin.

f. FCP[3:0] pins are I/O-s whose direction is controlled by FCEVIDEOn in VAFC configuration. FCVCLK is the clock that clocks them in and which should be used to clock them while they are displayed or at least to resynchronize them before being latched on the internal clock. FCVCLK is always an input when in VAFC configuration.

g. Nordic-1M facilitates NTSC output by providing RGB 6:6:6 just before DAC on the R5:0, G5:0, B5:0 when in a special mode. It also provides odd/even frame signal and true Display Enable in sync with the RGB. Nordic-1M will run in terlaced mode when in NTSC Out mode. All the needed signals will be comming out on the Flat Panel Pins in the NTSC Out mode.

Audio Port (on ADVDD): 6

SDO (SErial Data Output to CODEC pin SDIN)
SDI (Serial Data input from Codec pin SDOUT)
FSYNC (Frame Sync Output)
SDCLK (Serial Data Clock I/O)
D/Cn/AUXS1 (Data/Control Select Output or CS4231S Chip Select for the ISA bus)
PDN (Power Down Output)
Note: These pins can be used as extensions for 24 bit TFT panels, in which case the chip does not support the audio port. **Note also that CS4215 has Resetn pin.**

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Miscellaneous Pins: 10

Following pins on MVDD:

TRWn	I	(Test Latch Load Enable, active L - for pinscan & test mode)
SW2	I	(Switch #2 or reserved for SDRAM support in the future)
SW1/MCLK/XMCLK	I/O with PD controlled by XReset	(Switch #1 or mclk driver buffered output for tesing and debug or external mclk for testing; a special register bit disables this output in normal operation for power savings. Default: Input on which either SW2 or XMCLK comes in. Only if the special register bit is set, this input becomes output and outputs MCLK from the clock synthesizer for testing. The special register bit defaults 0 = the pin is configured as Input. Please note that a h/w configuration PU/PD controlls if the actual internal mclk comes from an internal or external source, but this PU/PD does not control if

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SW2/MCLK/XMCLK is an input or an output.)

RES4CKE O NC Pin Reserved for Future Nordic chips

Following Pins on BVDD:

SW0/VCLK/FCDCLK I/O (Switch #0 Input or vclk driver buffered output for testing and debug, or VAFC Dot-Clock Out ; Default for this pin is Input on which SW#0 is applied. VCLK and FCDCLK is the same signal, the name is diferent to ease reference to VAFC spec)

Following Pins on PVDD:

FCP[7:4] I/O Feature Connector Data Pins bits 7 to 4. The other Feature Connector pins are shared with some panel or host bus pins.

FCESYNCn/RES4SDCLK I 5428 Feature Connector ESYNCn pin - controlls the direction of FCBLANKn and its effect and tri-states HSYNC and VSYNC.

System/Bus Interface Signal Mapping

(See 54xx Reference Manual for Feature Connector Pins Description: FCyyyy)

TABLE 4. VESA-VL <-> PCI bus <-> ISA bus Pin Mapping

VESA-VL	Intel-PCI	ISA
HIMEM	--	--
ADR23:16	--	LA23:16
ADR15:9	--	SA15:9
ADR8	PAR	SA8
ADR7	STOPn	SA7
ADR6:2	--	SA6:2
BE3n	C/BEn3	SA1
BE2n	C/BEn2	SA0
BE1n	C/BEn1	SBHEn
BE0n	C/BEn0	RFRSHn
DAT31:22	AD31:22	--
DAT21:19	AD21:19	--
DAT18	AD18	MWRn
DAT17	AD17	IOCS16n
DAT16	AD16	IRQ
DAT15:0	AD15:0	SD15:0
RESET	RESET	RESETDRV ??
LADSn	FRAMEn	BALE
LDEVn	DEVSELn	MCS16n
RDYRTNn	IRDYn	AEN

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TABLE 4. VESA-VL <-> PCI bus <-> ISA bus Pin Mapping

VESA-VL	Intel-PCI	ISA
W/Rn	IDSELn	IORn
M/IOn	--	MRDn
LCLK	CLK	IOWn
RDYn	TRDYn	IOCHRDY
EBROMn/VADRn	VADRn	EROMn/VADRn
INTR	INTR	ZEROn

Notes: 1. SW2, SW1/MCLK/XMCLK and SW0/VCLK pins are normally used by the BIOS as panel type switches readable on SR24[2:0].

2. XMCLK and XVCLK (on OSC/XVCLK) are needed for manufacturing test of the chip. When they are used, SR24[1:0] will wiggle at clock rate and they should be masked on the tester.

3. MCLK and VCLK are needed for manufacturing test of the clock synthesizer and for chip debug.

Digital, Mixed Voltage Power Pins: 22

BVDD1, BVDD2, FPVDD1, FPVDD2, MVDD1, MVDD2, ADVDD, CVDD1:4, (BVDD goes now to HSYNC and VSYNC)
VSS1:11

Total Pins Used: 208 (with no pin left).

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Pinout Modifications in rev. 3.8 relative to rev. 3.7 09/11/93

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1. Took-out Whisper Support Pins: WWRn, WRdn, WAD[3:0], FPCn.

2. Reduced the number of CPU Address Pins: ADR[24:27] went-away. Use HIMEM to place the chip outside 16MB of memory for linear addresing.

3. Killed CRTVDD and placed CRT Interface on Host Bus VDD.

4. Introduced VAFC pins in a unique pinout configuration in both VESA VL and PCI.
Added VAFCPU a pull-up to enable VAFC (VESA Advanced Feature Connector).
ADR[27:24] VAFC pins, and R[7:4], G[7:6], EROMn/VADRn, SUSPI/BLI, SBYI/ACTI get a configuration for VAFC -> total 14 pins.
SW0/VCLK will be used as VAFC VCLK, losing SW0 pin as panel type when VAFCPU is used.
In PCI bus, no ADR pin will be shared with VAFC.
ASW0PU (Alternate Switch 0) will be added on MD pins to replace SW0 pin when VAFC is enabled by VAFCPU. ASW0PU will read-back in the same register bit as SW0.

so the BIOS will not feel any modification in the reporting scheme. The chip will draw more power in suspend with VAFC.

5. Moved SW2. SW1/MCLK/XMCLK the two reserved pins (one obtained by killing CRTVDD)and TRWn on MVDD to prepare for SDRAM pin compatible option in the next Nordic that supports SDRAMs. Marked them as "reserved for SDRAM pin name". It looks that TRWn will not be needed, but it was moved on MVDD so that in case it is needed, it is available (in this case we'll need an extra switch for SDRAM support or at least to disable TRWn test mode effect).

6. Rearanged VAFC pins as pins R4 and R5 were used by VAFC - an error.

Configuring Nordic-1M

If Terminator used specially assigned pins to configure the chip, **Nordic-1M will use some of the MD31:0 pins sampled on the Reset trailing edge,** similar to Mustang. The pad cells will have an active pull-down controlled by an **extended Reset** signal. The pull-down resistence will be about 75KOhm. An external pull-up less than 60KOhm is needed only if the option is used. In Suspend, the MD pads are inputs and the DRAM OEn is H so no DC current is drawn by the configuration h/w. An external resistor is needed only if the configuration pin has to be H at Reset.
All h/w configuration latches are read accessible via I/O. The h/w configuration is latched on Reset trailing edge. (these latches were r/w, with s/w PU read, having only read is enough).
We'll define the configuration pins to minimize the number of external resistors:

CPU Bus Configuration:

On MD18:16 &	-> no external PU	= 32bits VESA VL bus at 33MHz or less bus clock
& MD23	-> MD16 PU	= 32bits PCI bus with Burst PU called "PCIPU"
	-> MD17 PU	= 16bits ISA bus PU called "ISAPU"
	-> MD18PU	= 32BIT VESA VL BUS AT 50MHZ BUS CLOCK PU called "FVLPU
	-> MD23 PU	= 32bits PCI bus no Burst PU called "PCINBPU" This is a reserved configuration in case burst does not work on a PCI bus.

Reads-back in SR22:

PCIPU on MD16 -> SR22[0]
ISAPU on MD17 -> SR22[1]
FVLPU on MD18 -> SR22[2]
PCINBPU on MD23 -> SR22[7]

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Clock Configuration:

On MD19 (reads back on SR22[3])
-> no external PU = internal MCLK and VCLK clocks, from the internal clock synthesizer
-> MD19 PU = use external clocks from SW1/MCLK/XMCLK and OSC/XVCLK
PU called"XCLKPU"

This PU is used for manufacturing test.

One reg. bit is needed if internal clock is selected to control outputing mclk on the MCLK/XMCLK pin = 1 if use internal clock then output it on SW1/MCLK/XMCLK pin. -> SR23[0] is this bit.

Memory Configuration: SRF[0]
No Pins, Use Two Register Bits -> 2CAS/2WE bit=H 2WE, bit=L 2CAS (default =L)
-> Symetric/Asymetric bit=H Asym., bit=L Sym. (default=L)

BIOS Support: (reads-back on SR22[6] for BIOS8PU)

Nordic-1M supports 16bit or 8bit BIOS and only in ISA bus configurations.
The BIOS is always supported when in ISA.

On MD22 -> no external PU = 16bit BIOS
-> external PU = 8bit BIOS (no MEMCS16n decode on C000)
This option is mostly for debug in case 16 bit BIOS range decode is not fast enough.
If the BIOS support is disabled, this configuration is don't care. Called "BIOS8PU".
Please note that Nordic-1M supports C000 BIOS only in ISA.

In a normal note-book the BIOS is at E000:0, not supported by Nordic; so no external component is needed.

Sleep Address Selection:

On MD21: Sleep Address Selection (reads-back on SR22[5]).
-> No external PU = sleep at 3C3[0] - to be used when Nordic is on the Mother-board (most cases)
-> External PU = sleep at 46E8[3] - to be used when Nordic is an adapter (like a PCMCIA card and/or an adapter to turn desktop into an environment friendly PC) Called: S46PU

Note that Nordic-1M comes-up awake, though this has to be cleared with the BIOS group.

Feature Connector Configuration: (reads-back on SR24[7])
On MD25:

-> No external PU = no Feature Connector Support: outputs used only for FC are forced L. I/O are forced inputs, I/O and inputs are forced on the chip so that they do not take power if not connected externally.

-> External PU = All pins needed for FC including OVRW are active.
Called: VAFCPU

On MD26: Alternate SW0 Selection (Reads-back on SR24[0] when SR24[7] is 1)
When SR24[7] is 1, SW0 pin is forced to output DCLK and this external PU latched on Reset trailing edge plays as SW0. It reads back at the same bit as SW0 does.

-> No external PU = SW0 reads back 0 in SR24[0]

-> External Pu: SW0 reads back 1 in SR24[0].

Total: 10 H/W PU configuration options.
In normal operation with FC enabled up to three external PU-s may be needed (bus type if not VL and FC).
In normal operation with FC disabled up to one external PU-s may be needed (bus type if not VL and FC)

Summary of PU/PD Configuration Pins and Register Bits where they can be read-back:

SR22 [7:0] H/W Configuration Read Register #1

Read only register, written on reset training edge by activating PU/PD on MDi pins. The PD-s are inside the pads active only during XReset (extended reset).

[7] 32bits PCI bus no Burst h/w PU configuration on MD23. It is called "PCINBPU" (read only bit).
This is a reserved configuration in case burst does not work on a PCI bus.

[6] Select 8 bit BIOS support (if 1). Otherwise 16 bit BIOS support if the BIOS support is at all enabled. PU on MD22.

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[5] Resereved for Sleep Address Select: reads back S46PU (MD21).
1 = I/O address 46E8[3] as sleep address (needs external PU).
0 = I/O address 03C3[0] as sleep address (no external PU is needed).

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[4] Reserved

[3] Select external clocks: MCLK and VCLK on SW1/MCLK/XMCLK and OSC/XVCLK. (default: internal clock synthesizer, SW1 and OSC).

PU on XCLKPU on MD19.

0 = internal clocks with the pins used as inputs for panel type switch #1 and OSC. If SR23[4] and SR23[0] are 1, SW0/VCLK and SW1/MCLK/XMCLK, respectively become VCLK and MCLK outputs respectively, for test purposes (only if SR22[3]=0 MCLK can be seen, but VCLK can be seen even if SR22[3]=1 as long as SR23[4]=1)

1= SW1/MCLK/XMCLK and OSC/XVCLK become XMCLK and XVCLK inputs generating directly chip MCLK and VCLK without clock synthesizer. The clock synthesizers are powered down if SR22[3]=1.

[2] Select VESA VL Bus at 50MHz
1 = VESA VL bus at 50MHz selected (needs external PU on MD18)
0 = VESA VL bus at 50MHz not selected

[1] Select ISA Bus with PU on MD17.
1 = ISA bus selected (PU on MD17)
0 = ISA bus not selected (no PU on MD17)

[0] Select 32bit PCI Bus with PU on MD16.
1 = 32bit PCI bus selected (PU on MD16)
0 = 32 bit PCI bus not selected (no PU on MD16)

If [1:0] = 00 (i.e. no external PU on MD17:MD16) 32bit VESA VL bus is selected. No more than one PU on MD17:MD16 should be used.

Note: In AVGA3, CF14 is "Enable Local BUs Address Latching Interface". Alpine does not have this configuration bit. We need to do what was done in Alpine to get rid of this Configuration Pull-up/Pull-Down option. *CAN we? WAs this done, Dwarka?*

SR24 Panel Type Switches Register

[7] VAFCPU (VESA Advanced Feature Connector External Pull-up) Read-back. If external pull-up (the bit read-back 1) then all VAFC pins are configured for Video Port. Otherwise they have other functions or are disabled if no other function. (Disabled= the inputs are foced = the TTL and CMOST threshold controls are off & the outputs are tri-stated. It actually reads back what is latched on Reset on VAFCPU. VAFCPU is on MD25.

[2:0] SW2:0 pins read back (read only bits) Please note that bit [0] reads back SW0 if VAFCPU (SR25[2]) is 0 and ASW0PU if VAFCPU is 1.ASW0PU is on MD26.

Configuration Register Bits needed:

Symetric/Asymetric DRAM -> SR8[7] in T1, CF13 in AVGA3
=> SRF[1] 0 = Symetric DRAM Default: 0
1 = Assymetric DRAM

This bit is read only in AVGA3 (reads back CF9), but it is writable in T1. It controlls MCLK frequency as an alternate to SR1F. We will use only SR1F to program MCLK frequency in Nordic. The default MCLK frequency will be 39.374MHz, corresponding to SR1F[5:0] = 18H=22D. This frequency fully meets the spec for -80 256Kx16 DRAM-s.

Two CAS or two WE DRAM -> pin 72 in T1, CF12 in AVGA3
=> SRF[0] 0 = 2 WE DRAM (Default:0)
1 = 2 CAS DRAM

16 or 32bit wide Video Memory (One or Two 256Kx16 DRAM-s or SDRAM-s)
-> not in T1, SRF[4:3] in AVGA3 (01=16bit, 10=32bit)
=> SRF[7,4:3] will be used in Nordic with the same encoding as in AVGA3. (11 is reserved for 64bit wide). Default: 10 (32bit). See Table next page. Please note that we have room to add other types of DRAM-s (SDRAM-s for instance).

In AVGA3 SR8[0] is "CS OUt to EEPROM" a feature Nordic does not Support. Nordic will not change the meaning of AVGA3 bits unless they are read only (like the pins or external PU read back).

SR8[2:0] are in T1 the read-back bits for SW2:0 input pins, but AVGA3 uses them for EEROM programming so we moved SW2:0 read back to SR24[2:0].

In T1 SR8[7] is symmetric/assymetric addressing... in Nordic this is SRF[1].

Two or one Bank 32bit wide DRAM

-> not in T1, SRF[7,4:3] in AVGA3 (00=8bit, 01=16bit, 10=32bit, 11=64bit, SRF[7] controls if 2MB of Video memory are available with 4x512kx8 -0- or with 4 256Kx16 DRAM-s, twoi banks -1-). *It seems that in AVGA3 to support 1MB with two 256Kx16 dram-s and 32bit wide bus, we select 32bit wide and SRF[7]... but I do not exactly know how this configuration is selected.*

=> SRF[7,4:3] in Nordic, will select the Video Memory Configuration slightly differently than in AVGA3 and Alpine. See the following table.

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	SRF[7]	SRF[4]	SRF[3]	Memory Configuration
new	0	0	0	32bit, 2MB=4x512Kx8
	0	0	1	16bit, 512KB=1x256Kx16
	0	1	0	32bit, 1MB=2x256Kx16 (default)
	0	1	1	Reserved (64bit in Alpine)
new ?	1	0	0	32bit, 2MB=4x256Kx16, Two Banks
	1	0	1	Reserved

1	1	0	Reserved
1	1	1	Reserved

DRAM Timing select (short RAS or long RAS)
-> SRF[2] in T1 and AVGA3
=> SRF[2] in Nordic, default 1 = short RAS (3.5 L, 2.5H)

BIOS 48KB or 32KB -> not in T1; CF8 in AVGA3. In T1 SR8[4] is Suspend pin polarity. In Nordic Suspend pin is always active L (0 on pin puts the chip in Suspend).
=> SR23[2] in Nordic =0 32KB BIOS (default=0) C0000:C7FFF
=1 48KB BIOS : C0000:CCFFF
The initial BIOS code should be placed in the first 32KB starting at address C0000.

BIOS ROM ZERO* wait select in ISA and fast timing in VL bus
-> not in T1; CF1 in AVGA3
=> SR23[1] in Nordic =0 no ZERO wait state for BIOS in ISA and slow, safe BIOS timing in VESA VL and PCI.
=1 ZERO wait state for BIOS in ISA, 8MHz bus

Output internal VCLK on VCLK/XVCLK pin -> not in T1 or AVGA3
=> SR23[4] in Nordic =0 if SR22[7]=0, then VCLK/XVCLK is an output pin forced L
=1 if SR22[7]=0, then VCLK/XVCLK is an output pin and it outputs VCLK.

Output internal MCLK on MCLK/XMCLK pin -> not in T1 or AVGA3.
=> SR23[0] =0 (default) force L on the pin
=1 output mclk

SuspendI/BLI bit -> not in T1 or AVGA3.
=> SR23[5] in Nordic, 0= Suspend pin in Suspend/BLI pin (default)
1= BLI pin on Suspend/BLI pin

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SBY/ACTI bit. -> not in T1 or AVGA3
=> SR23[6] in Nordic, 0= SBY on SBY/ACTI pin (default)
1= ACTI on SBY/ACTI pin

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Video Port Enable bit active in PCI bus -> not in T1 or AVGA3.
(read only bit, actually reflecting the status of an external configuration PU: FCPU on MD25 latched at RESET or under S/W Control)
=> SR24[7] 0= Video Port Disable at pins to save power: inputs are forced.

outputs are L. I/O-s are inputs forced H in case they are not connected in the system.
If any shared pins, they are not in Feature Connector configuration.
1= Video Port Enabled at pins. If any shared pins, they are now in Feature Connector Configuration.

Live Video Enable bit -> not in T1 or AVGA3.
=> SR24[6] 0= disable (default)
1= enable

Audio In (from CS4215 to Nordic) Enable bit -> not in T1 or AVGA3.
=> SR24[5] 0= disable (force inputs inactive and outputs L disable AI-FIFO and cycles)
1= enable

Audio Out (from Nordic to CS4215) Enable bit. -> not in T1 or AVGA3
=> SR24[6] 0= disable (as above but AO-FIFO)
1= enable

Panel Type Switch Read-back -> SR8[2:0] in T1 or SR7[6:4], not in AVGA3
=> SR24[2:0] in Nordic, read only, writable on Reset or under S/W Control (SR24[3])
When SR24[3] whose default is 0, transits from 1 to 0 SW2:0 pin value is latched into SR24[2:0 which cannot be written by I/O.

Cross Talk Reduction Enable -> not in T1 or AVGA3.
-> SR24[3] =0 disable (default)
=1 enable - the pinout is configured to support cross talk reduction chip. The I/O registers for the cross talk reduction chip are always decoded, to make things simple. Reserve SRFX for this purpose.

Please note that **R9x[1:0]** TFT Panel type field of T1 was expanded to support 24bit TFT panels:

00 -> 9bit (333) (as in T1)
10 -> 12bit (444) (as in T1)

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01 -> 18bit (666) [was x1 in T1 covering both 01 and 10 !!]
11 -> 24bit (888) -> new in Nordic

Notes:

a. If 24bit TFT panel is selected, all related pins will be configured for it and it has priority over panel pins configuration settings for cross talk reduction enabled.
b. If 24bit TFT is not selected then MOD is slected on MOD/B7 pin.
c. If STN Panels Cross Talk Reduction support is selected, and TFT type is not 24bits. then the Cross Talk Reduction support pin configuration is selected.
d. If 24bit TFT is not selected, then SUSPST is selected on G7/SUSPST and SBYST is selected on G6/SBYST and MOD is selected on MOD/B7.

Other Register Related Topics
(See nordic-regs-rev#.lst where # is the latest one)

BIOS SCratch Registers #5 and #6 (2 extra required) (r/w)

SR28:SR29[7:0] are scratch registers.
Note that SR9, SRA, SR14 and SR15 are AVGA3 scratch registers which we keep in Nordic. Also there are 13 18 bit scratch registers in the RAMDAC is SR12[1]=1.

R9x - TFT Panel Data Format

[7:5] Reserved

[4:2] Select a 0 to 7 shift-clock delay from the internal character clock counter (8 VCLK/Character Clock) to TFT panel HSYNC (LLCLK) signal -> as in T1.

[1:0] TFT Panel Type:

00 -> 9bit (333) (as in T1)

10 -> 12bit (444) (as in T1)

01 -> 18bit (666) [was x1 in T1 covering both 01 and 10 !!]

11 -> 24bit (888) -> new in Nordic

Registers that are Moved Relative to T1

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CR1B[7,4,3,2] (R1B in schematics):

[7] Disable Text Cursor Blink in T1. Do we use this feature in T1?
Enable Blank End Extensions in AVGA3
[4] PCLKO (Panel Clock) no divide by two control in T1.
I am not sure this bit is actually needed in Nordic.
[3] IRQ Every Frame or Every Other Frame ? Is this bit used inT1?
[2] Not Used at All in T1.

I think that all these bits are not actually used. Are they needed ? -> Robin.

CR1C[7:0] & CR1D[7:0]

Are important LCD and Power Management Registers in T1 and Overlay Registers in Alpine. These registers are not in AVGA3, but because they are used in Alpine we may move them to **CR2C[7:0] and CR2D[7:0]**, which requires one more CRTC Index Register Bit. So:

CR1C -> CR2C & CR1D -> CR2D in Nordic relative to T1.

SRF[7]

In T1 is CRT Refresh Disable. This bit gates /FB/RWC[5] in FB sheet 6. In AVGA3 is DRAM Two Bank Configuration select bit.
I don't think that this bit is used in T1 ? -> Robin.

SR16

In T1 is used to control the pads for power and threshold. In AVGA3 is not used. In Alpine is CRT FIFO demand threshold and other things ([4:0] are used).

Move SR16 bits of T1 to SR20 to avoid contention with Alpine. Increase SRX Sequencer Register Index to 6 bits.

SR1A

In T1 is used as Test register. In AVGA3 and Alpine is Signature Generator Result Hi.
Move T1 SR1A bits to SR21 if it is not replaced by a similar register in AVGA3.

Nordic Revision and Mask Codes

Nordic Revision: ??
Nordic Mask Code: 00

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-----$$$$-----

```
User name:    SHAW (11)                    Queue:  UIDESK/UNIX_UIMKGT
File name:                                 Server: CLFPCD010
Directory:
Description: NORDIC27.
             December 21, 1998                              5:29pm
```

EXHIBIT
RX-579

```
 SSS  H   H   A   W   W
S   S H   H  A A  W   W
S     H   H A   A W   W
 SSS  HHHHH A   A W W W
    S H   H AAAAA W W W
S   S H   H A   A WW WW
 SSS  H   H A   A W   W


L      SSS  TTTTT
L     S   S   T
L     S       T    : :
L      SSS    T    : :
L         S   T
L     S   S   T    : :
LLLLL  SSS    T    : :
```

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NORDIC-1M Design Specification

by Vlad Bril, Robin Han, Sasha Eglit, Rakesh Bindlish, Dwarka Partani.
Jeff Ort
rev.5.0 December 21, 1998

1.0 Introduction & Table of Contents

Nordic is Cirrus Logic's Fourth Generation Flat Panel VGA Controller to be marketted in first half of 1994.
Nordic-1M is a mid-end member of the Nordic family. It is a GUI Accellerator with PCI support and Multi-Media Features.
Nordic-1M is targetted for the mid to high end of the **Note-book Computer Market** and for for the energy efficient **desk-top computers mother-boards**.
Nordic-1M is **not** targetted to the adapter market.

1.1 Table of Contents

This Specification will address the following:

1. Introduction and Table of Contents
2. Basic Feature Set
3. Detailed List of Features
4. Pinout and Pin Description
5. Architecture Specification
6. Register Specification - this is a diferent document
7. Product Implementation Plan - this is also a diferent document

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2.0 Nordic-1M Basic Feature Set

1. **Flat Panel VGA Compatible GUI Accellerator register and feature compatible to 5428 and Alpine I A/V. Priority: A (= highest).**
2. **32bit CPU, 32bit Video Memory, 32bit BLT and 32bit CPU to Video Memory Data Path. Priority: A (= highest).**
3. **208 pin QFP package.**
4. **Targeted to sample CY Q1'94, production CY Q2 '94. Priority: A (= highest).**
5. **Target cost: $12 to $10 -> less than 400mil [/] in C8 Foster City.**

6. **Multimedia Features**

- Part of a well defined **System Solution** for high performance **CD-ROM video and audio playback** for the portable market. **Priority: B**
- Part of a well defined **System Solution** for mid performance **low cost live NTSC Video and Audio with the NTSC decoder on a PCMCIA card. Priority: B**
- ~~**Audio Port to Display Memory**: Audio Buffer to Serial Interface for CS4248 Audio Codec. **Priority: C** (CS4215 is not fit for notebook computers).~~
- **Video Playback decompression accelleration for CinePak** including Color Space Conversion (YUV -> RGB). **Priority: B**
- **Live Video in a 320x240 or 640x480 Window** from a proprietaryly compressed TV decoded data source (at 30Hz) on TFT color panels. Data is stored compressed and it is decompressed to 18bit/pel or 24bit/pel in real time at display time. NTSC decoder and data compressor is on the PCMCIA card or the PCMCIA controller. Please note that due to live video bandwidth requirements on PCMCIA bus , a relatively non-expensive way to achieve the second feature is to implement this compression algorithm. **Priority: B**
- Color Key Live Video Overlay based on a 5428-like Feature Connector with PCI bus (only).

7. **Integrated in Nordic 1-M**

- Color Space Converter for CinePak. **Priority: B**
- 18bit DAC with direct color capability **Priority: A**
- *24bit RAMDAC with true color capability* **Priority: C**
- Clock Synthesizers for Video and Memory Clock (65MHz/3V, 110MHz/4.5V). **Priority: A**

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- DAC IRef Current Source on chip. **Priority: C.** *Boyd and ManShek are working on it.*

8. **Direct Bus Interface**:

- 32bit VESA-VL bus (and 486 local bus) **Priority: A**
- 32bit PCI bus. No on chip BIOS ROM support in PCI. **Priority:** A
- 16bit ISA bus for demonstration and easy system validation. **Priority: B**
- 32K or 48KB BIOS ROM support in ISA and VESA VL bus. **Priority: B** (only for BIOS/ system debug)
- At least 5 scratch pad registers: optimum 8 scratch pad registers. **Priority: A.**

9. **Performance Enhancements** to achieve 15-20MWinmarks at 1Kx768 8b/pel:

- 32bit BitBLT with memory mapped I/O BitBLT registers (as in 5428 ?or Alpine) Priority:A
- BLT buffer of 8 (~~or 16~~) bytes for Source (and Destination ?) data. (5428 buffer is 8bytes. Alpine is 16bytes) (as 5428)
- *X/Y offset for Pattern BLT (as in Alpine)* **Priority:** C
- h/w graphic cursor 64x64 (as in 5428)
- color expansion (as in 5428)
- linear memory addressing (as in 5428)
- 4 stage 32bit wide write buffer and capability to page CPU cycles if accumulated in the write buffer (this is already in 5428)

10. **Display Memory:**

- *0.5MB (16bit wide)*, 1MB or 2MB memory addressing 32bit wide (as in 5428)
- *1 or* 2 256Kx16 one bank or 4 256Kx16 two banks (2 CAS symetric, 2 WE asymetric) (as in 5428)
- maximum memory clock frequency: 50MHz/3V, 65MHz/4.5V **Priority: C**

11.**Flat Panel Support**: **[Priority: A]**

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- Color TFT (24bit, 18bit, 12bit, 9bit)
- Color Dual Scan and *Single Scan STN* (16 and 8 bit, including dual clock panels)
- Monochrome TFT (8bit).
- Monochrome Dual Scan STN (8bit).
- Monochrome Single Scan (4 and 8bit) support

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- Simulscan with all Fast Panels (6.3MHz or equivalent) with 32bit wide memory.
  No simulscan with 16bit wide memory with dual scan color panels.
  No simulscan for 3MHz monochrome dual scan panels.
- 640x480 single and dual scan support (Priority:A)
- 800x600 TFT *and no single and dual mono and color STN panel support (Priority: C)*
- 1024x768 TFT *and no single and dual scan STN panel support. (Priority: D)*

12.Display Features

- High quality monochrome and color shading, at least as good as 6440. Priority: A
- Shading option for fast panels. Priority: B
- Up to 8, 64x64 Hardware Icons independently mapped color+transparent background. **Priority: C**
- *Whisper Cross-Talk Reduction (If panels will be available in the time frame and if we can accomodate it with the shading algorithm).* ***Priority: C***
- ***"Office Productivity Booster Dual Display"*** 640x480 (panel) & 640x480 (CRT) 4 or 8b/pel or 640x480 (panel) & 1024x768 (CRT) 4 or 8b/pel ***Priority: E***
- Vertical Expansion in text and graphics (as in 6235 or 6440)
- Automatic Centering if not expanded (as in 6235)
- *Grey-Shades Maping options ?? Is this needed ? Priority: D*
- Text Contrast Enhancement options. (as in 6235 or 6440)
- *Inking Plane ?? Priority: D*
- *180 and 90 degree image rotation ?? Priority: D*
- *12 and 16dots wide font support ?? Priority: D*
- *h/w offset on h/w cursor ?? Priority: D*

13.Resolutions Supported:

- the same as 5428 at 5V (4.5Vmin)
- up-to 45MHz dotclk (1024x768, 60Hz interlaced) at 3.3V

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14.Power Management

- Mixed 3.3V and 5V operation: memory, host and flat panel independent VDD
- Green-PC spec support. **Priority: B**
- Stand-by Mode with internal stand-by timer (as in 6235)

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- Suspend Mode I/O or pin in all modes (LCD, CRT,Simulscan)
- *Light Sleep ?? - better not for this chip as it requires too much h/w. Priority: F*
- Panel Power Sequencing: automatic or under I/O control (as in 6235)
- Reduced Active Power in Panel Only Operation: < 60mAmp @3.3V. **Priority:A**
- Reduced Suspend Current: < 0.5mAmp. **Priority: A**

2.1 Inputs from the Nordic-1M Features Meeting of 09/10/93

- 24bit DAC if not too expensive (VAR)
- mclk @5V max 65MHz, @3V max 50MHz
- vclk and fpvdclk @5V max 85MHz, @3V max 65MHz
- **panels:**
  - TFT 1280x1024? ##, **1kx768 ##, 800x600 ##**, 640x480
    24bit,18bit, 12bit, 9bit color, 6bit mono
    NEC analog output? ##
  - STN 800x600 dual scan color, 640x480 ds color 16bit
    640x480 ss color 8bit
    640x480 mono bit 8bit and 4bit
  - horiz ## and vertical centering
  - normal 9dot font in 800x600 text ##
  - simulscan for 800x600 and 1kx768 panels ## (need to run all modes at 800x600 or 1024x768 rezolutions -> option to clock panel till h&v Blank)
  - support for two alternate fonts 10x24 for 800x600 (10x18 actual with spacing) and 12x25 for 1kx768 ## difficult !!
  - h&v text expansion in 800x600 and 1kx768 panels ## ?
  - color text enhancement ## : bright white instead of white
  - *on chip cross-talk reduction ##* ? - any improvement ?
  - *shading look-up tables ##* ? - only if not too large
- ***NO Whisper support even on the bus side - out !***
- ***NO one 256Kx16 DRAM support - out !***
- **h/w icon support:** with h/w cursor, up to 4 simultaneously. Horizontal position controlled in increments of 64 pixels.
  Icon attributes: off/on, 4 colors/3colors + transparent, no_blink/blink, (simple/double).
  H/W cursor goes over the h/w icon (visually). Uses independenly mapped color in RAMDAC RAM. Start at scan-line 64.
- PC98 integration? ## - to be negotiated
- reserve pins for SDRAM-s and CDRAM-s ##
- *NO true dual display*!

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2.2 Inputs from Compaq 09/10/93

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- 50MHz 486DX bus
- 75Hz refresh rate
- **need one 256Kx16 support with Audio and some video for Contura - build one motherboard for Contura and LT Lite. Two DRAM-s only on LT Lite.**

- think that 8KB/buffer of audio buffer is not enough
- want to use Analog Devices for Audio
- No clear winner on conpression. They are watching. Need Indeo driver.
- Play-back zoom is required. At least pixel replication.
- Very interested in Compressed Live Video. WAnt to talk more.
- need h/w icon 64x64 with 3col+transparency or 4 color, with pixel replication to 128x128.

2.3 Inputs from AST 09/15/93

- They prefer horizontal icon

2.4 New Features as of 10/04/93

- 4bit/pel packed support for Windows Chicago
- 8bit/pel video out to the Feature Connector for conversion to NTSC-out with Nordic running 640x480 interlaced mode.
  Another idea was to use some of the panel outputs in this case and extend the data out to 16bits.
- The h/w icon can be horizontal or vertical using the Motion Video Window as implementation vechicle -> is it worth?
- IBM Raleigh asked for 12 and 16dots wide fonts for h/w assisted Kanji. 10/04/93
- IBM Raleigh asked for 8bit monochrome TFT panel support. 10/04/93

3.0 Important Additions to 5428 Data Base

1. **32 bit CPU Data bus in VESA VL bus support**
2. **PCI bus support**
3. **Mono and color, STN and TFT Flat Panel support (incl. hfb).**
4. **Live video in a true color window with Windows running in planar VGA mode, without a video port (using PCMCIA standard bus and Sasha's decompression technique).**
5. **CINE PAK decompression accelleration**
6. **Audio Port support for CS4215**
7. **Power Management: panel power sequencing, stand-by mode, suspend mode**
8. **Mixed Voltage, 3.3V operation and low active/suspend/standby power**
9. **h/w icon support, with a h/w cursor support**
10. **BLT performance improvements: Memory Mapped BLT I/O, patternning, 16 byte Source buffer**

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11.*[dual display 1024x768 on CRT with 640x480 on LCD, using the same RAMDAC] - if decided to do now*

4.0 Detailed List of Features

4.1 WAS: On the Cross Talk Reduction Technique -> not in - 1M

This part was deleted from Nordic-1M spec starting rev. 3.8 (09/11/93).

4.2 Green PC Spec Support (Based on VESA DPMS Proposal 1.0p rev. 0.53p)

This specification refferes to CRT Monitor power management. Additionally, Nordic will

TABLE 1. Display Power Management Summary

State	HSYNC	VSYNC	Video RGB	Compliance	Power Savings	Recovery Time
CRT On	Pulsese	Pulsees	Actuve	Mandatory	None	NA
CRT Stand-by	No Pulses	Pulses	Blanked	Opuonal	Minimal	Shon
CRT Sus-pend	Pulses	No Pulses	Blanked	Mandatory	Substantial	Longer
CRT Off	No Pulses	No Pulses	Blanked	Mandatory	Maximum	System Dependednt

control DAC power consumption. These power management CRT Monitor states are not necessarily related to the graphics controller power management states.

We'll define 2 bits - GRE[2:1] (the same as Alpine) that control HSYNC, VSYNC and DAC Power Off signal (or Blankn to the DAC).

TABLE 2. GRE[2:1] Effect

GRE[2:1]	CRT State	Vsync	Hsync	DAC Power	Nordic Power Management State
0	On	pulsing	pulsing	on	active
1	Stand-by	pulsing	static at MISC[6] inactive level	off	active
2	Suspend	static at MISC[7] inactive level	pulsing	off	active or stand-by
3	Off	static at MISC[7] inactive level	static at MISC[6] inactive level	off	active, stand-by or suspend

If Nordic is in its own Suspend mode, the BIOS should program GRE[2:1]=3 to put the monitor (if any) in the Off state.

If Nordic is in its own Stand-by mode, CRT Suspend mode should be forced bt the h/w, as stand-by is a timer driven mode and no s/w gets to play.

If Nordic is in LCD only, the BIOS should set GRE[2:1] to 3 to power off the CRT that may be connected to the notebook computer.

If CRT only mode and CRT is in stand-by or suspend, the BIOS may reduce the video clock and even memory clock frequencies after saving the current values.

Except for the above restrictions, CRT Power Management modes are not related to Nordic power management modes: they can be independently programmed.

If MISC bit is programmed for positive polarity, the SYNC signal will be stopped L, otherwise it will be stopped H.

4.3 Play-back Decompression Accelleration (applicable to Cinepak as well as other compression standards) - old, kept here only for reference

4.3.0 The problem

a) When playback data is compressed on a CD ROM, it is encoded in 24bit/pel YUV with crominance sub-sampling. Due to CDROM reduced bandwidth the display window is 160x120 or 320x240. If this compressed data is decompressed at full pixel depth, it should be displayed as 24bit/pel RGB window under MS Windows. As the play-back data is sent to the graphics controller from the CPU bus, it has to be placed in Video Memory in 320KB.

A standard VGA controller or even GD5428 are able to display the 24bit/pel play-back window only if MS Windows is run in 24bit/pel mode (for instance 1024x768 24bit/pel or 640x480 24bit/pel) by the driver. Under these conditions, the CPU will have to write the un-compressed 24bit/pel play-back data in the appropriate position in Video Memory, contigouus to the entire displayed data.
So, in order to display 24bit/pel in a play-back window, GD5428 needs the driver to run 24bit/pel at the maximum display resolution.
But, in order to run 640x480 at 24bit/pel we need 921.6KB of Video Memory and in order to run 1024x768 24bit/pel we need 2359.296KB of video memory. (Please note that 2M of memory has 2097.152KB).
Also, when running windows in 24bit/pel mode the performance will decrease 3 or 4 times relative to 8bit/pel mode, especially when using DRAM as Video Memory.

b) When running through MS Windows GDI, the driver can play-back data at 15fps or less (with a 486 33MHz). It is desirable to play-back data at 30fps.
This can be accomplished today only if the driver does not go through GDI.

c) If a picyure was stored on CDROM at low resolution (160x120 or 320x240) and it needs to be "zoomed", it has to be interpolated both horizontally and vertically for good picture quality. Vertical interpolation is expensive in h/w.

4.3.1 The Generic Solution - old, here for reference only

Today's Windows Accellerators run MS Windows, including the play-back window with the same pixel depth (8bit/pel), normally going through the RAMDAC, but using a split palette approach with 16 colors reserved for MS Windows and 240 colors reserved for the play-back window. The Cinepak driver writes data in video memory in 3:3:2 RGB format

(8bits/pel) which is created by the driver. Because of the s/w overhead involved in decompression as well as the GDI overhead, it is hard to go beyond 320x240 clips at 15fps, though the display quality is much lower than what Cinepak could achieve (240 colors versus 16 million colors).
To run Cinepak with 24pit/pel resolution, today's graphics controllers would require to run MS Windows in 24bit/pel mode, requiring almost 1MB in 640x480 and over 2MB-s in 1024x768 modes.

A graphics controller that could run MS Windows in 8 or 16bit/pel mode while displaying only the play-back window in 24bit/pel mode would increase significantly picture quality without degrading too much MS Windows performance with play-back, would reduce significantly the amount of Video Memory required for the same picture quality and would allow a higher frame rate for the play-back.

Further, if the play-back data is stored in Video Memory in a semi-compressed format that requires less than 24bit/pel this would further decrease the Video Memory requirements and it may even reduce the video memory band-width requirements.

When zooming the play-back window from 160x120 to 320x240 or higher it is important to interpolate. Vertical interpolation can be done in s/w but with a relatively large overhead. It may be possible to do vertical interpolation on key frames, but there is no practical way of doing vertical interpolation on inter-frames either in s/w or with h/w assist on the CPU write side of the graphics controller. If s/w driven vertical interpolation on key frames is not a solution, then vertical interpolation can be only achived in h/w on the CRT read side and this requires either one or two 16bit/pel line buffers or a big penalty on video memory bandwidth (the equivalent of reading 32 or 48bits/pel).

Horizontal interpolation can be done before play-back data is displayed, without s/w help

Please note that there are multiple ways to solve the play-back problems. In Nordic-1M we'll try to strike a ballance between the complexity of the h/w solution and the quality of the play-back image.

To a large extent, the solution adopted in Nordic-1M will be generic, not tied to Cinepak, though it will be first applied to Cinepak.

4.3.2 Nordic-1M old Play-back Accelleration Solution -> canned, kept here for reference

a)Nordic-1M will run Cinepak at 1:1 scale exactly the same way as today's graphics controllers: in 8bit/pel MS Windows with 8bit/pel (3:3:2 RGB) play-back window

b)Nordic-1M will run 1:2 scale (zoom) in 8bit/pel 1024x768 MS Windows with 24bit/pel (8:8:8 RGB) pixel depth in the play-back window, horizontally interpolated and vertically doubled. Play-back data will be stored in video memory as 16bit/pel (Y0 U01 Y1 U01)

c)Nordic-1M will run at 1:1 scale in 16bit/pel 1024x768 MS Windows with 24bit/pel pixel depth in the play-back window. Play-back data will be stored in video memory as 16bit/pel (Y0 U01 Y1 U01). This mode is good for programs that store data in 320x240 format.

Because today large play-back windows look bad, while small ones look OK, this solution will improve picture quality to a large extent.

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Concerns:

Many play-back programs today don't even have a zoom option. To this extent, mode "b" may not be needed.

Mode c could be implemented today with 16bit/pel RGB (555) in s/w and the only improvement we provide is 24bit/pel capability and h/w color conversion (some level of accelleration). So mode "c" may not be needed as a special h/w.

If this is the case, maybe we do not need to do anything in h/w for Cinepak !

One idea: should we run 24bit/pel MS windows stored in 4:2:2 (Y0 U01 Y1 U01) format? This will allow us to run 24bit/pel MS Windows and use 16bit/pel memory space with no loss of quality. The windows driver could compress the data and the h/w could decompress it.

4.4 Nordic-1M Motion Video Architecture

Sasha Eglit, Rakesh Bindlish, Vlad Bril and Dave Keene are important contributors to the Motion Video Architecture definition.

4.4.0 The Problems to Solve & Generic Solutions

Nordic-1M is supposed to support CDROM play-back and live-video under Microsoft's Video for Windows. With all of today's VGA Compatible Graphics Controllers, the play-back picture pixel depth has to be the same as the surrownding MS Windows pixel depth. In other words, we have to run MS Windows in a 24bit/pel mode in order to display 24bit/pel in the play-back window.
The only way we can run today live video is from a Video Port (= Feature Connector). In this case we'll use an overlay or a color key to define the live video window.
Due to CDROM player, s/w interface complexity, CPU bus and Video Memory limitations, only small clips at 15fps or less can be playd-back today. So today we need a lot of Video Memory to run small clips in slow motion at low rezolution. Nordic-1M will try to use less Video Memory, increase the clips size, their resolution and speed.

Nordic-1M is supposed to support:

- accellerated play-back for all popular CDROM compression standards, especially Cinepak and Indeo
- live video from a PCMCIA card in a system with a standard PCMCIA host adapter, for a "Multimedia-Ready Notebook Computer"
- live video from a Feature Connector, preferably VESA Advanced Feature Connector compatible, for a Multimedia Notebook Computer with direct NTSC input (full mother-

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board solution).

What will Nordic-1M bring to the Video plate:

A. Nordic-1M will break the dependency between the pixel depth of MS Windows and the pixel depth of the live-video / play-back window. By doing so, Nordic-1M will be able to run 24bit/pel LV/PB while running MS Windows in 8bit/pel or 4bit/pel (even planar) This will lead to high quality live-video and play-back, while minimizing Video Memory requirements.

B. Nordic-1M will further reduce Video Memory requirements as well as Video Memory Bandwidth requirements by storing data in compressed form: 4:2:2 YUV (16bit/pel). 4 1.1 YUV (12bit/pel) or Sashapak YUV (2.6bit/pel)

C. Nordic-1M will define one architecture and work-frame to run both play-back and live-video in a unitary way for both s/w and h/w.

D. Nordic-1M will support up to two active LV/PB windows at the same time.

E. By providing h/w YUV->RGB conversion and 1:2 zoom Nordic-1M will accellerate playback for most standards, but mostly for standards that allow us access to their decompressor like Cinepack (for whose decompressor we have a licence).

Nordic-1M will not provide Cinepak specific accelleration (custom BLT).

On the Live Video from Feature Connector (or Video Port)

Due to pin-out limitations, the VAFC implementation has to be limitted to 8 pins of data requiring external muxing of 16bit data to Nordic. Further, the VAFC solution will be restricted to 5428 type support: overlay and color key (no memory video port). The only additions to the 5428 support will be the internal YUV-> RGB converter able to accept sequential 4:2:2 YUV (16bit/pel in avarage: Y0,U,Y1,V) and display it as a 24bit/pel RGB in the overlay/color-key window. We may also support horizontal 1:2 zoom with avaraging. Nordic-1M will be back-wards compatible to 5428 and it will support also 16bit 5-5-5 RGB Sierra and 5-6-5 RGB XGA pixel formats. As in 5428, live video from the Feature Connector can be executed only from mode 5F (640x480 256 colors).

In the following we will refer mostly to the other two modes of operation: play-back and live video from a PCMCIA card, which we'll call compressed live video, because due to PCMCIA bus bandwidth limitations, we assume that video data received by Nordic is compressed with Sashapak (see Sashapak detailes further in this spec). Please note that due to its huge advantages, it makes sense to use Sashapak as a mother-board solution too The main reason we continue to support the Feature Connector based live video is the availability of drivers for 5428 which will give Nordic an early start in the live video arena.

Video Memory Band-width Constraints

Please note that, even with a 32bit wide Video Memory, there are severe memory band-width limitations when running 16bit/pel and 24bit/pel graphics modes.

Assumming that Nordic-1M does 8 CRT fetches in a row and 1 CPU cycle, for a CRT or TFT panel, here are the minimum frequency requirements for memory clock frequency at different rezolutions and pixel depths:

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24bit/pel:
R+7P+R=12m+14m=26m with 1 CPU cycle per CRT FIFO fill fetches data for 32B/3B=10pixels
R+7P = 6m+14m = 20m with no CPU cycle during non-display time
min mclk freq = 65MHz / 50MHz @ 640x480 -> Nordic-1M upper limit at 5V CVDD
= 104MHz / 80MHz @ 800x600 -> too high
= 169MHz / 133MHz @ 1024x768 60Hz -> too high

16bit/pel:
R+7P+R=12m+14m=26m / R+7P = 20m fetches data for 32B/2B=16pixels
min mclk freq = 40.6MHz / 36MHz @ 640x480 -> OK even at 3V
= 65MHz / 50MHz @ 800x600 -> Nordic-1M upper limit at 5V CVDD
= 105MHz / 83MHz @ 1024x768 60Hz -> too high

12bit/pel:
R+7P+R=12m+14m=26m / R+7P=20m fetches data for 32B/1.5B=21pixels
min mclk freq = 30.9MHz / 23MHz @ 640x480 -> OK even at 3V
= 49.5MHz / 38MHz @ 800x600 -> OK even at 3V
= 80.4MHz / 64MHz @ 1024x768 60Hz -> too high

8bit/pel:
R+7P+R=12m+14m=26m fetches data for 32B/1B=32pixels
min mclk freq = 20.3MHz @ 640x480 -> OK even at 3V
= 40.6MHz @ 800x600 -> OK even at 3V
= 52.8MHz @ 1024x768 60Hz -> OK at 5V

We may conclude that Nordic-1M will be able to run 24bit/pel only at 640x480 rezolution, 16bit/pel up to 800x600, 12bit/pel up to 800x600 and 8bit/pel up to 1024x768 rezolution. These results apply only to CRT or TFT and single scan STN panels.
Please note that for dual scan STN panels the memory requirements increase significantly

These severe memory bandwidth limitations lead us to attempt to minimize video memory traffic. If we store **Cinepak data in 4:2:2, with an avarage of 16bit/pel**, independent of Cinepak window size, **Nordic-1M will not be able to run Cinepak above 800x600.** Any attempt to execute vertical zoom with interpolation, even with two points interpolation will further aggravate this memory band-width bottleneck. The next step should be 100MHz SDRAM-s with a large CRT FIFO (32x32) or 64bit wide memory data bus. These considerations apply to any playback compression standard that stores data in video-memory as 16bit/pel in avarage. The key to a successful compression standard would be one that does decompresssion on the CRT memory read and stores data in memory as 8bit/pel or less, in avarage.

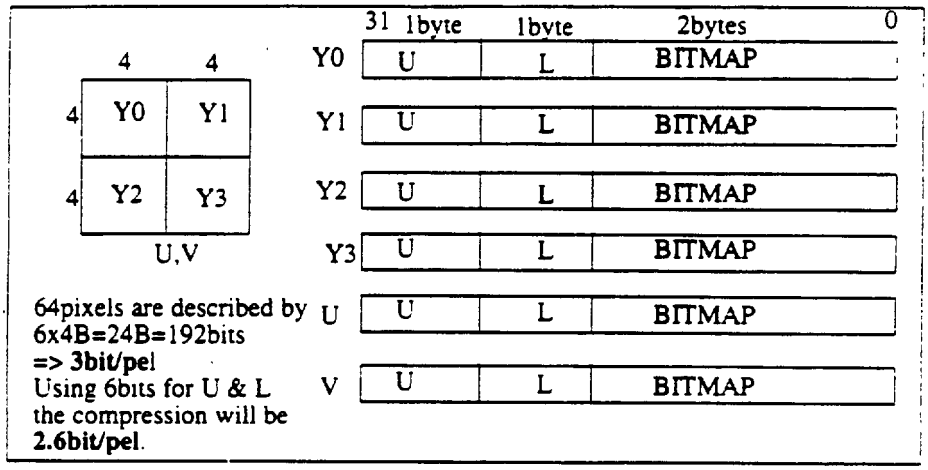
As we store live video at 2.6bit/pel and fetch it as if it was 8bit/pel with Sashapak, Nordic-1M should be able to run live video even at 1024x768.

If we defined a new CDROM play-back standard based on Sashapak, then we could run even 1024x768 with 24bit/pel accuracy and keep it memory as an 8bit/pel. **Keith and Ken are actually working on it, with Sasha's help.**

Sashapak is a highly assymetric, lossy "Block Truncation" compression algorithm optimized for visually equivalent image processing.

Data is proccessed as Y,U,V one byte each. U and V are sub-sampled, characterizing one 8 by 8 pixel array, while Y is characterizing a 4x4 pixel aray. Actually one of two values is assigned to each pixel inside the 4x4 (for Y) and 8x8 (for U and V).

At compression time, the compression chip determines a threshold and two values U&L for each group of sixteen (4x4) pixels. This way all pixels above threshold will be assigned the value U, all pixels below threshold will be assigned the value L



At decompression, the bitmap will control a mux between the U and L values. This way the decompression is straightforward.

The main drawback of this approach is that a BITMAP contains Y data from 4 scan lines and U,V data from 8 scan lines. When data is read from memory to be displayed only data from one scan line is used. Similarly the U/L values apply to several scan-lines and the same value will be read in each scan line. The same data will be read again and again in each scan line raising the actual memory bandwidth requirements to an equivalent of 16bit/pel map.

In order to overcome this problem and reduce memory bandwidth requirements, Sasha proposed a **scan line oriented, segregated mode of data organization**. This would require the Sashapak compression chip to write compressed data in a specific way puting the strain on the compresion chip address generator. The basic principles of the new organizations are:

1. Data is organised in the MV Window in chunks of 32 sequential pixels.

a)For **8bit U/L resolution**, as one Y covers 4 pixels, 8 U/L sequential values are needed, 16bits each -> **8x16/32=4W** (8x12/32=3W for 6bit res. U/L) (where W is a 32bit word)

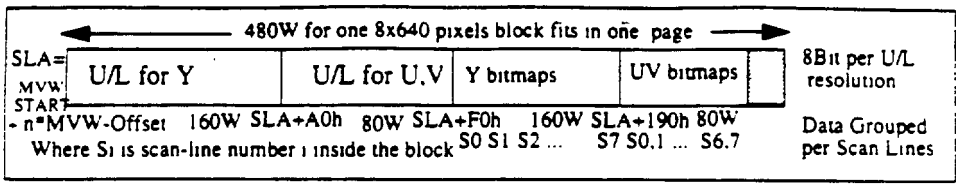
b)U and V U/L data is packed together in the same word (16bits for U U/L and 16 bits for V U/L -> total 32bits=1W) and as one pair of U and V applies to 8pixels, 4 such values are needed for 32 sequential pixels -> **4x32=4W**. (4x12x2/32=3W for 6bit res. U/L)

c) The mask data is also scan-line oriented: all 32bits of Y mask of sequential 32pixels are placed in one 32bit word and due to sub-sampling on U and V, all 32bits of U and V mask of sequential 32pixels are placed in one 32bit word. So in 2W data for 32 sequential pixels on one scan line is packed. -> **2W** (the same for 6bit resolution for U/L)

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d) For 640x480 window size, even at 8bit U/L resolution, data for 8 scan-lines fits in one DRAM page (symetric DRAM-s assumed): 320WY+80WU+80WV=480W < 512W page



f) The key to memory bandwidth optimization is the fact the the compression chip will organize data sequentially over 32 pixels instead of 8. This will be done for the mask bits which will be organized sequentially by scan line and for the U/L data. This way a 32bit word of Mask data contains only information for the current scan line and no extra memory fetches are required. The main reason we segregate U/L for Y and U/V is the fact that we want to use 6bit U/L. In this case it is easier to identify the proper U/L info chained within 32bit words if the words are sequential and we have a fix relationship between their address and the 6bit U/L quantities.

g) If we calculate now the amount of data we need to fetch to display 32 sequential pixels:

- for 8bit per U/L: 4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B
  --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
- for 6bit per U/L: 3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B
  --> 32B/32pixels = 8bit/pixel

This is a very good data fetch ratio, much better than the 16bit/pel we'd get without the optimization.

g) When reading data from the Motion Video Window the controller will generate the following sequence of addresses, all of them in the same DRAM page (8bit per U/L):

- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset, +1, +2, +3
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h, +1, +2, +3
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h
- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset+4, +5, +6, +7
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h+4, +5, +6, +7
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h+1
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h+1
- now the MVW FIFO is full.
- chunks of ten 32bit words will be proccessed for every 32pixels displayed
- the MVW FIFO gets empty after the first 10 words being read for decompression and display.

Please note that all data for every 8 scanlines starting from the top of the MVW is in the

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same DRAM page.
Because we have to fetch the MVW Data before we start displaying it, and because at that time the CRT FIFO does not empty as fast as it is needed (unless MS Windows is running at the same pixel depth as the MV Window), it is necessary to have a separate FIFO for the MVW or at least half the FIFO (at least 10W for 8bit per U/L and at least 8W for 6bits per U/L).
h) When we run 6bit per U/L, because the Video Memory band-width requirements are as if we were running 8bit/pel, we could do vertical zoom with avaraging. But there should not be a need for zoom with Live Video because there is enough CPU and memory band-width to run 640x480 windows even when MS Windows is run as 1024x768 4 or 8bit/pel

Conclusion: With Sashapak we can get data organized in memory such that the memory bandwidth is as for 10bit/pel (8bit U/L) or 8bit/pel (6bit U/L) pixel depth. The actual memory area will be close to 3bit/pel or 2.6bit/pel depending on the resolution of U/L values - 8 or 6bits per value.
Please note that the memory area will be slightly larger due to the fact that we use only 480 words in a page of 512.

4.4.2 YUV to RGB Conversion Algorithm

The ideal YUV to RGB transformation is:
R=Y+1.37V
B=Y+1.73U
G=Y-0.699V-0.336U

After defining an objective way of measuring color error, Sasha came up with the following Conversion algorithm:
R=Y+1.375V=Y+1 3/8 V
B=Y+1.75U=Y+1 3/4U
G=Y-0.375U-0.75V= Y-(3/8U+3/4V).

This algorithm can be implemented with 8 9bit adders and it should support excess 128 or two's complement U,V formats (U,V may be negative while Y is always positive).
This algorithm will be used with Live Video.
For Cinepak, the YUV->RGB converter will be reconfigured to the Cinepak YUV->RGB conversion rule:
R=V+Y
B=U+Y
G=Y-V/2-U/4

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4.4.2 Motion Video Architecture Functional Blocks

Instead of treating play-back and live-video as two separate modules, we'll isolate several generic functions to be used by both

- Display Window Generation Block:
allows s/w to define one or two play-back or live video **window(s)**.
The MV Window is defined in memory cycles relative to the start of line in horizontal and frame in vertical direction. Horizontally the unit of measure is different outside relative to the inside of the window: the horizontal window start coordinate is expressed in memory cycles for the surrounding pixel depth (MS Windows pixel depth, normally 4 or 8 bit/pel), while the width of the MVW is expressed in memory cycles for the MVW pixel depth (8bit RGB, 16bitRGB, 422YUV spacial, 422 YUV linear, 411YUV linear, Sashapak).

- **XS** = MVW Horizontal Start Coordinate (in surrounding pel depth memory cycles)
The horizontal position is programmed with 8 pixel resolution (0,8,16,... pixels starting from the left side of the screen)
XS register CR34[7:0] -> 8 bits
(up to 1K pels in increments of 8 pels)
To get an early warning, we will require XS to be programmed 8 pixels less than the actual position: 0 is zero, 1 is 16pels, 2 is 24 pels,...
- **XW** = MVW Horizontal Width (MVW pel depth memory cycles)
XW register CR35 [7:0] -> 8 bits
(up to 1K pels in increments of 8 pels)
To get an early warning, we will require XW to be programmed 8 pixels less than the actual width: 0 is zero, 1 is 16pels, 2 is 24 pels,... width.

- **YS** = Vertical MVW Start (in true scan-lines not affected by scan-line doubling or panel vertical expansion)
10 bits in CR36[1:0] (msb-s) and CR37[7:0] (lsb-s).
- **YE** = Vertical MVW End
(all bits are programmed, in true scan lines)
10 bits in CR36[3:2] (msb-s) and CR38[7:0] (lsb-s).
- **SAdOf=** Surrounding Address Offset (a number to be added every line to the surrounding CRT Address Counter value to allow it to jump over the MVW without counting through it. This allows calculating the surounding restart address.) This number depends on the surrounding mode resolution. Assuming a maximum line of 1024 pels, in increments of 4 pels per address (8bits/pel), 256 addresses is enough -> 8bits.
8bits in CR39[7:0]
- **WMAdS** = MVW Memory Address Start in increments of 16KB = 4KW (a phisical address 00000:3FFFF for 1MB or 00000:7FFFF for 2MB Video Memory).
7bits in CR3A[6:0]

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- **WMAdOf = MVW Memory Address Offset** (A number to be added to the current MVW Start Address to get the next MVW start Address) Having this s/w model allows panning through a large image for the MVW The actual image stored in memory may be as large as 1K pixels

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at 16bit per pixel (2 per word) -> 9bits.
9bits -> in CR36[4] (msb) and CR3B[7:0] (lsb).
Because the CRT Address Counter counts surrounding memory cycles, during the MVW display it would count a wrong number corresponding to the MVW pixel depth. To avoid this wrong count, the CRT Address Counter is stopped while MVW is displayed and loaded with the value corresponding to the end of MVW and restart of the surrounding display. As this address value changes every line, an offset is specified and will ba programmed by the MS Windows driver depending on the MVW size and pixel format The horizontal size of the window is controlled by a different counter counting to XW During the MVW display the adddress will be generated by the same CRT Address Counter which will be loaded with a MVW Memory Address Start (WMAdS).

- **XW8P = MVW Horizontal Width in 8 pixel units**. Defines the size of the window in 8 pixel units. It is used to terminate the window horizontally. It may require to program the value minus one or two. To be Defined Later. Register CR3D[6:0] will contain this value.

Every scan-line
MVW Scan-Line Start Address = Previous Scan-Line MVW Start Address + WMAdOf

Scan-line doubling for "zoom" should be taken into account when designing the MVW Architecture: on the address generation block.

- **Off-screen MV Memory Addressing and Access Control.** This includes data type tag generation based on MV memory Address and the circuitry placing the tags in the CRT-FIFO. This block has provisions for scan line replication by repeating the MV address generated on the previous scan line of the MV window (only).
As Cinepak needs 4:1:1 rectangular format the MV Memory Address Counter needs to count in a non sequential way:
Y0Sn Y1Sn Y2S(n+1) Y3S(n+1) U V
implies an address counter that can skip over two numbers, or maybe **a second address counter that starts counting from 2 instead of zero.**
- **One tag bit is generated based on CRT Address and is 1 if the data in the CRT FIFO is from the MVW, other-wise is 0.** This tag bit, called the **steering bit** will be delayed through the entire data path and end up controlling the final video data mux just before the DAC.
Other tag bits called "data-type" tag bits encode the type of 32bit word in a given data format and are used by MVW Decoder/Serialiser to steer CRT-FIFO data at CRT-FIFO read.
For instance, in 4:1:1 linear data format, data is stored in memory and in the CRT-FIFO as Y0Y1Y2Y3 U03V03Y4Y5 Y6Y7 U47V47, 3 groups of 32bits. Two "data-type tag bits will mark the three types of 32bit words so that steering logic knows where to place the three words in the data serialiser.
Similarly Sashapak will need 3 "data-type" tag bits to encode 8 32bit words (for 6bit per U/L) or 4 "data-type" tag bits to encode 10 32 bit words (for 8 bits per U/L).

16bit RGB 5:6:5 and 5:5:5 and 8bit RGB 3:3:2 can either use the **standard VGA data**

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path, which in 5428 was extended to 16bit wide (used for 16bit/pel 1kx768 interlaced) or the new data path, **if a phisically new data path will be actually created**.

- **MV Data Path .** This is area wise the largest piece. It consists of a new 16bit wide data-path with the same delay as the VGA data path, that takes MV data from the MV prefetch cache and the CRT FIFO, treats it appropriately depending on the MV data format encoded in the MV tags and converts it to 24 bit YUV first and 24bit RGB second. Horizontal zoom with avaraging (or maybe 5 levels of interpolation) is in this block too.

- **Larger (26 or 24 stages) CRT-FIFO, Variable CRT-FIFO threshold and its control.** Because the MS Windows pixel depth and MVW pixel depth don't match, it is necessary to reserve CRT-FIFO space to fill in enough high pixel depth data before the MVW display starts. In Sashapak this means 10 or 8W (for 8 or 6bits per U/L respectively).
This function can be implemented as a dinamic threshold size modification of the CRT-FIFO. If the CRT-FIFO has 24 stages instead of 16 but only 16 stages are used before the MVW but it is switched to 24 when MVW fetches start, there will be 8 more stages to fill at that time ensuring more prefetched data in the CRT-FIFO at the beginning of each MVW scan-line.
In normal operation the threshold is 8 (or 6).
Here is the sequence of events that follow the detection of MVW start:

1. **Drop CRT-FIFO threshold to 1 to get immediat service & make 10 (or 8) more stages available in the CRT-FIFO.**
2. **Start fetching MVW data till CRT-FIFO is full. (BLT in progress will increase latency)**
3. **Increase threshold to 10.**
4. **Proceed as such till end MVW.**
5. **Load the CRT Address Counter with its last contents + SAdOf**

(where SAdOf = Surrounding Address Offset)

7. **Continue fetching based on the new address (start with random cycle). CRT-FIFO threshold remains the same - at least 10 or 8. CRT-FIFO size is still 26 or 24.**
8. **At the end of line, upon flushing the CRT-FIFO before prefetch, decrease CRT-FIFO size back to 16 keeping the threshold the same.**
9. **Go back to #1 for the next scan-line.**

This sequence is applied if MVW pixel depth is higher than surrounding pixel depth. If MVW pixel depth is lower than surrounding pixel depth, then the action described at #1 above takes place at the end of MVW, instead of the beginning. *In other words, FIFO depth extension takes place when a switch from low to high pixel depth occurs.* If MVW pixel depth is the same as the surrounding, only the address is switched. In this case the CRT FIFO depth and the threshold remain the same.

- Steering logic decode the tags comming out of the special addition to the CRT-FIFO and the pre-fetch buffer and controls the decompression, formatting and serialization.

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(they tell the formatter what data is Y, U or V).

- What about the video serializer load and the CRT FIFO read signal? What hapens to them when in MVW? They are one signal today.
WHEN the data path switched to display MVW data, what hapens with the VGA Video Data Path is don't care as we do not display that data, except for the h/w cursor anf the h/w icon that do not go through the standard VGA serializer. So we'll probably stop the VGA data path untill the point h/w cursor and h/w icon are combined into it, to save power, as we will stop the MVW data path when not in use, for the same reason.
So, the Video Serializer Load may be stopped while MVW data is displayed, **but the CRT FIFO read will be going on, with a frequency and shape depending on the data format loaded in the CRT FIFO for display.**
In RGB 3:3:2 8bit/pel direct color mode CRT-FIFO read will be generated every 4 vclks.
In standard RGB 5:5:5 or 5:6:5 16bit/pel modes CRT-FIFO read will be generated every two vclks.
In YUV 4:2:2 24bit/pel (Y0 U Y1 V on one scan line) the CRT-FIFO read will be generated also every two vclks.
IN Sashapak 10 (for 8bit per U/L) or 8 (for 6bit per U/L) CRT-FIFO read pulses will be generated every 32 vclks.
- The MVW Address Counter, loaded at the beginning of each MVW scan-line with a start address calculated based on the Start MVW Address and the MVW Address Offset, will count at format dependent rate for as long as the CRT-FIFO is not full. Because the CRT-FIFO will be emptied faster in the MVW (in general the pixel depth will be higher in the MVW) there will be requests for more memory cycles when displaying in the MVW.

- If either h/w cursor or h/w icon are on, they should be displayed even if the direct data path is used. In this case both video data pathes will clock and the steer tag will point to the VGA data path when either h/w cursor or h/w icon or both are displayed, even on top of a MV window. Please note that neither the h/w cursor, nor the h/w icon data go through the CRT FIFO or the VGA Data path except for the final pixel address block and the RAMDAC RAM, though they have a special path in the RAM. So we could stop most of VGA data path (including the internal palette) but not all of it even if we are in 16bit/pel mode (the new one that goes through a separate 16bit data path).

- If we are in a 16bit/pel mode with no h/w cursor or h/w icon, or in a 640x480 MVW mode filling the screen, we can stop the VGA data path to save power

- The off-screen MVW memory will be a programable start memory array normally placed towards the end of the memory, but before h/w cursor, h/w icon and the half frame buffer, even the color one. The start of the MVW memory will be programable in increments of 4KW (16KB) as a physical address -> 7bits to program.
CR3B[6:0] is the MVW Memory Array Start Address.
2MB configuration will support enough memory to support:
- one 640x480 3bit/pel window or up to two 320x240 3bit/pel (Sashapak) -> 32KW
- one 640x480 16bit/pel window or two 320x240 16bit/pel windows
(153.6KW=614.4kB out of 256KW or 512KW available depending on the memory con-

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figuration) .

- all of the above at the same time up to a total of two windows though.

1MB configuration will support:

- one 640x480 3bit/pel Sashapak window or two 320x240 Sashapak windows or
- two 320x240 16bit/pel windows.

Please note that about 24KW are needed for 800x600 DS Color STN HFB, the h/w cursors and h/w icons while about 18KW are needed for 640x480 DS Color STN HFB and that

- 640x480 4bit/pel requires 38.4KW
- 800x600 4bit/pel requires 60KW
- 1024x768 4bit/pel requires 98.3KW
- 640x480 8bit/pel requires 76.8KW
- 800x600 8bit/pel requires 120KW
- 1024x768 8bit/pel requires 196.608KW

Video Motion Formats supported are:

- 8bit RGB 3:3:2 going through the palette (RGB 3:3:2)
- 16bit RGB (5:5:5 Sierra and 5:6:5 XGA) not going through the palette -> this is a 16bit/pel that does not require double dotclock !!
- 4:1:1 array converted to 4:2:2 Y0 Y1 Y2 Y3 U V -> Y0UY1V Y2UY3V for Cinepak (with Y2Y3 for the next scan line)
- 4:2:2 linear Y0UY1V from TV Decoder
- Sashapak format (we'll support only 6bit/pel)
  - for 8bit per U/L:
    4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B
    --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
  - for 6bit per U/L:
    3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B
    --> 32B/32pixels = 8bit/pixel

CR3C[3:0] will encode the pixel format for the first motion video window data.

0h = 0000 = 8bit RGB 3:3:2 going through the palette
1h = 0001 = 16bit RGB Sierra (5:5:5)
2h = 0010 = 16bit RGB XGA (5:6:5)
3h = 0011 = 4:2:2 YUV Y0UY1V
4h = 0100 = 4:1:1 YUV linear Y0Y1Y2Y3UV
5h = 0101 = 4:1:1 YUV array Y0Y1Y2Y3UV but Y2Y3 are in next scan line
6h = 0101 = Sashapak 6bits for U/L
7h = 0110 = Sashapak 8bits for U/L
8h:Fh = 0111:1111 = reserved

CR3C[4] = Enable Motion Video Window
CR3C[5] = Enable Live Video in Full Screen
CR3C[7] = MVW horizontal zoom (doubling)
CR3C[6] = MVW vertical zoom (doubling)

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Note: We will not support 4:1:1 linear from TV decoder, for design simplicity.

Memory data formats:
- 8bit and 16bit RGB, as in 5428.
- 4:1:1 Cinepak converted to 4:2:2 by writing a 4:2:2 Code-Book

first scan line -> Y0UY1V -> One 32bit Word

---

second scan line in memory -> Y2UY3V -> One 32bit Word

- 4.2:2 linear will be mapped in memory as follows:

first scan line Y0UY1V
first scan line Y2UY3V

---

consecutive data in the same scan line.

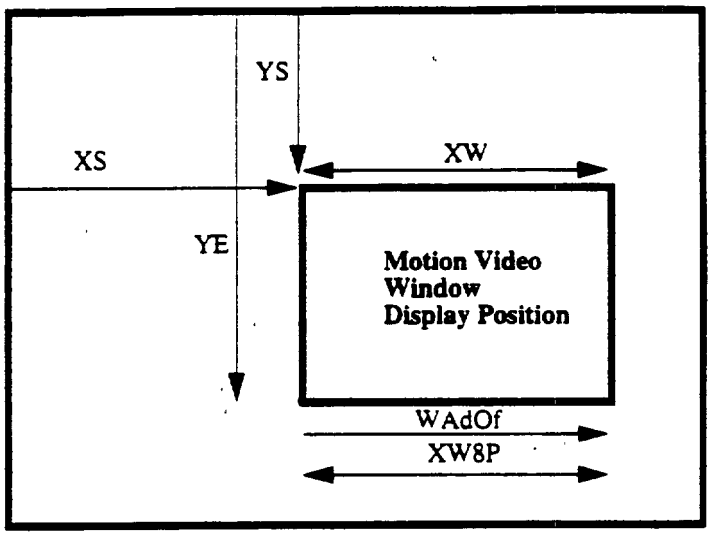
The tags that accompany the motion video data through the CRT-FIFO mark both the data format and the type of data inside the format (U/L for Y or U,V or mask for Y or U,V in Sashapak, Y0, Y1,U or V in 4:2:2).

Double Buffering for MVW Video Memory Data

In order to get a high quality Live Video full frames should be displayed at all times. This assumes that writing the video buffer and displaying it are in sync, which is normally not the case.
To solve this problem and provide a simple interface between MVA h/w and the driver, Nordic will support a double buffer approach:

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Full Screen in a given graphics mode



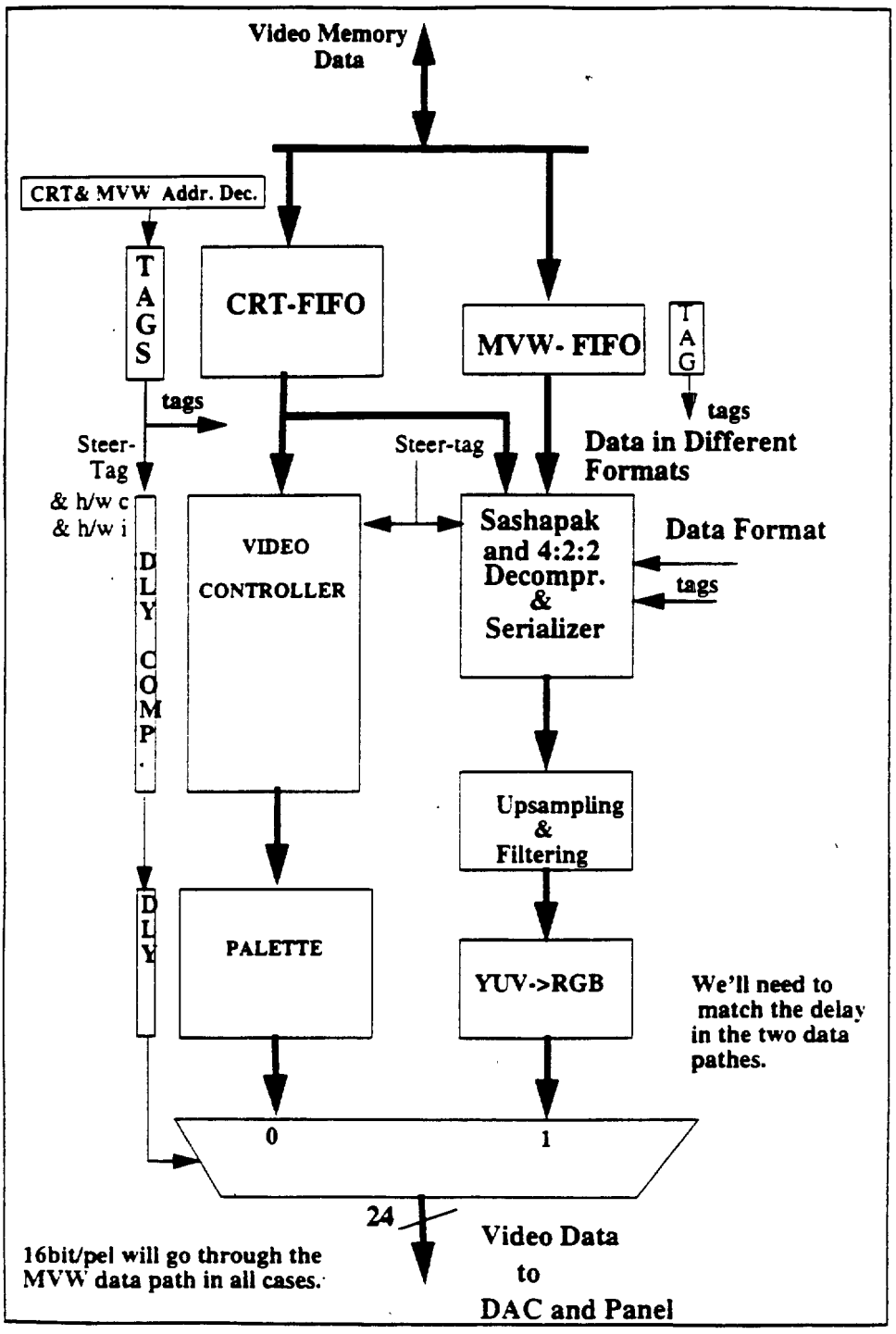
Where:

- **XS** = MVW Horizontal Start Coordinate (in surrounding pel depth memory cycles)
- **XW** = MVW Horizontal Width (MVW pel depth memoty cycles)
- **YS** = Vertical MVW Start (in true scan-lines not affected by scan-line doubling or panel vertical expansion)
- **YE** = Vertical MVW End (all bits are programmed, in true scan lines)
- **WAdOf** = MVW Address Offset (a number to be added every line to the CRT Address Counter to allow it to jump over the MVW without counting through it.
- XW8P = MVW horizontal width expressed in 8 pixel units

Please note that MVW horizontal width is defined twice in different units:
XW defines it on the memory side in memory cycles
XW8P defines it on the CRT side in 8 pixel units

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Video Memory Data
CRT& MVW Addr. Dec.
TAGS
CRT-FIFO
MVW- FIFO
TAG
tags
tags
Steer-Tag
Steer-tag
Data in Different Formats
& h/w c
& h/w i
DLY COMP.
VIDEO CONTROLLER
Sashapak and 4:2:2 Decompr. & Serializer
Data Format
tags
Upsampling & Filtering
DLY
PALETTE
YUV->RGB
We'll need to match the delay in the two data pathes.
0
1
24
16bit/pel will go through the MVW data path in all cases.
Video Data to DAC and Panel

4.5 Feature Connector Support

Nordic-1M will support 5428 Feature Connector so that it is compatible to Media Manager.
Nordic-1M will support VAFC (Vesa Advanced Feature Connector) in the 8bit VSVPC passthrough compatibility mode.
The main difference beteen 5428 FC and Nordic FC is the fact that 5428 FC has one EDCLKn control pin controlling the direction of the DCLK pin, while Nordic-1M as well as VAFC have a FCDCLK output pin and a FCVCLK input pin.
Dave Keene believes that 5428 FC is VAFC compatible. To ease the design, I kept 5428 FC pin names (not VAFC pin names).
On VAFC compatibility here are some comments:
- GENCLK can be applied on XVCLK if SR22[3]=1.
  But, if SR22[3]=1 (select xclk) & SR24[7]=1 (VAFC enabled), then XMCLK should get OSC and MCLK Synthesizer operates normally, except that the reference frequency comes from XMCLK instead of OSC pin. If SR22[3]=1 & SR24[7]=0, then MCLK comes directly from XMCLK pin and the MCLK and VCLK Synthesizers are powered-down !!
- GRDY signal is similar to OVRW.
- VRDY is similar to EVIDEO if EVIDEO is dinamically switched as a valid data in signal.
- EGENn is not needed if we configure Nordic-1M in the right configuration with SR22[3] (XCLKPU) and SR24[7] (VAFCPU).
- As VAFC maximum FCVCLK frequency is 37.5MHz, VAFC supports a mode in which data is sent at 37.5MHz to the DAC and it each pixel will be displayed twice if the chip is running at 75MHz pixel clock. This allows only 8bit/pel data to be displayed. To display 16bit/pel data we should use both phases of the FCVCLK and pack the data into one pixel. I think that this is already done in 5428, if not Man-Shek and Fong-Jim are modifiying the 5429 RAMDAC to support this mode -> we need to support it too.
- VAFC requires FCDCLK to be switchable under s/w control beteen 1x and 1/2x the pixel clock. If we took this out of Nordic-1M data base, we should put it back, but the divide by two should affect only FCDCLK going out of the chip.

Check VESA VAFC Proposal 1.0p rev. 0.31 07/15/93 for VAFC timing info.

Nordic-1M FC Pins Functional Description

Most of this is from 542X Data Sheet page 3-26:

VSYNC and HSYNC	TO	The standard CRT pins tri-stated when FCESYNCn is L. Thes pins have programable polarity.
FCBLANKn	I/O	BLANKn in 5428. If FCESYNCn is H, this is an output and it supplies the actual composite BLANKn CRTC signal. VAFC requires this to be the composite Display Enable (no borders). If this is the case, we'll need a bit for VAFC that puts DE = HDE & VDE inverted on BLANKn.

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If FCESYNCn is L, FCBLANKn is an input and it forces RAMDAC RAM outputs to 0 (black), but it should force them black before they go to the panel.

It seems that by connecting OVRW output to BLANKn as input we can display FC data in a window - this will work though only if OVRW, internally controls the pixel address mux between normal VGA data and the FC data.

FCP[7:0] I/O P[7:0] in 5428.
If FCEVIDEOn is H, these pins are outputs and represent the pixel address of the RAMDAC.
IF FCEVIDEOn is L, these pins are inputs and represent the pixel address to the RAMDAC.
CR1A[3:2] control the way the FCP[7:0] are muxed with the normal data.

FCDCLK O (the actual pin is I/O) outputs VCLK or VCLK/2 if selected through s/w.

FCESYNCn I ESYNCn in 5428. Controls HSYNC, VSYNC and FCBLANKn (H-> outputs, L-> H/VSYNC are tri-stated, FCBLANKn is tri-stated.).

Nordic does not have EDCLKn input as FCDCLK and FCVCLK are not shared.

OVRW O OVRW in 5428 = Overlay Window. **This active Low** signal, is generated by the BLANKn VT and HT logic (shared) and is supposed to be used to create an Overlay Window in which data from the Feature Connector is displayed. *I don't know why we output this signal. It should be controlling the MUX between the normal pixel address and the FC originated pixel address.*

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4.5.1 On the Video Port for TFT Panels

A Video Overlay live video solution requires a TV Decoder Chip Set, a de-interlacer (at least a line buffer, but usually a full frame buffer), a scalar/filter/color converter chip (like CL-PX0072, CL-PX0070 or the more expensive CL-PX2070). To display live video in a window at 800x600 or 1024x768 a full frame buffer is needed and some frame level synchronization needs to be achieved.

Is there a cheap way to display full screen TV on a 640x480 panel?
Is a video port a cheap system solution to the above problem?

Can we design a system that uses a universal TV Decoder like SAA7151A and feeds data directly to a Video Port that displays live video at 640x480 30fps with no additional components? This is what customers require!

Problems to solve:

1. Accept 7151 data format: 4:2:2 YUV at 6.75MHz or 4:1:1 YUV at 3.375MHz, interlaced.
2. Synchronize at frame level.
3. De-interlace. Optionally display only odd fields with scan line doubling (according to Sasha this looks better than displaying true de-interlaced picture).
4. Get enough memory bandwidth with a 32bit wide DRAM.
5. Have enough storage space on the Graphics Controller to go over the CRT horizontal non-display memory refresh & prefetch time while Live Video Data comes at normal TV display speed.

4.5.1.1 Data Format

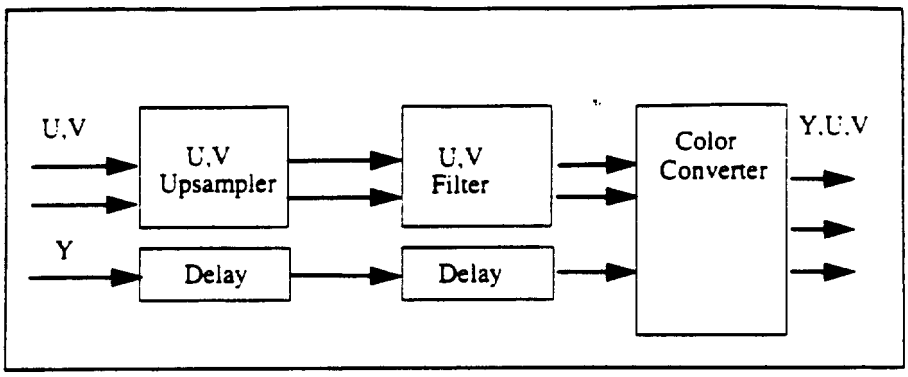
In order to accept YUV data, we need good up-sampling filters on U and V. After up-sampling and filtering we need a Color Space Converter with 2-th complement (for 7151) or excess 128 (for other TV decoders). A good 4:1:1 UV up-sampling filter is quite complex and requires many stages of pipe-lining (9 or 11) . A good 4:2:2 UV up-sampling filter requires less than 5 stages of pipe-lining.

As data is stored in TV decoder format, up-sampling, filtering and color conversion are done on the CRT read side at dot-clock rate.

Please note that 4:1:1 data requires 48 bits of storage (two data packs will fill 3 32 bit words).

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4.5.1.2 Synchronize at Frame Level

To avoid moving objects jagging we should display only full frames. In many systems today this requirement is not met. For instance play-back systems display as fast as possible without any regard for frame synchronization. According to Sasha this is not good for TV. How bad it is remains to be seen.
If the CRT/TFT display runs at 27MHz (double TV dot-clock rate) it is possible to use a double buffer scheme in which we display twice each frame while writing one TV frame in the other video buffer and alternate the two buffers. For a 640x480 display at 4:2:2 YUV we'd need 2MB of DRAM, as the buffers are embedded in the Video Memory (614.4KB per buffer needed).
Even with this scheme, external VSYNC from the TV Encoder should be used to synchronize (= reset) Nordic vertical counter, so that TV and Graphics frames start at the same time. SAA7151 outputs VS (TV VSYNC) which can be used as external SYNC by Nordic
If only odd fields are displayed, half data is stored reducing Video Memory requirements to 307KB per frame (614KB total which fits in 1MB). This is not a bad idea especially if the picture looks better!

4.5.1.3 De-interlace

This is naturally done by writing data in the Video Memory. If only odd fields are displayed, Nordic has to determine the field boundary by counting HS (TV HSYNC) pulses.

4.5.1.4 Memory Bandwidth with 32bit Wide DRAM

There are two cases: 4:2:2 YUV and 4:1:1 YUV.

A. 4:2:2 YUV Bandwidth Requirements

CRT-dot-clock frequency = 27MHz, TV-clock frequency = 13.5MHz
R=6m, P=2m

a TV-FIFO = 16 stages with 8 to write 8 to read .

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CRT-FIFO = 16 stages with 8 to write and 8 to read
2xCRT-FIFO-fills + TV-FIFO-empty < 2x16 CRT-dotclks=16 TV-dotclks=1185ns
2x(R+7P) + R+7P + 3m = 3R+21P+3m=18m+42m+3m = 63m < 1185ns
mclk-period < 1185ns/63 = 18.8ns -> 53MHz min mclk frequency

b. TV-FIFO = 32 stages with 16 to write and 16 to read.
CRT-FIFO = 16 stages with 8 to write and 8 to read
4xCRT-FIFO-fills + TV-FIFO-empty < 4x16 CRT-dotclks=32 TV-dotclks=2370ns
4x(R+7P) + R+15P + 5m = 5R+43P+5m=30m+86m+5m = 121m < 2370ns
mclk-period < 2370ns/121 = 19.58ns -> 51MHz min mclk frequency

c. **CRT-FIFO = 32 stages 16 to write and 16 to read @ 27MHz**
TV-FIFO = 16 stages 8 to write and 8 to read @ 13.5MHz

CRT-FIFO-fills + TV-FIFO-empty < 32 CRT-dotclks=16 TV-dotclks=1185ns
(R+15P) + R+7P + 2m = 2R+22P+2m=12m+44m+2m = 58m < 1185ns
mclk-period < 1185ns/58 = 20.43ns -> **48.9MHz min mclk frequency**

Please note that Nordic already has 32 (or 36 stages of CRT FIFO - MVA FIFO) and 24 stages of FB-FIFO (write + read). So if we use all the buffering area available we can meet case c requirements and run direct live video at 48.9MHz mclk.

d. CRT-FIFO = 24 stages (12/12)
TV-FIFO = 12 stages (6/6)
CRT-FIFO-fills + TV-FIFO-empty < 24 CRT-dotclks=12 TV-dotclks=888ns
(R+11P) + R+5P + 2m = 2R+16P+2m=12m+32m+2m = 46m < 888ns
mclk-period < 888ns/46 = 19.3ns -> 51.8MHz min mclk frequency

B. 4:1:1 YUV Bandwidth Requirements

a. CRT-FIFO = 24 stages (12/12)
TV-FIFO = 12 stages (6/6)
CRT-FIFO-fills + TV-FIFO-empty < 32 CRT-dotclks=16 TV-dotclks=1185ns
(R+11P) + R+5P + 2m = 2R+16P+2m=12m+32m+2m = 46m < 1185ns
mclk-period < 1185ns/46 = 25.7ns -> 38.8MHz min mclk frequency

Because 3x32bit house 8 pixel data, it is advisable that the number of stages in the FIFO-s are a multiple of 3 for 4:1:1.

For 4:1:1 YUV, the picture quality is not that good as for 4:2:2, the control requirements are harder to meet, the filter on U and V is expensive, but the bandwidth requirements are easy to meet.

4.5.1.5 Covering the Memory Refresh and CRT-FIFO Prefetch Time

During each horizontal non-display time, Nordic executes memory refresh (normally 3 with an option of 1 - all random cycles), h/w icon and CRT-FIFO prefetch cycles.

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At that time the TV data comes at normal rate and has to be stored in the TV-FIFO. Let's see how long it takes to execute all these cycles.

a. With reference to case A.c. 4.5.1.4
(4.2:2 YUV the case that meets bandwidth requirements at 48.9MHz mclk)

x. CRT-FIFO = 32 stages, 3 refreshes, h/w icon 64x64x2 (4 h/w icon cycles)
R+31P + 3R + R+3P + 3m = 5R+34P+3m=30m+68m+3m=101m < 1185ns
-> m < 1185ns/100m=11.7ns -> min mclk freq. is 85MHz
(off by about 42mclks to get to 50MHz mclk).

y. CRT-FIFO = 32 stages, 3 refreshes, h/w icon but prefetch 16 CRT-FIFO stages
(no need to fill the FIFO at the beginning of the line).
R+15P + 3R + R+3P + 3m = 5R+18P+3m=30m+36m+3m=69m < 1185ns
-> m < 1185ns/69m=17.17ns -> min mclk freq. is 58.2MHz

z. CRT-FIFO = 32 stages, 1 refresh, h/w icon but prefetch 16 CRT-FIFO stages
(no need to fill the FIFO at the beginning of the line & use extended refresh DRAMs).
R+15P + 1R + R+3P + 3m = 3R+18P+3m=18m+36m+3m=57m < 1185ns
-> m < 1185ns/57m=20.78ns -> **min mclk freq. is 48.1MHz**

This case meets the minimum requirements for non-display time buffering.

b. With reference to case B.a. 4.5.1.4
(4:1:1 YUV the case that meets bandwidth requirements at 38.8MHz mclk)

x. CRT-FIFO = 24 stages, 3 refreshes, h/w icon 64x64x2 (4 h/w icon cycles)
R+23P + 3R + R+3P + 3m = 5R+26P+3m=30m+52m+3m=85m < 1185ns
-> m < 1185ns/85m=13.9ns -> min mclk freq. is 71MHz
(off by about 26mclks to get to 50MHz mclk).

y. CRT-FIFO = 24 stages, 1 refreshes, h/w icon but prefetch 16 CRT-FIFO stages
(no need to fill the FIFO at the beginning of the line & extended refresh DRAMs).

R+11P + 1R + R+3P + 3m = 3R+14P+3m=18m+28m+3m=49m < 1185ns
-> m < 1185ns/49m=24.18ns -> **min mclk freq. is 41.3MHz**

Case b.y will do it for an mclk frequency above 41.3MHz.

Note. If required, we could disable the h/w Icon and h/w Cursor when in full screen live video from Video Port.

Conclusion on Video Port Cheap System Solution

It is possible to achieve a minimum cost mother-board solution for full screen 640x480 30fps live video by interconnecting directly a digital TV decoder to Nordic Video Port under the following conditions:

1. **Prefetch only half CRT-FIFO instead of the entire FIFO**
2. **Do one refresh per line (eventually use extended refresh DRAMs)**
3. **To display 4:2:2 YUV use 32 CRT-FIFO stages and 16 TV-FIFO stages (between CRT-FIFO and MVA-Buffer we have enough storage now, but it has to be reconfigured). Minimum memory clock frequency is 48.9MHz**
4. **To display 4:1:1 YUV use 24 CRT-FIFO stages and 12 TV-FIFO stages. Minimum memory clock frequency is 41.3MHz.**

Under the same conditions, it is possible to display live video in a window with a 640x480 TFT panel, but the image has to be scaled-down and filtered with PX0070 or PX0072 - a more expensive solution. Also, during the actual live video display time, CPU and BLT will get very few cycles. This is not a factor with full screen live video as the CPU does not need to access the Video Memory at that time.

The question is now: how much cheaper is this solution relative to a full screen TV with overlay ? Sasha is working on a cheap solution with overlay.

Minutes of the Meeting on MM in Nordic in Nov. '93

With D.Keene, Keith, Del and Nordic Team on

- Video Port with 32bit memory is bwth. limitted. It is not a good solution for 32bit bus - better use Overlay or Sashapak.

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4.6 On WavePort Architecture and Audio Driver

Starting from Dave Keene's WavePort Specification, Rakesh, Sasha and Vlad came-up with some ideas which could greatly simplify the design work for WavePort, reduction the complexity and the number of gates of the WavePort.
We'll start with the small issues and move towards more important issues.

4.6.1 AUXS1 and AUXS2 Pin

A. Dave proposed to share this pin with PDN (Power Down) WavePort Pin and configure it as AUXS2 when using 4231S.
We noticed that 4231S does have a PDN pin which we'd like to use to save power
We'll put AUXS2 on another pin.

B. Dave proposed to have a fully programmable location for AUXS1 and AUXS2 CPU I/O map with a default at 530H and 388H. This is costly (4 registers and fast comparators) and very difficult to design at required speed: will slow down address range decode for I/O a lot affecting command to command parameters.
We suggest to have a fix address for these ports: 530H and 388H.
Two register bits (one per address) can disable the chip from answering to these I/O addresses.
If we are not sure where to place these ports, we can leave it as a metal option for future modification or have one more alternative for each, but the address should be fix for fast decode.
GR58:GR5B are no longer needed if this option is accepted. We'll need two bits to disable 530H and 388H address decode and eventually two other bits to select other two alternate I/O addresses. We should always decode 16 addresses: 530:53F and 388:397 (not 4 or 16)

4.6.2 WavePort R/W Buffer Location and Size

To simplify the h/w and reduce verification work-load , WavePort R/W Buffer Size should be fix: 32KB for each, enough for at least 180msec of operation -> 90msec for half buffer. Every 90msec the CPU will have to fill and/or empty half Audio Buffer (write or read respectively).
It is also possible to place the WavePort memory buffer in a fix memory location, common for both desktop and portable architectures. We could place it in Memory in the upper part
(in high address area), just before the h/w cursor. If the h/w cursor takes the upper 16KB of the memory, we could use the next 64KB for the WavePort buffer.
Going down in memory, in Nordic we'd place the h/w icon in the next 16KB (only 4KB needed now... but leave some room for expansion) and the Half Frame Buffer for monochrome and color panels in the next 32KB and 96KB respectively.

Total:
96KB for CRT/TFT/SS STN panels,
128KB for monochrome panels and
192KB for dual scan color STN panels.
out of 1MB or 2MB memory available.

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When the memory is expanded, all these fix components should move automatically in the upper side (towards the end of memory).

This places the WavePort buffer at:

- **for 1MB** of memory by 32 (256Kx32 -> 00000:3FFFF) **3B000:3EFFF**
- **for 2MB** of memory by 32 (512Kx32 -> 00000:7FFFF) **7B000:7EFFF**

If we adopt this solution, GR43 is not needed.

4.6.3 On Host Access to WavePort Buffer

In order to ensure independence between the Graphics s/w Driver and the Audio Driver, taking into account AVGA limitation of no CPU accesses during BLT operation, Dave proposed a separate path for WavePort Host Accesses. This involves a separate 4 stage by 32bit write and read buffer and separate arbitration for the Audio cycles. The buffer is shared by WavePort read and write operations and an I/O to an extension register bit is needed in order to switch from a read operation to a write operation or vice-versa.
Dave also proposed that the host address be dependent on GR6 CPU address map bits such that the video and audio address maps don't overlap.
Please note that this approach prevents debug with a Hercules card when in graphics.

In the following an alternate scheme is proposed:
- There is one register bit that enables WavePort memory write accesses and one register bit that enables WavePort memory read accesses. When one of these bits is asserted ,the chip expects only host accesses for the WavePort: the host address will be automatically translated to a memory address inside the WavePort buffer. The access will be fully linear, 32bit only, **graphics mode independent** (like in extended 8bit/pel). The Graphics block will be forced to this mode and all planes will be automatically enabled. On the Host side, the WavePort buffer will be placed always at A000:0000 - A000:FFFF -> 64KB with 32KB for read buffer (the upper side) and 32KB for write buffer (the lower side of this 64KB segment).
- The CPU Data Path is the same as for any other CPU cycle: no special FIFO, no special arbitration are required. The Audio Driver and The Graphics Driver communicate through interrupts: There is an interrupt for BLT completed (Dave's idea when presented with this proposal) and an interrupt for Audio Buffer Full (or Audio Transfer Completed). When the BLT is completed, if Audio is enabled on the chip, the BLT Completed interrupt allows the Audio Driver to check if there is any need to service the Audio and vice-versa. If possible, the Graphics driver should restrict the extent of the BLT operations to less than 160msec or so (leaving at least 20msec to start filling the WavePort buffer).

- There is no on chip CPU WavePort address generation. The CPU address in the range A0000:AFFFF (incremented by 4 every cycle for DW accesses) is translated to physical memory address 3B000:3EFFF. If host side WavePort pointers are used, the host address is latched and translated for comparison with the Codec pointers generated on chip

Adopting this scheme would greatly simplify the extent of the design and verification work for WavePort: 8 weeks at least will be saved.

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4.6.4 On the Audio Driver

Dave proposed that the Graphics Controller has h/w to compare the WavePort pointers and generate interrupts. The Codec pointers are I/O readable by the host as well as several buffer status bits (Audio-IN buffer Full, Audio-In buffer half-full, Audio-Out buffer half-empty, Audio-Out buffer empty,....).

Nordic-1M will support Dave's proposed interrupt driven interface.
In this case the only important difference for the driver will be that it will have to generate the buffers address and not rely on the h/w to do this (Dave suggests that CPU will write and read always the same address A000:0 or B000:0 and the actual address on the host side is generated on the chip - we sugest to change this and let CPU generate the address).

Because CPU has to wait untill the a BLT operation is complete and the BLT has to wait for Audio buffer to be full or the transfer completed, two more interrupts are needed: BLT operation completed and Audio transfer completed. This way the Audio Driver and the Video driver can communicate with each other.

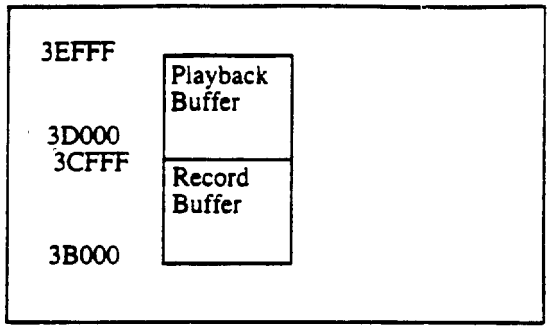
The Read and Write CPU side pointers will be generated by latching the last read and write WavePort CPU address (lower 16bits only) after translation to physical memory address. Comparators on the host and codec pointers will generate Buffer Full and Buffer Empty signals.

Jeff Ort drew our attention to the fact that the driver transfers a certain size block and needs an interrupt anytime half of what was placed in the Audio buffer was read by the Codec (the play-back buffer is half empty). To make things simple for the h/w, we propose to give Jeff an interrupt when the CODEC side playback buffer read pointer reached a preprogrammed value, value the driver programs everytime it transfers a block of a certain size in the playback buffer. For instance, if the driver put 2KB of data in the playback buffer starting from phisical address 3B000 (host address A000:0) and wants on interrupt when the first 1KB was read by the CODEC, it should program 3B0FF in the playback interrupt register, as 1KB = 256 32bit words. The register will have 16bits and the driver will program B0FF to get an interrupt when the CODEC reads 3B0FF or 7B0FF playback buffer address.

Similarly, on the record side, there will be a programable interrupt on the CODEC side to be used to tell the driver when the Record buffer is half full.
So we'll need two 16bit indexed registers for these programable interrupts. For each WavePort interrupt we also need a status bit to say that the interrupt happened, an enable bit to enable the particular interrupt. As Dave proposed, GR4D is the Interrupt Status register but bits [0] and [2] will be the programable interrupts status bits. The interrupts and the status bits will be cleared after this register is read (automatic clear in h/w).

We could use registers GR58:5B as high and low byte for the programable interrupt

on Record and Play-back buffers respectively.



The write-buffer (or Audio-Out =the one in which the CPU writes) is empty one WavePort write cycle to memory after

WRBUF-Write-Pointer = WRBUF-Read-Pointer+1

(this condition will activate set an empty flag).

The write-buffer is full one WavePort write cycle to memory after

WRBUF-Read-Pointer = WRBUF-Write-Pointer + 1

The same equations apply to the WavePort read-buffer, only this time the read-pointer is on the host side and the write-pointer on the Codec side.

Shouldn't be a Audio-Out buffer full interrupt and a status bit for it?

Threshold detect mechanism will require to increment host pointers, but the CPU is supposed to read this pointer and generate the proper address when going above the threshold. The idea of the threshold detector is that by incrementing the Audio-In read pointer everytime the write pinter is incremented if the Audio data is under the threshold value, the delta between the pointer remains the same and the buffer does not fill in with sub-threshold value. This was true if the half-full detection had been generated based on the delta between pointers. After talking to Dave, there are some clarifications to be made on the threshold detect mechanism for record:

For one record sesion, this is a one time event mechanism: if the threshold was passed once after being enabled, its effect is lost - even if the sound level goes below the threshold the record buffer read pointer works normally. The threshold will help only in the initial stage before the first actual voice pattern is detected, but it does not have any effect after the intitial triggering event - once the sound leved passed once the threshold.

With this driver approach, GR43 and GR58:5B will not be needed.

Five registers are saved. Twenty One register are still needed (plus two reserved = 23).

Another possible approach for the driver uses extensively the Vertical Interrupt

In this case every Vertical Interrupt, the Audio Driver reads the Codec side pointers, compares them with the Host side pointers, the driver generates based on the CPU address it last wrote to or read from and makes its own decisions. The driver will also check the BLT completed status bit.

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In other words, every 18msec (@60Hz), on the Vertical Interrupt the Audio driver can process data from the Codec pointers, calculate based on the last address if the WavePort buffer is full or empty and decide how many more WavePort accesses to execute. As at least 180msec worth of data is in a full Waveport Buffer, the driver has 6 opportunities to find out that the buffer is empty and start filling it before half WavePort buffer is empty. On chip h/w is still needed to stop sending data to the Codec after sending all data and to read all data from the WavePort read memory buffer on the host side. Because the CPU decides when the buffers are full, half full or empty there is no need for registers for the pointers on the CPU side, but the CPU address will still be latched to generate the host side pointers.
The "BLT operation completed" and the "Audio transfer completed" interrupts are needed anyway bacuse we share the data-path for BLT and CPU cycles.

By adopting this mechanism in the driver, no special h/w is needed to preserve pointers on the Host side, to compare the Host side pointers (read and write) with the Codec pointers and to generate interrupts and status bits. The only interrupts needed are Standard VGA Vertical Interrupt as a time base, BLT completed Interrupt and Audio Completed interrupt.

We can still implement the threshold detect.

GR44,GR45, GR48 and GR49 won't be needed.
Nine registers are saved. Seventeen register are still needed (19 with two reserved registers).

Conclusion
The above proposal, if OK for the WavePort driver, would reduce significantly the amount of design and verification work on the WavePort. This document was written in order to get feed-back and reach an agreement ASAP. Our goal is to have a unique s/w model for the WavePort, but we'd like to cut the amount of work if possible.

Rakesh's notes on the discussion with Jeff Ort and Dave Keene, 11/03/93

1. Since in Nordic, we do only 1R + 1P always, what happens if the bit is disabled for the host read at a time when ODD number of FIFO stages are filled? At Present we assume that while recording some SILENCE is inserted at the end of recording session and thus we can disable the bit as soon as driver disable it.
Jeff and Dave Kenne both agree that even though no SILENCE is inserted at the end, it is still valid to disable the memory transfer immediately after the bit is negated.

2. Threshold Issue.
If threshold mechanism is enabled, we keep putting the samples into the AUDIO

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BUFFER.
If the data in buffer is more than the programmed value (GR74 and GR75) and input data crosses the threshold value, the interrupt is generated immediately. But if data amount is less than the value in the registers GR74-GR75 and input data has crossed the threshold value then we wait till it crooses this value(GR74 and GR75) and then interrupt is generated.

Dave's specs talk about two pointers on the RECORD buffer, one for the CPU read and another for CODEC write. Both of these pointers are accessable by the CPU in his specs. So he suggests that before the threshold is met we should fill up the buffer till half full condition. Once the buffer is half full, any more writes to RECORD buffer by the CODEC should increment both of these pointers. In this case whenever the threshold is met we are guaranteed to have some information about the history of audio samples just before the threshold is met. At the time when threshold is met the generated interrupt should tell CPU that CPU can read the data from the location pointed to by CPU read pointer.

But in NORDIC, the CPU read pointer is not accessible by CPU. Thus we keep putting the samples in the RECORD buffer and not generate the interrupt till the threshold is met even though we might pass the programmed value for the interrupt. At the time when the threshold is met, the interrupt is generated if CODEC write pointer is past programmed number. If threshold is met before the CODEC write pointer passes the programmed number, we wait till it does cross the programmed number. So the driver for Nordic should store the CPU address at the time when the threshold mechanism is enabled. So at the time of interrupt CPU can calculate the amount of samples in the BUFFER.

3. Independent control for IN / OUT mono / stereo .
Codec read and write are independently controllable for mono or stereo input / output

4 Jeff agrees with the usage of OFFSET register GR9 to generate the CPU side adress for audio, instead of NORDIC generating the adress automatically.

Minutes of 11/20/93 Meeting with Keith, Del and Dave Keene

1. We need to check if WavePort accesses work with linear addressing (SR7 - aperture register).
2. Make sure that OverRun Status is there even if OverRun Interupt is disabled.
3. Enable looking for threshold only after you reach the given address.
4. Bit GR6E[6] should move to GR6E[3].
5. Talk about programable address for AUX1 and 2.
6. Check out arbitration for audio throughly.
7. Check overrun interrupt during threshold... always programmed interrupt after crossing threshold. ?? Rakesh may understand this!!

4.6.5 Registers specs for the AUDIO of NORDIC1-M.

GR60 Wave Port Control 1

7. Reserved
6. Reserved
5. Enable audio for host accesses.
4. Select 4215
3. Stereo for reciever (i:e STEREO CODEC)
2. Stereo for transmitter (i:e STEREO NORDIC)

1:0 Data Format select

- 00 16 bit
- 01 8 bit
- 10 4 bit
- 11 reserved.

GR61 Waveport control 2

7. Reserved
6. powerdown control ---> 0 will force low on PDN.
5. Enable command mode. 4215 must have been placed in COMMAND mode by forcing low on D/C* pin.
4. input level in SDI in command mode.
3. output level on SDO in command mode.
2. output level on SCLK in command mode.
1. output level on FSYNC in command mode.
0. output state of D/C* pin.

GR62 Input Audio Threshold setting.

7:0 Available only for 16bit mode. Only +ve data is compared i:e if msb of left data is 1 no compare is performed.

GR65

7. Enable Threshold detect mode.

6:0 Reserved

GR66 7:0 Audio Input Codec write pointer low byte

GR67 Audio Input Codec write pointer high byte

7. Enable input from codec to audio buffer.

6:0 Audio Input Codec write pointer (low 7 bits of 15 bit pointer)

GR6A 7:0 Audio Output Codec Read pointer low byte

GR6B Audio Output Codec Read pointer high byte

7 Enable output to codec from audio buffer.

6:0 Audio Output Codec read pointer (low 7 bits of 15 bit pointer).

GR6C : Interrupt Control.

7:6 Reserved.

5. Standard VGA Interrupt disable.
   - 0 --> Allow VGA interrupt
   - 1 --> Disable VGA interrupt.

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4:2 Reserved.
1. Audio Input interrupt control -----> DURING RECORD SESSION.
0 --> disable this interrupt source.
1 --> Enable input buffer full OR programmed full interrupts.
0. Audio Output interrupt control -----> DURING PLAY SESSION.
0 --> disable this interrupt source.
1 --> Enable Output buffer empty OR programmed empty interrupts.

GR6D : Interrupt Status.

Indicates any active enabled interrupt. Reading this register will clear the interrupt state and reset the status. No effect on the standard VGA interrupt status or interrupt.

For All of the following 1 in the bit means PENDING INTERRUPT.

7:6 Reserved.
5. Standard VGA Vsync interrupt (state of 3C2(7)).
4. Reserved.
3. Record Buffer FULL (OVERRUN).
2. Record Buffer PROGRAMMED FULL.
1. Play Buffer EMPTY. (UNDERRUN)
0. Play Buffer PROGRAMMED EMPTY.

GR6E : AUX1 and AUX2 control

7 Enable Aux Sel 1 low-true output on adress match 530-53Fh.
6. Enable Aux Sel 2 low-true output on adress match 388-397h.
5:0 Reserved.

GR6F: Code status.

7:4 Reserved
3. Timer status (ADI) time slot 6 bit 7
2. overrange (OVR) time slot 7 bit5
1. PIO1 input status. time slot 7 bit 7
0. PIO0 input status. time slot 7 bit 6

GR70: Codec control DWORD from Nordic to codec. byte D7:0
GR71: Codec control DWORD from Nordic to codec. byte D15:8
GR72: Codec control DWORD from Nordic to codec. byte D23:16
GR73: Codec control DWORD from Nordic to codec. byte D31:24

GR74:75 Interrupt value for audio IN buffer.

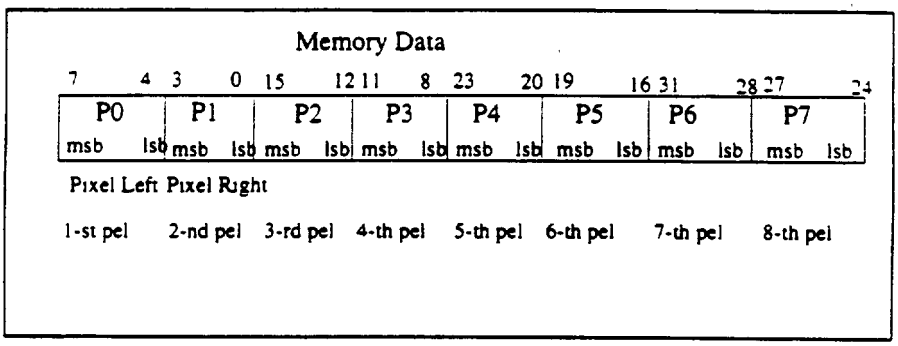
When CODEC reaches the programmed adress -1, an interrupt is generated during the record session.

GR76:77 Interrupt value for audio OUT buffer.

When CODEC read pointer reaches the programmed adress -1, an interrupt is generated during the play session

4.7 Four Bit per Pel Packed Format

To fully support Windows Chicago, Nodnc-1M should support 4bit/pel packed format. CPU will be able to write only 8bits or more at a time. To modify only 4bits the CPU will do read modify write and mask four bits (bring them from CPU latches).
The following picture shows the actual format:



In order to get Nordic-1M to support this mode, we need to place the VGA Video Data Path in 8bit per pixel mode with pixel doubling (mode 13) but disable the mechanism that concatenates adjaisant 4bits to make one 8bit pixel displayed twice (at a divided by two RAMDAC VCLK) and disable as well dividing by two the RAMDAC VCLK.

On the CPU side chain 4 address scrambling should be disabled and data should be shifted right like in extended 256 color modes.
In nordic-regs-rev9.lst we assigned SR26[0] to enable this graphics mode.

4.8 Robin's Ideas on High Resolution Panels for Nordic-1M

Nordic's objective is to be able to center and fill the screen on 800x600 panels and to center an 800x600 picture on 1024x768 panels. The main focus is 800x600 panel support TFT and dual scan STN.
In TEXT there will be three options:

- horizontal and vertical centering with 9x16 fonts (disable 640x480 force to 8dots font)
- auto-expand the font to fill the screen
- special font to fill the screen

In Graphics there will be tree options:

- horizontal and vertical centering
- use a driver to run at maximum resolution
- automatic expand to 800x600 (only if s/w verification shows it being OK).

In all cases horizontal and vertical options will be decoupled (different enable bits)

Here's a list of what needs to be done:
a. Expand horizontal and vertical centering capability from 640x480 to 1024x768

b. Shadow all H/V CRTC registers except HDE and VDE.
The vertical registers are shadowed now, but the horizontal registers are not.
We need to shadow CR0, 2, 3, 4 and 5. These registers will be written by the BIOS at POST. The same mechanism to enable/disable vertical shadow is used to enable/disable horizontal shadow.

c. Support 10dot character-clock and CRT-FIFO-Read / Shift/Load (Video-Serializer Load). Now only 8dot and 9dot character-clocks are supported. For smooth-scrolling the pel-pan has to be expanded to 10 pisitions (0:9).

d. TEXT auto-expand will be as follows:
- horizontal: replicate the last pixel once for 9 dots wide fonts and twice for 8 dots wide fonts.
- vertical: replicate all odd scan-lines

TABLE 3. Font Expansion for Different Panel Sizes

Font-Size/Panel-Size	480	600	768
8x14	8x19	10x21	10x21 + center
8x8 with scan-ln. doubling	8x19	10x24	10x24 + center
9x16	8x19	10x24	10x24 + center

Please note that in text vertical expansion is done on the scan-line counter as well as the vertical display line counter, but it does not affect the vertical non-display line counter.

e. Graphics modes expansion (to be implemented only after s/w verification)
Graphics expansion is less important as it is assumed that important applications will run at maximum panel resolution with a driver.
We'll need to supply drivers for many applications with high res. panels !!
Vertical expansion:.
- 350lines -> replicate all odd scan-lines
- 400lines -> replicate all odd scan-lines
- 480 lines -> replicate every 4-th line

Horizontal:
- center
- duplicate every 4-th pixel
- ~~duplicate every 4-th pixel with diagonal shift~~

(~~scan-line 0 -> 1st pel, scan-line 1 -> 2nd pel, scan-line 2 -> 3rd pel, scan-line 3 -> 4th pel~~
~~...~~

f Please note that when character clock is expanded to 10 dots, h/w cursor also needs to be positioned at 8 or 9, so it needs one more bit of fine position.
SR2E[0] will be the msb of h/w cursor (default zero) to be used in this case.

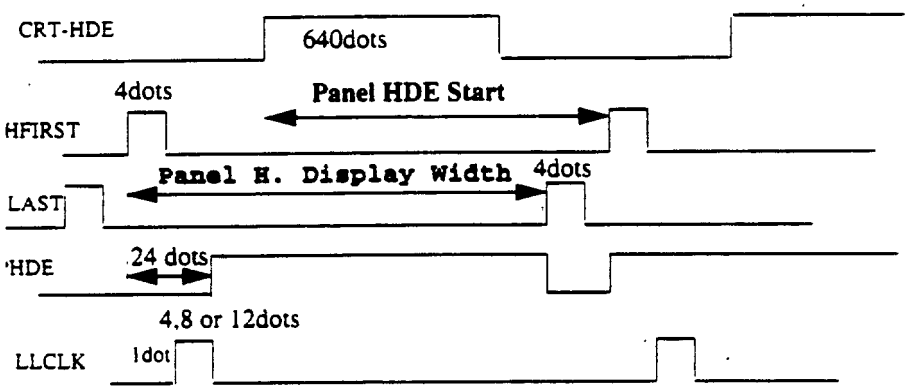
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4.8.1 Panel Horizontal Timing Control in Nordic

If in Terminator all panel timing is based on HSYNC and VSYNC programing, in Nordic it will be independent of HSYNC and VSYNC programming.

Horizontal Timing for 800x600 panel with 640x480 picture:



Registers for Panel Horizontal Timing Control

This set of four registers are used to generate horizontal panel timing with 640x480 or 800x600 panels and to center horizontally a 640dots or 720dots picture on an 800x600 panel.

CR40 No Center Panel HDE Start Register

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. This register is used to program Panel Line Clock Start and Panel Display Enable Start with both 640x400 and 800x600 panels any time no horizontal centering is needed.

CR41 Panel HDE Start Register to Center 720 dots

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register

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will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 720 dot mode (text or graphics - RIX mode only) is centered on an 800x600 panel. If horizontal expansion is on CR40 is used.

CR42 Panel HDE Start Register to Center 640 dots

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 640 dot mode (text or graphics) is centered on an 800x600 panel. If horizontal expansion is on CR40 is used.

CR43 Panel HDE Dot-Clock Skew Control Register

[7:6] Panel Line Clock Width:
- 0 = 4 dot-clocks
- 1 = 8 dot-clocks
- 2 = 12 dotclocks
- 3 = reserved

[5:4]CR42 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

[3:2]CR41 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

[1:0]CR40 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

By programming this skew, it is possible to compensate internal delays on Panel HDE for diferent types of panels. If all delays are matched the skew fields should be zero to

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align with character clock.

Automatic switching between these three registers will be done based on CRTC and Sequencer programming and the type of panel used
(640x480 or 800x600).

CR 44 Horizontal Panel Display Width Register

The value in this register is expressed in 4 dot-clocks (never divided by two).

[7:0] Panel Display Width in hex expressed in 4 dot-clock chunks. As it is used to compensate for internal delays, this value is close but not exactly 640/4 or 800/4.

4.8.2 Horizontal CRTC Registers Shadowing

In order to run VGA programs on 800x600 panels, Nordic needs to shadow the horizontal timing registers except the display enable end, which is application dependent.
(T1 has shadows only for horizontal total.)
This is because all horizontal timing registers but HDE have to be set-up for 800x600 in order to run an 800x600 panel. Symulscan with 800x600 panels runs even the CRT as an 800x600 display in all graphics modes.
In T1 as well as in Nordic, vertical panel registers are mapped at R2x, R3x,.... accesible when CR2D[7] = 1. In nordic these registers remain there.
IN T1 there are two registers: **R0x and R1x** which represent HTot shadows, accessible with **CR2D[7]**. They are no longer used in Nordic, **but there is a replacement for them, independent of CR2D[7].**

In Nordic, H Total, H Retrace Start and End, H Blank Start and End are shadowed. Each entity has two values to chose from: a value for dclk/2 and a value for dclk not divided by two. The effect selection is done automatically based on SR1[3] value, but for access there is a selection bit: CR2C[4] to control which of the two sets of registers gets read or written.

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Here is a summary of the horizontal shadow registers and its controls:
CR2C[5] write protect for horizontal shadow:

1 -> write both the shadow registers and the corresponding standard VGA registers fields (some registers are not accessed entierly but only in their timing part)
read back the shadow registers

0 -> write only the standard horiz. timing VGA registers (the shadow registers are write protected). Changing onlt the value of these registers does not have any effect over the CRTC timing.
read back the standard VGA horiz. timing registers

CR2C[4] Select the set of horizontal timing shadow registers to be used (low rez or normal). This bit is reutilsed from T1: it was low power RAMDAC mode - tie now the logic L) .
0 -> select Ry for access
1 -> select Rz for access

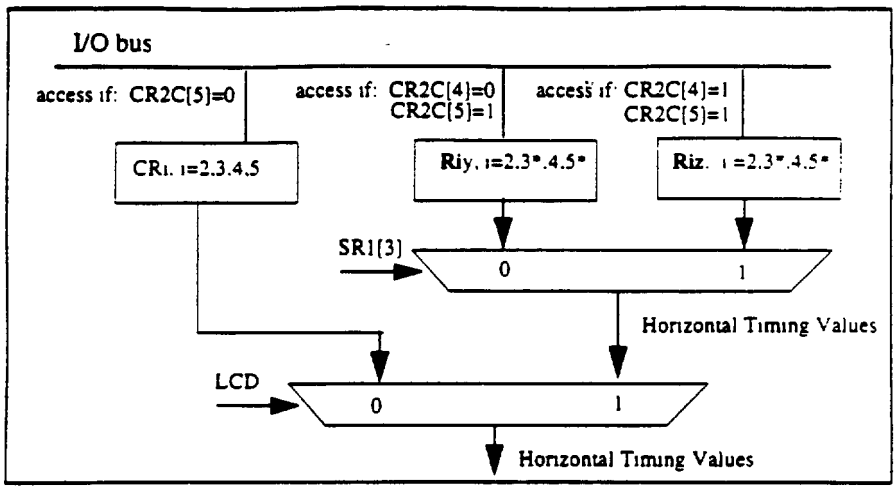
To diferentiate from the Rx registers which still exist as in T1, and are vertical panel registers, we'll call the two sets of horizontal shadows mapped in the same address space Ry and Rz (Ry = normal, Rz = dclk/2 case)
The effect of Ty and Rz is controlled by SR1[3] (dclk/2 bit).

The Horizontal Timing shadow registers are:
R0y,z R02y,z R03y,z (only lower bits) R04y,z R05y,z (only lower bits)

When CR2D[7] =1 we can access only the panel registers: R2x,... RBx. In this case we cannot access either the VGA standard registers or the horizontal timing shadow registers. **Please note that R0x and R1x are reserved in Nordic. Their function is replaced by R0y,z.**

Standard VGA CR0,2,3,4,5 horizontal timing registers (only the timing fields) do not have any effect on the CRTC: only the shadow registers have effect.

Note: Vertical Blank registers CR15 and CR16 are only write protected in T1 - not shadowed. This seems to be an error... so they should be shadowed in Nordic.
When using blank as overlay, DEn becomes blank and the shadow registers create the overlay both horizontally and vertically, but they are no longer write protected by CR2C[3] or [5]... As in 5428, they will not be write protected at all as the overlay is used only under MS Windows which is a controlled environment.



4.9 TV-Out Support in Nordic-1M

Nordic's objective is to be able output data to an analog TV Encoder chip thus supporting a cheap way of displaying on a TV. The main application is graphics, probably under windows, TV display and tape-recordig are of interest.

Nordic will run in a locked interlaced mode at 13.5MHz for NTSC and it will use the LCD panel supprt shadowing mechanism (the shadow Horizontal and Vertical CRTC registers) to prevent the application from changing the CRTC set-up. Even the dotclock frequency will be locked. Horizontal and vertical display enable will be open to the application.

Nordic will provide analog RGB, Composite SYNC, NTSC/PAL and TV-ON to the TV encoder. AD720 and MC1377 analog TV encoders that accept RGB input will be supported directly (with no glue logic).

Nordic will have edge skew h/w on the appropriate signals in order to meet the TV Standards timing requirements .

In this mode Nordic will not be able to run a panel or a CRT monitor... no simulscan supported with TV-OUT. But the same system will display on a panel, a CRT monitor or a TV with minimum glue logic.

Digital TV Encoders are not be supported.

All standard VGA modes plus 640x480 8bpp can be supported, though special set-modes are required, as they all run interlaced. I suspect that we'll end up supporting only a few important modes. Should we compress text to 8dot wide fonts?

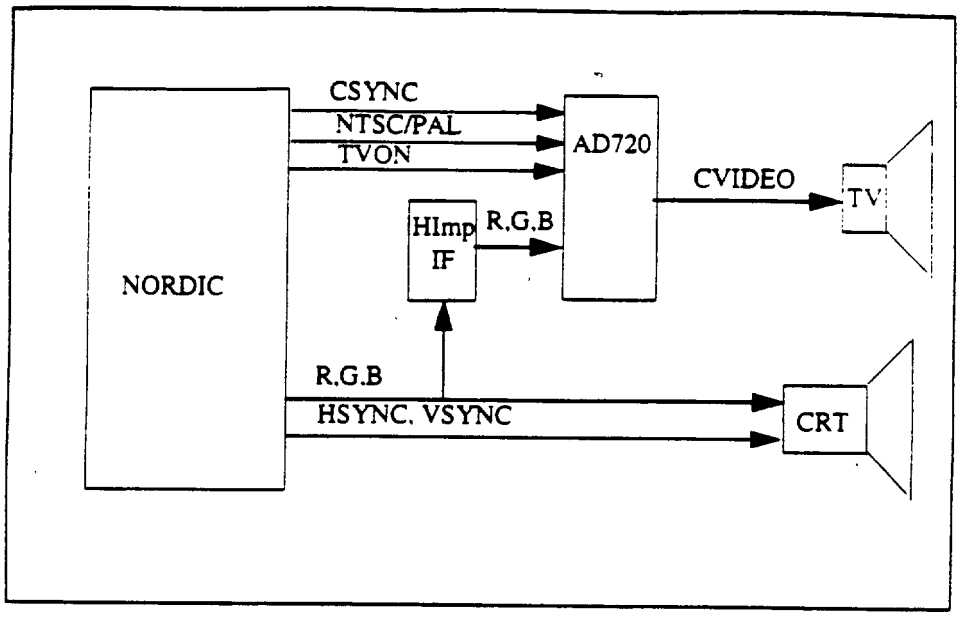


TABLE 4. Data on TV Standards

PIXCLK	Multiples of Line Frequency	Active Pixels per Line	Field Rate
12.2727MHz	780xFH	640	60Hz
14 75MHz	944xFH	768	50Hz
13 5MHz	858xFH	720	60Hz
13 5MHz	864xFH	720	50Hz

Signals to be supplied by Nordic:
- CSYNC = Composite SYNC signal
- NTSC/PAL = a programable output selecting the TV Standard NTSC (1) or PAL (0) The value of CR30[2] comes out on the pin.
- TVON = H for the TV Encoder to be ON, L for it OFF. The value of CR30[3] comes out on the pin. If CR30[3] =0, CSYNC and NTSC/PAL pins are L.

In Nordic-1M all these signals will come out to the panel pins when a certain configuration bit is enabled.

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Vertical Timing

Vertical Blank and the appropriate CRTC registers are programmed to generate Blank which in TV case is the actual Display Enable.

For NTSC program 9 lines of VBlank.

For PAL program 7 lines of VBlank. In h/w Nordic will generate 7.5 lines of VBlank in this case by delaying the trailing edge by 0.5 line.

Vertical Sync Registers will be programmed for Field Sync generation.

For NTSC program 3 lines.

For PAL program 3 lines and get 2.5 lines by delaying the leading edge by half line.

Horizontal Timing

Two basic pulses are generated:

- HREF1 = Horizontal Reference 1 which is HSYNC start with 64 dotclocks width
  CR30[1:0] controls the fine skew of this edge by increments of two dot-clocks.
- HREF2 = Horizontal Reference 2 which is a pulse marking the middle of the line between two HSYNC start edges. CR19[7:0] are used to program the start of this pulse.
  CR30[1:0] controls the fine skew of this edge by increments of one dot-clock.

Note that HREF1 and HREF2 skews are in sync: HREF2 skew is half HREF1 skew.
Horizontal Total is 858 dot-clocks at 13.5MHz for NTSC and 864 dot-clocks at 13.5MHz for PAL.

Composite SYNC Logic Equation is:

CSYNC = [(HREF1 + HREF2) & VS] trigg368dclk-pls + -> Field Sync (serration)
[(HREF1 + HREF2) & VS*&VB] trigg32dclk-pls + -> Equalization
[HREF1 & VB*] trigg64dclk-pls -> standard sync during display time

Where: VS is Vertical Sync programmed time
VB is Vertical Blank programmed time
* is a logic negation
trig32dclk-pls means: on the rising edge of this signal generate a 32 dot-clocks wide pulse.

There are three ways to connect the video encoders and the CRT. We are now in the process of deciding which one is the best:

1. The simplest way to connect the TV decoder is to assume that the CRT Monitor should not be hooked to the notebook computer at the time the TV is. In this case we can put a high resistance voltage divider (2KOhm) to get the required 0.7V or 1.0V full swing to the decoder. The 2KOhm voltage divider will not practically affect the 50 Ohm resistance on the CRT, when the CRT is hooked on. The disadvantage of this method is that it requires a CRT to be disconnected from the note-book computer when connecting a TV. The TV encoders get RGB input through an AC connection (a capacitor) so the DC source may be a high resistance.

The advantage is that it is simple and low cost.

2. There are no buffers or other resistors than usual. We control the RSET resistor value on the LM334 current source depending on the presence of the CRT Monitor hook-up or not. If the CRT Monitor is not hooked-up, we adjust IRef so that DAC-s full swing output voltage is 0.7V (or 1.0V) with a 150 Ohm load. If the CRT Monitor is detected to be hooked up, RSet will be left as it is now. The adjustment is done automatically with a transistor. This approach requires a programmable output (from Nordic or Core Logic) to control RSet value. The detection of the CRT Monitor presence is done by s/w the standard VGA way.

3. Put 50 Ohm load on the DAC output and feed it to the TV encoder and to an Analog Voltage Repeater that drives the CRT Monitor RGB lines. This way DAC output is always 0.7V full swing independent if the CRT Monitor is hooked to the notebook or not.

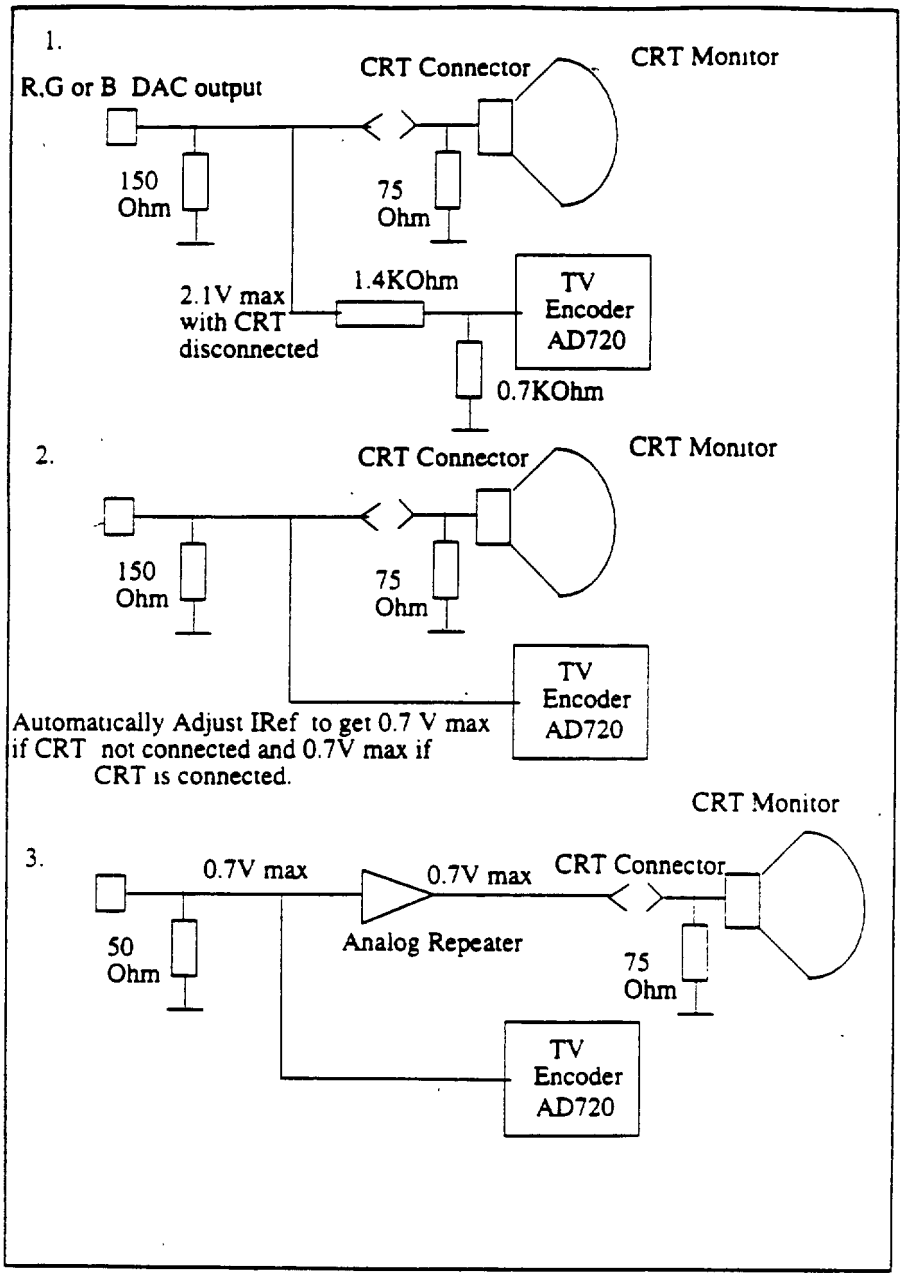
This approach works for AD720 but not for MC1377 which requires 1V full swing. With this approach the presence of the CRT monitor cannot be detected VGA style (incompatibility issue ?).

4. Leave the CRT path unehanged, except for a low resistor shunt added in series.Convert the constant current delivered by the DAC into voltage that is amplified to NTSC/PAL level depending on the type of encoder used. Requires fast operational amplifiers on each gun, but allows operation with or without CRT connected and color compare.

This looks to be the best scheme but it is also the most expensive. The op-amp can be used also as a filter to limit the spectrum and avoid cross talk in color monitors.

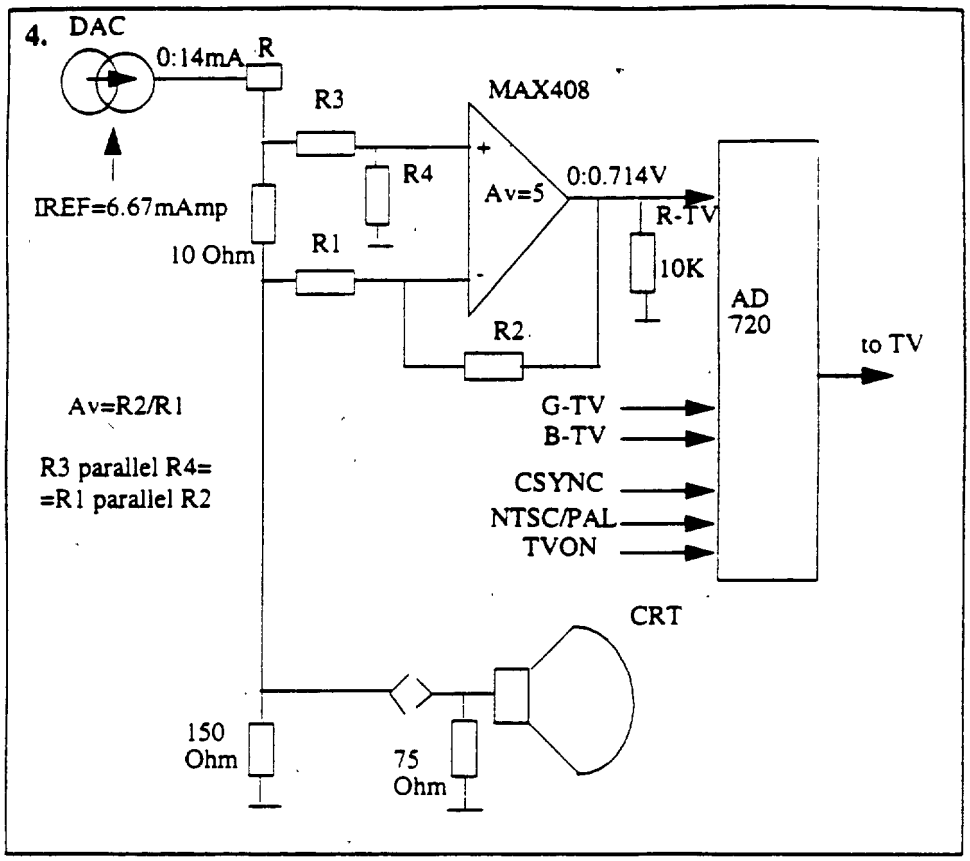
Three possible ways to connect an Analog PAL/NTSC TV Encoder to DAC output.

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4. DAC
0:14mA
R
R3
MAX408
R4
Av=5
0:0.714V
R-TV
IREF=6.67mAmp
10 Ohm
R1
10K
AD
720
R2
to TV
Av=R2/R1
G-TV
B-TV
R3 parallel R4=
=R1 parallel R2
CSYNC
NTSC/PAL
TVON
CRT
150
Ohm
75
Ohm

4.10 H/W ICON Support for Nordic-1M

Nordic-1M will support a h/w icon with the following features:
- Up to 4 64x64 Icons displayed at the same time as a vertical bar.
- All Icons move together and they are inedex by 64 scan lines.
  The Icon start reference point is top left corner.
- Horizontal Resolution is one pixel programed coarse as character clocks and fine as pixels exactly as a h/w cursor.
- Vertical Resolution is one scan-line.
- Each Icon has inependent display control for
  - icon number i enable for display (i=0:3)
  - display mode: 3colors + transpency or 4 colors
  - blink enable at text cursor rate (or half of it)
  - horizontal pixel doubling (extendes towards right)
  - vertical scal line doubling (extends down)
  - mamory map selection: two maps available per icon
- H/W Cursor goes on top of H/W Icon
- Icon memory model is and phisical address space are very similar to h/w cursor.
  Actually the icon resides in memory in h/w cursor area: Nordic supports half the number of h/w cursor maps 5428 does and uses the remaining space for icon maps. Eight 64x64 icon maps are supported: two for each icon we can display. Icon memory map assignment is fix.

H/W Icon S/W Model

Icon position will change at set mode if it is not compensated. BIOS should service the icon so that it keeps the position stable in all graphics modes: read current position and translate in the same position in the new graphics mode. The BIOS should have a call to set-up the h/w icon position and another call to control which icon is displayed and how

What we need:
a. Horizontal Start Position in character clocks and pixels
  Will be programmed exactly as h/w cursor at SR10,30,50,70,90,B0,D0,F0.
  (or SR "odd" "zero"). The upper 3 bits of index define the fine (vclk) position.
  SR2A[6] is the fine postion msb to be used with 9 and 10dots fonts.See 542X Reference Manual page 9-13, SR10 description.
Note: 1. If character clock or vclk change (8/9/10 dot cclk or vclk/2) the horizontal position should be adjusted.
  2. As with h/w cursor the horizontal and vertical position of the icon are synchronized. s/w writes the horizontal position first, but the new position effect takes place only after vertical position was updated.

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b. Vertical Start Position in scan lines.
  Will be programmed exactly as h/w cursor at SR11,31,51,71,91,B1,D1,F1.
  (or SR "odd" "one"). The upper three bits of index define the low order three bits

of position in scan lines. See 542X Reference Manual page 9-14, SR10 description.
How will Nordic know to program icon or cursor?
One bit will tell if icon is programmed instead of cursor. As the icon position is programmed seldom, this mechanism does not affect performance while saving address decode h/w.

c. Enabling icon position modification by CPU is done in the same register h/w cursor is enabled: SR12.

SR12[3] Enable CPU access for Icon Position Modification
(default:0 = disable = use the same I/O address for cursor position modification)
This bit affects both horizontal and vertical position.

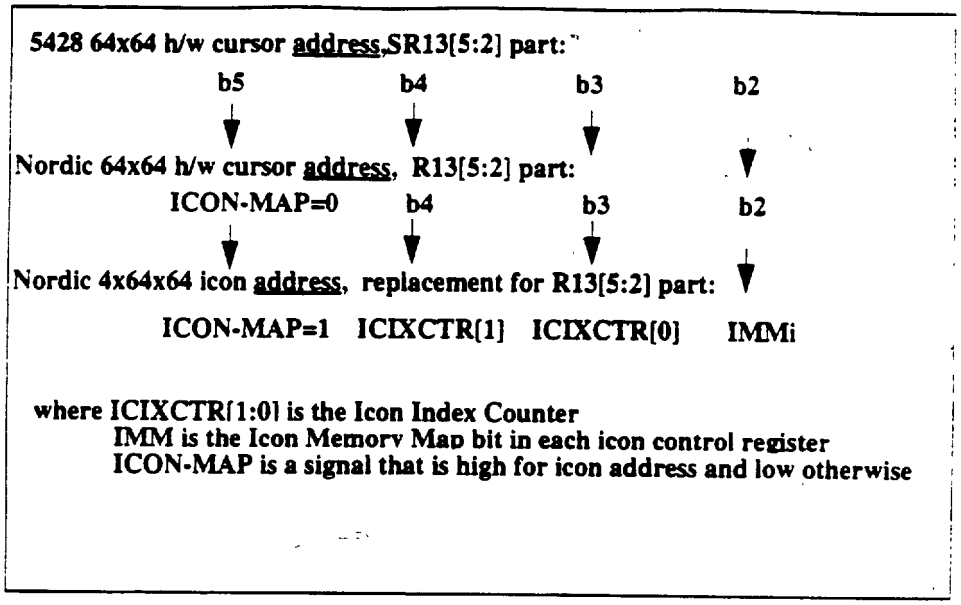
d. Icon and h/w cursor memory map selection:
5428 uses SR13[5:0] for 32x32 h/w cursor memory map selection (64 maps) and SR13[5:2] for 64x64 h/w cursor memory map selection (16 maps).

In Nordic, SR13[4:0] still select h/w cursor memory map, but the memory address bit which in 5428 is controlled by SR13[5] is no longer controlled by SR13[5]. It is controlled by an internal signal whose value is always 0 when a h/w cursor is addressed and 1 when icon is addressed. So in Nordic SR13[5] is no longer used to select a h/w cursor map. Only half of the 5428 h/w cursor memory is available for Nordic h/w cursor memory map. In Nordic there are 32 32x32 and 8 64x64 h/w cursor memory maps available.

The icon address is generated exactly as the h/w cursor address, but the source of the address map selection is no longer SR13[5:0] (it cannot be as SR13 is used for h/w cursor). SR13[5] is also noy used. To generate icon mamory map select, a two bit counter counts the first, second, third and fourth set of 64 scan lines on the Vertical Total Line Counter (the one not affected by vertical expansion). This two bit counter output, called the Icon Index Counter (ICIXCTR) will replace SR13[4:3] in Icon Memory Map Address generation.
A signal called ICON-MAP will be generated during Icon addressing. This signal is 1 if an icon data is to be fetched from memory and 0 otherwise (including when h/w cursor data is to be fetched from memory).
ICON-MAP signal will replace SR13[5] in both h/w cursor and icon memory map selection address.
One register bit in each icon control field will select the first or second memory map for each icon to be retrived from memory. This bit called Icon Memory Map (IMM) will

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replace SR13[2] in icon memory map generation.



e. Icons Control Registers

Each Icon has a field of bits attached to it

0.- icon i enable for display (i=0:3)
1.- display mode: 3colors + transpency or 4 colors
2.- blink enable at text cursor rate (or half of it)
3.- horizontal pixel doubling (extendes towards right)
4.- vertical scal line doubling (extends down)
5.- mamory map selection: two maps available per icon

Six bits per icon, all defaulting to zero. The icon enable bits select which icon is displayed
Start at SR2A register.
Use **SR2A,2B,2C,2D[5:0]** for Icon 0,1,2,3 control.
If an icon is not enabled, do not generate the memory cycles for its data... if it is not difficult to do, and do not display that icon.

f. SR2A[7] is Icon Test bit. Normally it is zero, only in test mode it will be 1.

g The colors for the Icon are in the 16 location RAM extension at location 258.
See SR12 description in 5428 Technical Reference Manual.
Locations 256 and 257 are accessible with pixel address 0 and F for h/w cursor access
Locations 259, 260, 261 and 262 are accessible with pixel address 3,4,5,6 as icon colors 0,1,2 and 3.
When three colors plus transparent attribute is used, the pixel addresses will be 4,5,6, for colors 1,2,3 (so pixel address 3 and color 0 of the 16 location special RAM are not used)

h. **SR2A[6]** is the most significant bit of fine horizontal position for the h/w icon:

SR2A[6] SRX[7] SRX[6] SRX[5] --> bit3 bit2 bit1 bit0

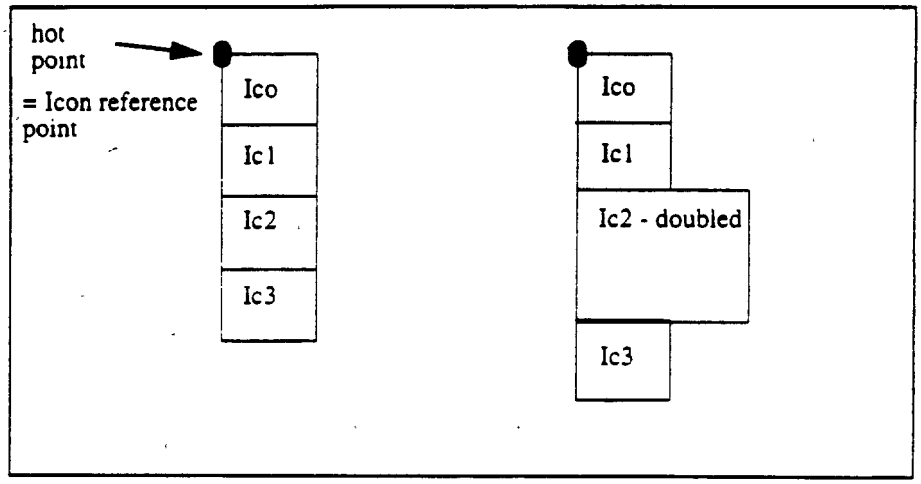
Please note that SR2A[6] will be used only in 9 or 10 dots text when the fine position is 8 or 9

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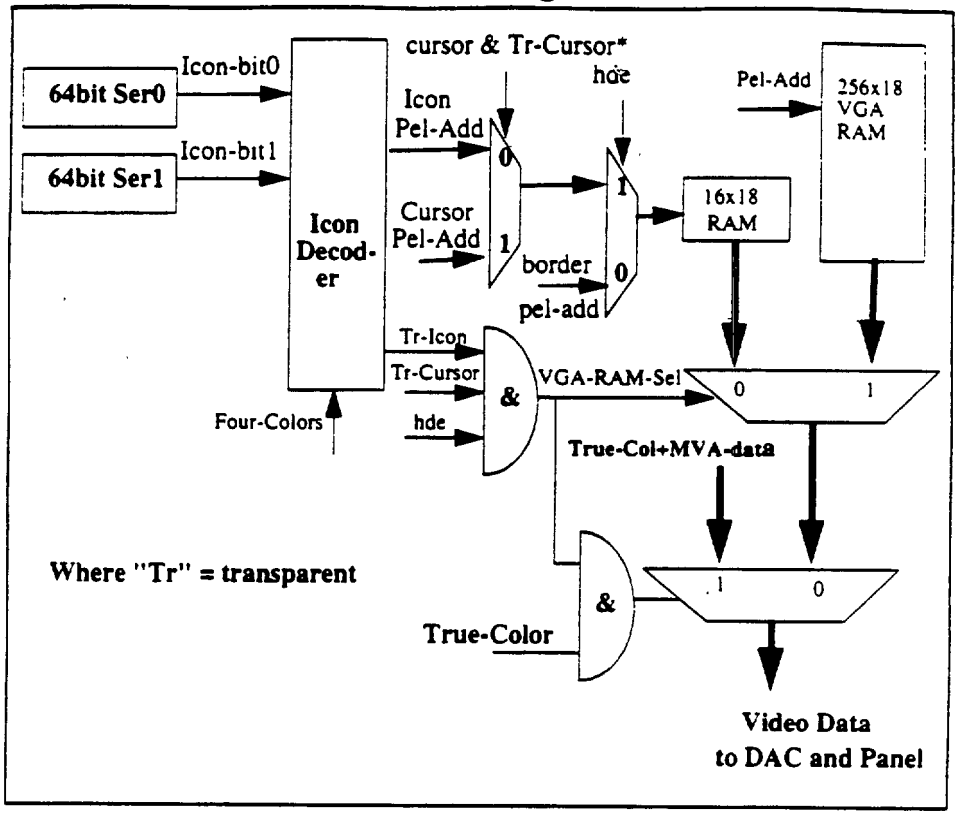
i. Please note that when character clock is expanded to 10 dots, h/w cursor also needs to be positioned at 8 or 9, so it needs one more bit of fine position.
SR2E[0] will be the msb of h/w cursor (default zero) to be used in this case.

H/W Activity for Icon

1. Horizontal and Vertical Window
2. Address Generation including the independent scan-line counter for Icon
3. Memory cycle generation (at the end of line, after h/w cursor if icon and cursor are on the same line)
4. Icon Latch, Serializer and Data Path including icon blink
5. Horizontal and Vertical Doubling



Icon Data Path Block Diagram



4.11 Dithering in Nordic

Due to new pixel depth modes and for increased flexibility the dither block in Nordic is diferemt than T1.
In Nordic the dithering is subtractive, (not additive like in T1). This moves the dither error (= double shade) to black where it is less obvious than it was before (when it was white).

CR4C - Input Resolution Override Register for Dithering

Bit	Definition
[7]	Enable Input Resolution Override (default disable) Normally the graphics mode resolution is decoded and fed to the dither block. For all graphics modes that go through the RAMDAC RAM - 6bits/gun is automatically the input resolution. For 5:5:5 RGB or 5.6:5 RGB or 8:8:8 RGB we use

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a diferent input resolution: 5 for 5:5:5 and 5:6:5 and 8 for 8:8:8 RGB.
In all cases the proper input resolution is automatically selected. If there is a need to overide this value, than we wiill use this bit to enable the override and write the new value in bits 3:0. For 8 bit per gun we write 8 (1000), for 6 bits per gun -> 6 (0110) and for 5 bits per gun -> 5 (0101).

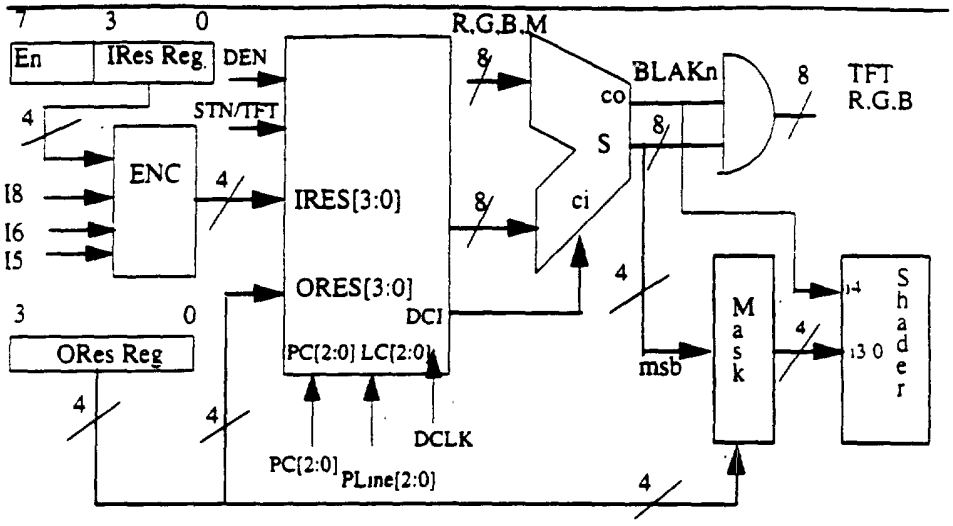
[6:4] Reserved

[3:0] The binary value of the override input resolution.
1000 -> 8bit/gun
0110 -> 6bit/gun
0101 -> 5bit/gun

CR4D - Output Resolution Register for Dithering

Bit	Definition
[7:4]	Reserved
[3:0]	The binary value of the output resolution for dithering 1000 -> 8bit/gun (TFT) 0110 -> 6bit/gun (TFT) 0100 -> 4bit/gun (TFT or 16 shades STN) 0011 -> 3bit/gun (TFT or 8 shades STN) 0010 -> 2bit/gun (4 shades STN) 0001 -> 1bit/gun (2 shades STN)

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TFT: 8,6,4,3 bits/gun

STN: 4,3,2,1 bits/shade (16+1,8+1,4+1,2+1 shades, +1 = force black)

Nordic Dithering

5.0 Nordic-1M Pinout Specification 208 pin package:

System Interface (reference is VESA VL bus): 74

(on BVDD)

DAT31:0
HIMEM0/ADR[24] (normally used as ADR[24], but it can be used as any upper address or any logic combination of upper addresses. The valid value of this pin for Nordic address space is programable in VESA VL and PCI bus.
HIMEM1/ADR[25] (normally used as ADR[25], but it can be used as ADR31 and leave 2GB of upper address space reserved for MPEG/JPEG boards). The valid value of this pin for Nordic address space is programable in VESA VL and PCI bus.
With these two pins, Nordic can directly decode up to 64MB of CPU address space in VESA VL bus.
ADR[23:2]
BE3n,BE2n,BE1n,BE0n
LADSn,LDEVn,RDYn
M/IOn, W/Rn
RESETn, LCLK
RDYRTNn,
EBROMn/SLEEPIn (Enable BIOS ROM Buffers on all busses or when not in ISA or SLEEP Input active L. If this pin is L, the chip goes in sleep mode as if 3c3[0] is 0 or 46E8[3] is 0. The ISAPU read-back register bit configures the pin for EBROMn. If not in ISA bus, this pin is configured as SLEEPIn and it should be tied H if not used.
INTR, CLK32K, OSC/XVCLK (14.318MHz or External VCLK)
SUSPIn/BLIn, SBYIn/ACTIn/FCEVIDEOn
(32KHz clock input,
Supend Input/ Back-Light Input
Stand-by Input/Activity Input/VAFC External Video Control Input - controlls the direction of FCP[7:0]. Pin configuration controlled by VAFCPU. Most systems will
use only one direction for VIDEO, probably video in, so the fact the FCEVIDEO is on BVDD should not require voltage translation).

Configurations: - VL/PCI/ISA bus, support/not BIOS, 8/16bit BIOS.
- Need a register bit to select SUSPEND Input or Back-Light Input. Default is SUSPEND Input.
- Need a register bit to select Stand-By Input or Activity Input. Default is Stand-By Input.
- SUSPIn, BLIn, SBYIn, ACTIn are level triggered, active L inputs. In Nordic there is no Suspend pin polarity bit as in T1 (SR8[4])

Note: a.In PCI bus, Alpine used ADR17:2 as BIOSA15:0. We assume that all portable

systems will use a motherboard video BIOS and do not support an adapter BIOS in PCI. We do support an adapter BIOS in VESA VL bus and ISA to facilitate demo board design.

b. EBROMn is active on all bus types: in ISA is generated on Address Decode and MEMRn, while in VL and PCI is unlatched address decode. In PCI bus the BIOS should be relocatable, an option we do not support. That is why we say that we do not support BIOS in PCI. We do support IOCHRDYn and RDYn/TRDYn for BIOS accesses too. All this logic should already be in 5428 (ISA and VL) and Alpine (PCI)

c. The 5428 Feature Connector pins are available in all buses. A register bit enables them early in the logic to save power when not in use.

d. In ISA RESETn has to be inverted outside the chip.

System/Bus Interface Signal Mapping

(See 54xx Reference Manual for Feature Connector Pins Description: FCyyyy)

TABLE 5. VESA-VL <-> PCI bus <-> ISA bus Pin Mapping

VESA-VL	Intel-PCI	ISA
HIMEM	--	--
ADR23:16	--	LA23:16
ADR15:9	--	SA15:9
ADR8	PAR	SA8
ADR7	STOPn	SA7
ADR6:2	--	SA6:2
BE3n	C/BEn3	SA1
BE2n	C/BEn2	SA0
BE1n	C/BEn1	SBHEn
BE0n	C/BEn0	RFRSHn
DAT31:22	AD31:22	--
DAT21:19	AD21:19	--
DAT18	AD18	MWRn
DAT17	AD17	IOCS16n
DAT16	AD16	IRQ
DAT15:0	AD15:0	SD15:0
RESET	RESET	RESETDRV ??
LADSn	FRAMEn	BALE
LDEVn	DEVSELn	MCS16n
RDYRTNn	IRDYn	AEN
W/Rn	IDSELn	IORn
M/IOn	--	MRDn
LCLK	CLK	IOWn
RDYn	TRDYn	IOCHRDY

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TABLE 5. VESA-VL <-> PCI bus <-> ISA bus Pin Mapping

VESA-VL	Intel-PCI	ISA
EBROMn/VADRn	VADRn	EROMn/VADRn
INTR	INTR	ZEROn

Notes: 1. SW2, SW0/MCLK/XMCLK and SW1 pins are normally used by the BIOS as panel type switches readable on SR24[2:0].

2. XMCLK and XVCLK (on OSC/XVCLK) are needed for manufacturing test of the chip. When they are used, SR24[1:0] will wiggle at clock rate and they should be masked on the tester.

3. MCLK and VCLK are needed for manufacturing test of the clock synthesizer and for chip debug.

DRAM Interface (for assymetric, dual WEn 256Kx16 DRAM-s): 50
(on DVDD)

MA9:0
MD31:0
RAS0n,RAS1n,CASn/WEn, OEn
WE0n/CAS0n,WE1n/CAS1n,WE2n/CAS2n,WE3n/CAS3n

Configurations: symetric/assymetric DRAM, dual WEn/CASn

Note: a) For dual CASn DRAMs, the WE0n:WE3n pins become CAS0n:CAS3n, while CASn becomes WEn.
b) Two RAS-es are used for two banks.
c) OEn is not actually needed as we use early write.

Clock Synthesizers: 6
(MAVDD, MAVSS feed mclk clock synthesizer, VAVDD, VAVSS feed dclk clock synthesizer)

MAVSS, VAVSS, MAVDD, VAVDD,
MFILTER, VFILTER
(Can we design a clock synthesizer without an external filter?)

CRT & TV-OUT Interface and RAMDAC related pins: 13
(DAVDD, DAVSS feed all RAMDAC custom layout)

R,G,B (analog)
IRef, DCVDD1, DCVDD2, DCVSS1, DCVSS2

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On CRTVDD:

HSYNC , VSYNC TO (these two pins are on CRTVDD)
CSYNC O (Composit Sync to be used with any analog TV Encoders like AD720
CSYNC is activated by SR25[4]=1, otherwise is forced 0.)

NTSC/PAL O
(A programable output that can be used to control a TV Encoder input that selects the TV standard. This pin is a generic programable output Its value is not affected by SR25[4].)

On FPVDD:

TVON/RES O (Generic Programable Output controlled by CR30[3] .
It can be used to control AD720 TV Encoder Power Control Pin.)
TVON is on FPVDD (not on CRTVDD like the other TV-OUT pins)
This pin is also reserved for future use (DRAM-s).

Note: If TV-OUT feature is disabled CSYNC, NTSC/PAL and TVON are forced L (to avoid powering up the TV Encoder in case it is powered off when not in use).

FLAT PANEL and Power Management Interface (on FPVDD): 31

R7/SUD3, R6/SUD2, R5/SUD1, R4/SUD0, R3/SUD7, R2/SUD6, R1/FCP[3], R0/FCP[2],

G7/SLD7/sud3/UD3/TD7, G6/SLD6/sud2/UD2/TD6, G5/SLD5/sud1/UD1/TD5, G4/SLD4/sud0/UD0/TD4, G3/SUD5, G2/SUD4, G1/SUSPSTn/FCP[1], G0/SBYSTn/FCP[0]

B7/SLD3/sld3/LD3/TD3, B6/SLD2/sld2/LD2/TD2, B5/SLD1/sld1/LD1/TD1, B4/SLD0/sld0/LD0/TD0, B3/MOD, B2, B1/OVRW, B0/FCVLK

(use slow edge pads and stagger them modulo 4)

FPVDCLK, LLCLK, LFS, FPDE, (use slow edge output pads)
FPVCC, FPBL, FPVEE

Notes:

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b. R1:0, G71:0, B1:0 (24 bit TFT panel extra video data out pins)
c. We need also bits for SUSPST and STANDBYST, PANEL-ON/OFF, PANEL-IN-POWER-UP-or-DOWN. Dwarka, do we have this now ?
d. We assume that only STN panels need external MOD. CL 152590
e. No NPD pin.
f. FCP[3:0] pins are I/O-s whose direction is controlled by FCEVIDEOn in

VAFC configuration. FCVCLK is the clock that clocks them in and which should be used to clock them while they are displayed or at least to resynchronize them before being latched on the internal clock. FCVCLK is always an input when in VAFC configuration.

Nordic TFT Panel Data Pin Name versus the actual TFT Panel Data Signal for diferent types of TFT Panels

Nordic Pin Name-> /Panel Type	RGB7	RGB6	RGB5	RGB4	RGB3	RGB2	RGB1	RGB0
8bit/gun	RGB7	RGB6	RGB5	RGB3	RGB2	RGB1	RGB0	RGB0
6bit/gun	RGB5	RGB4	RGB3	RGB2	RGB1	RGB0	N.U.	N.U.
4bit/gun	RGB3	RGB2	RGB1	RGB0	N.U.	N.U.	N.U.	N.U.
3bit/gun	RGB2	RGB1	RGB0	N.U.	N.U.	N.U.	N.U.	N.U.

Where N.U. = Not Used for Panel Data with this type of panel.

~~Audio Port (on ADVDD): 6~~ **Removed on 12/24/93**

~~SDO (SErial Data Output to CODEC pin SDIN)~~
~~SDI (Serial Data input from Codec pin SDOUT)~~
~~FSYNC (Frame Sync Output)~~
~~SDCLK (Serial Data Clock I/O)~~
~~D/C#/AUXS1 (Data/Control Select Output or CS4231S Chip Select for the ISA bus)~~
~~PDN (Power Down Output)~~
~~Note: These pins can be used as extensions for 24 bit TFT panels, in which case the chip does not support the audio port. Note also that CS4215 has Reset# pin.~~

Miscellaneous Pins: 12

Following pins on MVDD:

SW2/RES4CS I (Switch #2 or reserved for SDRAM support in the future)
SW1/RES4CKE I (Switch #1 or reserved for SDRAM support in the future)

SW0/MCLK/XMCLK I/O with PD controlled by XReset
(Switch #1 or mclk driver buffered output for tesing and debug or external mclk for testing; a special register bit disables this output in normal operation for power savings.
Default: Input on which either SW2 or XMCLK comes in.
Only if the special register bit is set, this input becomes output and outputs MCLK from the clock synthesizer for testing.
The special register bit defaults 0 = the pin is

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configured as Input. Please note that a h/w configuration PU/PD controlls if the actual internal mclk comes from an internal or external source, but this PU/PD does not control if SW2/MCLK/XMCLK is an input or an output.)

RES4PMS Free Pin with no buffer on it.

Following Pins on PVDD:

TRWn I (Test Latch Load Enable, active L - for pinscan & test mode)
VCLK/FCDCLK I/O (Switch #0 Input or vclk driver buffered output for testing and debug, or VAFC Dot-Clock Out ; Default for this pin is Input on which SW#0 is applied. VCLK and FCDCLK is the same signal, the name is diferent to ease reference to VAFC spec)
FCP[7:4] I/O Feature Connector Data Pins bits 7 to 4. The other Feature Connector pins are shared with some panel or host bus pins.
FCESYNCn/RES4SDCLK I 5428 Feature Connector ESYNCn pin - controlls the direction of FCBLANKn and its effect and tri-states HSYNC and VSYNC.
FCBLANKn I/O Feature Connector active low bidirectional Blank signal. Its direction is controlled by FCESYNCn.

Digital, Mixed Voltage Power Pins: 22

BVDD1, BVDD2, FPVDD1, FPVDD2, MVDD1, MVDD2, CRTVDD, CVDD1:4, VSS1:11

Total Pins Used: 208 (with two Reserved pins and three other pins that could be freed.).

Pinout Modifications in rev. 3.8 relative to rev. 3.7 09/11/93

1. Took-out Whisper Support Pins: WWRn, WRdn, WAD[3:0], FPCn.

2. Reduced the number of CPU Address Pins: ADR[24:27] went-away. Use HIMEM to place the chip outside 16MB of memory for linear addresing.

3. Killed CRTVDD and placed CRT Interface on Host Bus VDD.

4. Introduced VAFC pins in a unique pinout configuration in both VESA VL and PCI. Added VAFCPU a pull-up to enable VAFC (VESA Advanced Feature Connector). ADR[27:24] VAFC pins, and R[7:4], G[7:6] , EROMn/VADRn, SUSPI/BLI, SBYI/ ACTI get a configuration for VAFC -> total 14 pins.
SW0/VCLK will be used as VAFC VCLK, losing SW0 pin as panel type when VAFCPU is used.

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In PCI bus, no ADR pin will be shared with VAFC.

ASW0PU (Alternate Switch 0) will be added on MD pins to replace SW0 pin when VAFC is enabled by VAFCPU. ASW0PU will read-back in the same register bit as SW0, so the BIOS will not feel any modification in the reporting scheme. The chip will draw more power in suspend with VAFC.

5. Moved SW2, SW1/MCLK/XMCLK the two reserved pins (one obtained by killing CRTVDD)and TRWn on MVDD to prepare for SDRAM pin compatible option in the next Nordic that supports SDRAMs. Marked them as "reserved for SDRAM pin name" It looks that TRWn will not be needed, but it was moved on MVDD so that in case it is needed, it is available (in this case we'll need an extra switch for SDRAM support or at least to disable TRWn test mode effect).

6. Rearanged VAFC pins as pins R4 and R5 were used by VAFC - an error.

Pinout Modifications done on 01/06/94 rev. 3.0

1. Update Panel Data Pins based on Robin's Table.
2. Move MOD pin on a Panel Data Pin used in 18bit TFT
3. Move OVRW on a 24bit Panel Data Pin.
4. Removed pin configuration for TV-OUT support with digital encoders. All pins marked TV were removed. As a result, some pins like LLCLK, LFS, FPDE, FPVDCLK have one function now
5. Removed WavePort pins, including AUDVDD: total 7 pins freed. AUX2 and TVG muxed on EBROMn are no longer needed either.
6. Added one more CPU address pin: instead of HIMEM, Nordic has now HIMEM0 and HIMEM1, corresponding to CPU Address 24 and 25 or any other external decode of the high order CPU address bits. In the proccess of adding this pin, most CPU Interface pins on the right side were moved to the right by one pin
7. Added CRTVDD supplying HSYNC, VSYNC, CSYNC, NTSC/PAL CRT and TV Interfaces output buffers.
8. EBROMn is shared with TVON, the power-on signal for AD720. So, in ISA bus with on chip BIOS support, AD720 power on cannot be directly controlled by Nordic.
9. Added pins for Analog TV Encoder support - AD720 and MC1377
   a. CSYNC = Composit Sync signal
   b. NTSC/PAL = 0 -> NTSC, 1-> PAL
   c. EBROMn/TVON (see #8).
10. ASW0PU "Alternate Switch 0 Pull-Up" pull-up on pin 155. MD[26] was removed, as SW0 is now not multiplexed.
11. Demultiplexed some of the pins previously multiplexed:
    a. Pin 168 TWRn/RES4PMS is now RES4PMS, a pin reserved for synchronous DRAM support.
    b. SUSPI/BLI/FCBLANKn is now SUSPI/BLI, not affected by the Feature Connector Enable Configuration
    c. As a consequence of b, pin 97 is FCBLANKn (not muxed with anything) Please note that FCEVIDEOn is still muxed with SBYI/ACTI as before, as Standby Input and Keyborard Activity are less important functions in a system
    d. SW0 is no longer muxed on VCLK/FCDCLK So VLK/FCDCLK is a pin but it moved to pin 103 in the PVDD area, to be consistent with FC power supply

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12. SW1. muxed on MCLK/XMCLK (pin197) became SW0 This is just a name change to have the switches placed in a more consistent manner
13. SW1 is now muxed with a reserved pin: RES4CKE. pin 148. which before was totally reserved. The idea here is to go for pu/pd with SDRAM-s for SW2 and SW1. while keeping SW0 on MCLK even with SDRAM-s.
14. Pin 147 is Reserved. It is actually one of the WavePort pins. but placed in-between Memory and Panel VDD busses (on MVDD) for maximum flexibility To acheive this. the pins on its right were moved to the right by one
    FPVEE <BIAS> moved down to pin 98 (it was 105).
15 TRWn is now by itself on pin 96. on FPVDD
16 The names of all flat panel data pins reflect the panel type table attached to this document

Configuring Nordic-1M

If Terminator used specially assigned pins to configure the chip, **Nordic-1M will use some of the MD31:0 pins sampled on the Reset trailing edge,** similar to Mustang. The pad cells will have an active pull-down controlled by an **extended Reset** signal. The pull-down resistence will be about 75KOhm. An external pull-up less than 60KOhm is needed only if the option is used. In Suspend. the MD pads are inputs and the DRAM OEn is H so no DC current is drawn by the configuration h/w. An external resistor is needed only if the configuration pin has to be H at Reset. H/W configuration can be read via s/w too.

All h/w configuration latches are read accessible via I/O. The h/w configuration is latched on Reset trainling edge. (these latches were r/w, with s/w PU read, having only read is enough).

We'll define the configuration pins to minimize the number of external resistors:

CPU Bus Configuration:

On MD18:16 &	-> no external PU	= 32bits VESA VL bus at 33MHz or less bus clock
& MD23	-> MD16 PU	= 32bits PCI bus with Burst PU called "PCIPU"
	-> MD17 PU	= 16bits ISA bus PU called "ISAPU"
		ISAPU controls also the pin EBROMn/SLEEPIn
		In ISA bus this pin is EBROMn output; otherwise it
		is SLEEPIn input to be tied H if not needed
	-> MD18PU	= 32BIT VESA VL BUS AT 50MHZ BUS CLOCK
		PU called "FVLPU

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-> MD23 PU = 32bits PCI bus no Burst PU called "PCINBPU".
This is a reserved configuration in case burst does not work on a PCI bus.

Reads-back in SR22:

PCIPU on MD16 -> SR22[0]
ISAPU on MD17 -> SR22[1]
FVLPU on MD18 -> SR22[2]
PCINBPU on MD23 -> SR22[7]

Clock Configuration:

On MD19 (reads back on SR22[3])
-> no external PU = internal MCLK and VCLK clocks, from the internal clock synthesizer
-> MD19 PU = use external clocks from SW1/MCLK/XMCLK and OSC/XVCLK
PU called"XCLKPU"

This PU is used for manufacturing test.

One reg. bit is needed if internal clock is selected to control outputing mclk on the MCLK/XMCLK pin = 1 if use internal clock then output it on SW0/MCLK/XMCLK pin. -> SR23[0] is this bit.

Memory Configuration: SRF[0]
No Pins. Use Two Register Bits -> 2CAS/2WE bit=H 2WE, bit=L 2CAS (default =L)
-> Symetric/Asymetric bit=H Asym., bit=L Sym. (default=L)

BIOS Support: (reads-back on SR22[6] for BIOS8PU)

Nordic-1M supports 16bit or 8bit BIOS and only in ISA bus configurations.
The BIOS is always supported when in ISA.

On MD22 -> no external PU = 16bit BIOS
-> external PU = 8bit BIOS (no MEMCS16n decode on C000)
This option is mostly for debug in case 16 bit BIOS range decode is not fast enough.
If the BIOS support is disabled, this configuration is don't care. Called "BIOS8PU".
Please note that Nordic-1M supports C000 BIOS only in ISA.

In a normal note-book the BIOS is at E000:0 or C000:0 but it is not supported by Nordic: so no external component is needed.

Sleep Address Selection:

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On MD21: Sleep Address Selection (reads-back on SR22[5]).
-> No external PU = sleep at 3C3[0] - to be used when Nordic is on the Mother-board (most cases)
-> External PU = sleep at 46E8[3] - to be used when Nordic is an adapter (like a PCMCIA card and/or an adapter to turn desktop into an environment friendly PC) Called: S46PU
Note that Nordic-1M comes-up awake.

Feature Connector Configuration: (reads-back on SR24[7])
On MD25:
-> No external PU = no Feature Connector Support: outputs used only for FC are forced L, I/O are forced inputs, I/O and inputs are forced on the chip so that they do not take power if not connected externally.
-> External PU = All pins needed for FC including OVRW are active.
Called: VAFCPU

~~On MD26: Alternate SW0 Selection (Reads-back on SR24[0] when SR24[7] is 1)~~

Total: 9 H/W PU configuration options.
In normal operation with FC enabled up to three external PU-s may be needed (bus type if not VL and FC).
In normal operation with FC disabled up to one external PU-s may be needed (bus type if not VL and FC)

Summary of PU/PD Configuration Pins and Register Bits where they can be read-back:

SR22 [7:0] H/W Configuration Read Register #1

Read only register, written on reset training edge by activating PU/PD on MDi pins. The PD-s are inside the pads active only during XReset (extended reset).

[7] 32bits PCI bus no Burst h/w PU configuration on MD23. It is called "PCINBPU" (read only bit).
This is a reserved configuration in case burst does not work on a PCI bus.

[6] Select 8 bit BIOS support (if 1). Otherwise 16 bit BIOS support if the BIOS support is at all enabled. PU on MD22.

[5] Resereved for Sleep Address Select: reads back S46PU (MD21).
1 = I/O address 46E8[3] as sleep address (needs external PU).
0 = I/O address 03C3[0] as sleep address (no external PU is needed).

[4] Reserved

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[3] Select external clocks: MCLK and VCLK on SW0MCLK/XMCLK and OSC/XVCLK. (default: internal clock synthesizer, SW0 and OSC).

PU on XCLKPU on MD19.

0 = internal clocks with the pins used as inputs for panel type switch #1 and OSC. If SR23[4] and SR23[0] are 1, VCLK and SW0/MCLK/XMCLK. respectively become VCLK and MCLK outputs respectively, for test purposes (only if SR22[3]=0 MCLK can be seen, but VCLK can be seen even if SR22[3]=1 as long as SR23[4]=1)

1= SW0/MCLK/XMCLK and OSC/XVCLK become XMCLK and XVCLK inputs generating directly chip MCLK and VCLK without clock synthesizer. The clock synthesizers are powered down if SR22[3]=1.

[2] Select VESA VL Bus at 50MHz
1 = VESA VL bus at 50MHz selected (needs external PU on MD18)
0 = VESA VL bus at 50MHz not selected

[1] Select ISA Bus with PU on MD17.
1 = ISA bus selected (PU on MD17)
0 = ISA bus not selected (no PU on MD17)

[0] Select 32bit PCI Bus with PU on MD16.
1 = 32bit PCI bus selected (PU on MD16)
0 = 32 bit PCI bus not selected (no PU on MD16)

If [1:0] = 00 (i.e. no external PU on MD17:MD16) 32bit VESA VL bus is selected
No more than one PU on MD17:MD16 should be used.

Note: In AVGA3, CF14 is "Enable Local BUs Address Latching Interface". Alpine does not have this configuration bit. We need to do what was done in Alpine to get rid of this Configuration Pull-up/Pull-Down option. *CAN we? WAs this done, Dwarka?*

SR24 Panel Type Switches Register

[7] VAFCPU (VESA Advanced Feature Connector External Pull-up) Read-back. If external pull-up (the bit read-back 1) then all VAFC pins are configured for Video Port. Otherwise they have other functions or are disabled if no other function. (Disabled= the inputs are forced = the TTL and CMOST threshold controls are off & the outputs are tri-stated. It actually reads back what is latched on Reset on VAFCPU. VAFCPU is on MD25.

[2:0] SW2:0 pins read back (read only bits) ~~Please note that bit [0] reads back SW0 if VAFCPU (SR25[2]) is 0 and ASW0PU if VAFCPU is 1.ASW0PU is on MD26.~~

Symetric/Asymetric DRAM -> SR8[7] in T1, CF13 in AVGA3
=> SRF[1] 0 = Symetric DRAM Default: 0
1 = Assymetric DRAM

This bit is read only in AVGA3 (reads back CF9), but it is writable in T1. It controlls MCLK frequency as an alternate to SR1F. We will use only SR1F to program MCLK frequency in Nordic. The default MCLK frequency will be 39.374MHz. corresponding to SR1F[5:0] = 18H=22D. This frequency fully meets the spec for -80 256Kx16 DRAM-s.

Two CAS or two WE DRAM -> pin 72 in T1, CF12 in AVGA3
=> SRF[0] 0 = 2 WE DRAM (Default:0)
1 = 2 CAS DRAM

16 or 32bit wide Video Memory (One or Two 256Kx16 DRAM-s or SDRAM-s)
-> not in T1, SRF[4:3] in AVGA3 (01=16bit, 10=32bit)
=> SRF[7,4:3] will be used in Nordic with the same encoding as in AVGA3. (11 is reserved for 64bit wide). Default: 10 (32bit). See Table next page. Please note that we have room to add other types of DRAM-s (SDRAM-s for instance).

In AVGA3 SR8[0] is "CS OUt to EEPROM" a feature Nordic does not Support. Nordic will not change the meaning of AVGA3 bits unless they are read only (like the pins or external PU read back).

SR8[2:0] are in T1 the read-back bits for SW2:0 input pins, but AVGA3 uses them for EEROM programming so we moved SW2:0 read back to SR24[2:0].

In T1 SR8[7] is symmetric/assymetric addressing... in Nordic this is SRF[1].

Two or one Bank 32bit wide DRAM
-> not in T1, SRF[7,4:3] in AVGA3 (00=8bit, 01=16bit, 10=32bit, 11=64bit. SRF[7] controls if 2MB of Video memory are available with 4x512kx8 -0- or with 4 256Kx16 DRAM-s, two banks -1-). *It seems that in AVGA3 to support 1MB with two 256Kx16 dram-s and 32bit wide bus, we select 32bit wide and SRF[7]... but I do not exactly know how this configuranon is selected.*

=> SRF[7,4:3] in Nordic, will select the Video Memory Configuration slightly differently than in AVGA3 and Alpine. See the following table.

	SRF[7]	SRF[4]	SRF[3]	Memory Configuration
new	0	0	0	32bit, 2MB=4x512Kx8
	0	0	1	16bit, 512KB=1x256Kx16
	0	1	0	32bit, 1MB=2x256Kx16 (default)
	0	1	1	Reserved (64bit in Alpine)
new ?	1	0	0	32bit, 2MB=4x256Kx16, Two Banks
	1	0	1	Reserved

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1	1	0	Reserved
1	1	1	Reserved

DRAM Timing select (short RAS or long RAS)
-> SRF[2] in T1 and AVGA3
=> SRF[2] in Nordic, default 1 = short RAS (3.5 L, 2.5H)

BIOS 48KB or 32KB -> not in T1; CF8 in AVGA3. In T1 SR8[4] is Suspend pin polarity. In Nordic Suspend pin is always active L (0 on pin puts the chip in Suspend).
=> SR23[2] in Nordic =0 32KB BIOS (default=0) C0000:C7FFF
=1 48KB BIOS : C0000:CCFFF
The initial BIOS code should be placed in the first 32KB starting at address C0000.

BIOS ROM ZERO* wait select in ISA and fast timing in VL bus
-> not in T1; CF1 in AVGA3
=> SR23[1] in Nordic =0 no ZERO wait state for BIOS in ISA

=1 ZERO wait state for BIOS in ISA, 8MHz bus

Output internal VCLK on VCLK/FCDCLK pin -> not in T1 or AVGA3
=> SR23[4] in Nordic =0
VCLK/FCDCLK is an output pin forced L
=1 either VCLK or
FCDCLK is outputed on this pin,
depending on VAFCPU (read back in SR24[7] value).
If SR24[7]=1 (Feature Connector pins enabled) than FCDCLK is outputed, otherwise, if SR23[4]=1 than VCLK is outputed. VCLK out is needed only for manufacturing test.

Output internal MCLK on SW0/MCLK/XMCLK pin -> not in T1 or AVGA3.
=> SR23[0] =0 this pin is an input namely XMCLK if SR22[3]=1 (enable external clocks) and SW0 otherwise.
=1 output mclk
This pin will normally be used as SW0, except for manufaturing test where mclk and xmclk functions are needed.

SuspendI/BLI bit -> not in T1 or AVGA3.
=> SR23[5] in Nordic, 0= Suspend pin in Suspend/BLI pin (default)
1= BLI pin on Suspend/BLI pin

SBY/ACTI/FCEVIDEOn bit. -> not in T1 or AVGA3
=> SR23[6] in Nordic, 0= SBY on SBY/ACTI pin (default)

1= ACTI on SBY/ACTI pin
If SR24[7] = 1 (VAFC pins enabled) this pin is FCEVIDEOn independent of SR23[6].

VAFC Enable bit -> not in T1 or AVGA3.
(read only bit, actually reflecting the status of an external configuration PU: VAFCPU on MD25 latched at RESET or under S/W Control)

=> SR24[7] 0= VAFC Disabled at pins.
All VAFC dedicated pins are disabled to save power: inputs are disabled, outputs are L. **I/O-s are disabled inputs (forced H)** internally. The shared pins are not in Feature Connector configuration.
1= VAFC Enabled at pins.
If any shared pins, they are now in Feature Connector Configuration.
All dedicated pins are active in this configuration.

Compressed Live Video (SashaPack) Enable bit -> not in T1 or AVGA3.
=> SR24[6] 0= disable (default)
1= enable

~~Audio In (from CS4215 to Nordic) Enable bit -> not in T1 or AVGA3.~~
~~=> SR24[5] 0= disable (force inputs inactive and outputs L disable AI-FIFO and cycles)~~
~~1= enable~~

~~Audio Out (from Nordic to CS4215) Enable bit. -> not in T1 or AVGA3~~
~~=> SR24[6] 0= disable (as above but AO-FIFO)~~
~~1= enable~~

Panel Type Switch Read-back -> SR8[2:0] in T1 or SR7[6:4], not in AVGA3
=> SR24[2:0] in Nordic, read only, writable on Reset or under S/W Control (SR24[3])
When SR24[3] whose default is 0, transits from 1 to 0 SW2:0 pin value is latched into SR24[2:0 which cannot be written by I/O.

Please **note** that **R9x[1:0]** TFT Panel type field of T1 was expanded to support 24bit TFT panels:

00 -> 9bit (333) (as in T1)
10 -> 12bit (444) (as in T1)
01 -> 18bit (666) [was x1 in T1 covering both 01 and 10 !!]
11 -> 24bit (888) -> new in Nordic

Notes:

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0.1 a. If 24bit TFT panel is selected, all related pins will be configured for it and it has priority over panel pins configuration settings for cross talk reduction enabled.
b. MOD is selected only with STN panels.
c. If 24bit TFT is not selected and VAFC is not selected, then SUSPST is selected on
G1/SUSPSTn/FCP[1] and SBYST is selected on G0/SBYSTn/FCP[0].
d. Panel Data unused output pins are forced 0 when not in use (depending on panel type)

SR25 Timers S/W Reset, H/W Config. #2 & Packed Modes Register

[7] The 8514A RAMDAC address is decoded as valid RAMDAC address in addition to the standard VGA RAMDAC address.
[6] Allows use of EBROMn as external 8514A RAMDAC
In this case it bahaves like 5428.
[5] Enable 1bit/pel packed mode
[4] Reserved for 2bit/pel packed mode
[3] Enable 4bit/pel packed mode
[2] Configure PCI bus Nordic module for Faster PCI write
[1] Reset Stand-by Timer
[0] Reset Backlight Timer

Other Register Related Topics
(See nordic-regs-rev#.lst where # is the latest one)

BIOS SCratch Registers #5 and #6 (2 extra required) (r/w)

SR28:SR29[7:0] are scratch registers.
Note that SR9, SRA, SR14 and SR15 are AVGA3 scratch registers which we keep in Nordic. Also there are 13 18 bit scratch registers in the RAMDAC is SR12[1]=1.

R9x - TFT Panel Data Format

---

[7] Reserved

[6:4 Select a 0 to 7 shift-clock delay from the internal character clock counter
(8 VCLK/Character Clock) to TFT panel HSYNC (LLCLK) signal -> as in T1.

[3:2] Panel size select:
00 -> 640x480
01 ->

[1:0] TFT Panel Type:

00 -> 9bit (333) (as in T1)
10 -> 12bit (444) (as in T1)
01 -> 18bit (666) [was x1 in T1 covering both 01 and 10 !!]
11 -> 24bit (888) -> new in Nordic

Registers that are Moved Relative to T1

CR1B[7,4,3,2] (R1B in schematics):

[7] Disable Text Cursor Blink in T1. Do we use this feature in T1?
Enable Blank End Extensions in AVGA3
[4] PCLKO (Panel Clock) no divide by two control in T1.
I am not sure this bit is actually needed in Nordic.
[3] IRQ Every Frame or Every Other Frame ? Is this bit used inT1?
[2] Not Used at All in T1.

I think that all these bits are not actually used. Are they needed ? -> Robin.

CR1C[7:0] & CR1D[7:0]

Are important LCD and Power Management Registers in T1 and Overlay Registers in Alpine. These registers are not in AVGA3, but because they are used in Alpine we may move them to **CR2C[7:0] and CR2D[7:0]**, which requires one more CRTC Index Register Bit. So:

CR1C -> CR2C & CR1D -> CR2D in Nordic relative to T1.

SRF[7]

In T1 is CRT Refresh Disable. This bit gates /FB/RWC[5] in FB sheet 6. In AVGA3 is DRAM Two Bank Configuration select bit.
I don't think that this bit is used in T1 ? -> Robin.

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SR16

In T1 is used to control the pads for power and threshold. In AVGA3 is not used. In Alpine is CRT FIFO demand threshold and other things ([4:0] are used).

Move SR16 bits of T1 to SR20 to avoid contention with Alpine. Increase SRX Sequencer Register Index to 6 bits.

SR1A

In T1 is used as Test register. In AVGA3 and Alpine is Signature Generator Result Hi. Move T1 SR1A bits to SR21 if it is not replaced by a similar register in AVGA3.

Nordic Revision and Mask Codes

Nordic Microsoft ID CR2F: CD
Nordic Revision CR27 (4bits chip code, 7z , where z is BIOS rev. counting down): 2F
Nordic Mask Code CR25: 00
Nordic PCI ID: 1200H

-----$$$$-----

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```
User name:    SHAW (11)                    Queue:  UIDESK/UNIX_UIMKGT
File name:                                 Server: CLFPCD010
Directory:
Description: NORDIC28.
             December 21, 1998                              5:30pm
```

EXHIBIT
RX-580 C

```
 SSS  H   H   A   W   W
S   S H   H  A A  W   W
S     H   H A   A W   W
 SSS  HHHHH A   A W W W
    S H   H AAAAA W W W
S   S H   H A   A WW WW
 SSS  H   H A   A W   W


L      SSS  TTTTT
L     S   S   T
L     S       T     : :
L      SSS    T     : :
L         S   T
L     S   S   T     : :
LLLLL  SSS    T     : :
```

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0 5 9 4 0 4 7 - 0 5 9 4 0 4 7 5 9 0

NORDIC-1M Design Specification

by Vlad Bril, Robin Han, Sasha Eglit, Rakesh Bindlish, Dwarka Partani.
Jeff Ort
rev.5.1 December 21, 1998

1.0 Introduction & Table of Contents

Nordic is Cirrus Logic's Fourth Generation Flat Panel VGA Controller to be marketted in first half of 1994.
Nordic-1M is a mid-end member of the Nordic family. It is a GUI Accellerator with PCI support and Multi-Media Features.
Nordic-1M is targetted for the mid to high end of the **Note-book Computer Market** and for for the energy efficient **desk-top computers mother-boards**.
Nordic-1M is **not** targetted to the adapter market.

1.1 Table of Contents

This Specification will address the following:

1. Introduction and Table of Contents
2. Basic Feature Set
3. Detailed List of Features
4. Pinout and Pin Description
5. Architecture Specification
6. Register Specification - this is a diferent document
7. Product Implementation Plan - this is also a diferent document

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2.0 Nordic-1M Basic Feature Set

1. **Flat Panel VGA Compatible GUI Accellerator register and feature compatible to 5428 and Alpine I A/V. Priority: A (= highest).**
2. **32bit CPU, 32bit Video Memory, 32bit BLT and 32bit CPU to Video Memory Data Path. Priority: A (= highest).**
3. **208 pin QFP package.**
4. **Targeted to sample CY Q1'94, production CY Q2 '94. Priority: A (= highest).**
5. **Target cost: $12 to $10 -> less than 400mil [/] in C8 Foster City.**

6. **Multimedia Features**

- Part of a well defined **System Solution** for high performance **CD-ROM video and audio playback** for the portable market. **Priority: B**
- Part of a well defined **System Solution** for mid performance **low cost live NTSC Video and Audio with the NTSC decoder on a PCMCIA card. Priority: B**
- ~~**Audio Port to Display Memory**. Audio Buffer to Serial Interface for CS4248 Audio Codec. **Priority**: C (CS4215 is not fit for notebook computers).~~
- **Video Playback decompression accelleration for CinePak** including Color Space Conversion (YUV -> RGB). **Priority: B**
- **Live Video in a 320x240 or 640x480 Window** from a proprietaryly compressed TV decoded data source (at 30Hz) on TFT color panels. Data is stored compressed and it is decompressed to 18bit/pel or 24bit/pel in real time at display time. NTSC decoder and data compressor is on the PCMCIA card or the PCMCIA controller. Please note that due to live video bandwidth requirements on PCMCIA bus , a relatively non-expensive way to achieve the second feature is to implement this compression algorithm. **Priority: B**
- Color Key Live Video Overlay based on a 5428-like Feature Connector with PCI bus (only).

7. **Integrated in Nordic 1-M**

- Color Space Converter for CinePak. **Priority: B**
- 18bit DAC with direct color capability **Priority: A**
- *24bit RAMDAC with true color capability* **Priority: C**
- Clock Synthesizers for Video and Memory Clock (65MHz/3V, 110MHz/4.5V). **Priority: A**

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- DAC IRef Current Source on chip. **Priority: C.** *Boyd and ManShek are working on it*

8. **Direct Bus Interface**:

- 32bit VESA-VL bus (and 486 local bus) **Priority: A**
- 32bit PCI bus. No on chip BIOS ROM support in PCI. **Priority:** A
- 16bit ISA bus for demonstration and easy system validation. **Priority: B**
- 32K or 48KB BIOS ROM support in ISA and VESA VL bus. **Priority: B** (only for BIOS/ system debug)
- At least 5 scratch pad registers: optimum 8 scratch pad registers. **Priority: A.**

9. **Performance Enhancements** to achieve 15-20MWinmarks at 1Kx768 8b/pel:

- 32bit BitBLT with memory mapped I/O BitBLT registers (as in 5428 ?or Alpine) Priority:A
- BLT buffer of 8 (~~or 16~~) bytes for Source (and Destination ?) data. (5428 buffer is 8bytes, Alpine is 16bytes) (as 5428)
- *X/Y offset for Pattern BLT (as in Alpine)* **Priority:** C
- h/w graphic cursor 64x64 (as in 5428)
- color expansion (as in 5428)
- linear memory addressing (as in 5428)
- 4 stage 32bit wide write buffer and capability to page CPU cycles if accumulated in the write buffer (this is already in 5428)

10. **Display Memory:**

- *0.5MB (16bit wide),* 1MB or 2MB memory addressing 32bit wide (as in 5428)
- *1 or* 2 256Kx16 one bank or 4 256Kx16 two banks (2 CAS symetric, 2 WE asymetric) (as in 5428)
- maximum memory clock frequency: 50MHz/3V, 65MHz/4.5V **Priority: C**

11.**Flat Panel Support**: **[Priority: A]**

- Color TFT (24bit, 18bit, 12bit, 9bit)
- Color Dual Scan and *Single Scan STN* (16 and 8 bit, including dual clock panels)
- Monochrome TFT (8bit),
- Monochrome Dual Scan STN (8bit),
- Monochrome Single Scan (4 and 8bit) support

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- Simulscan with all Fast Panels (6.3MHz or equivalent) with 32bit wide memory
  No simulscan with 16bit wide memory with dual scan color panels.
  No simulscan for 3MHz monochrome dual scan panels.
- 640x480 single and dual scan support (Priority:A)
- 800x600 TFT *and no single and dual mono and color STN panel support (Priority: C)*
- 1024x768 TFT *and no single and dual scan STN panel support . (Priority: D)*

12.Display Features

- High quality monochrome and color shading, at least as good as 6440. Priority: A
- Shading option for fast panels. Priority: B
- Up to 8, 64x64 Hardware Icons independently mapped color+transparent background. **Priority: C**
- *Whisper Cross-Talk Reduction (If panels will be available in the time frame and if we can accomodate it with the shading algorithm).* ***Priority: C***
- ***"Office Productivity Booster Dual Display"*** 640x480 (panel) & 640x480 (CRT) 4 or 8b/pel or 640x480 (panel) & 1024x768 (CRT) 4 or 8b/pel ***Priority: E***
- Vertical Expansion in text and graphics (as in 6235 or 6440)
- Automatic Centering if not expanded (as in 6235)
- *Grey-Shades Maping options ?? Is this needed ? Priority: D*
- Text Contrast Enhancement options. (as in 6235 or 6440)
- *Inking Plane ?? Priority: D*
- *180 and 90 degree image rotation ?? Priority: D*
- *12 and 16dots wide font support ?? Priority: D*
- *h/w offset on h/w cursor ?? Priority: D*

13.Resolutions Supported:

- the same as 5428 at 5V (4.5Vmin)
- up-to 45MHz dotclk (1024x768, 60Hz interlaced) at 3.3V

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14.Power Management

- Mixed 3.3V and 5V operation: memory, host and flat panel independent VDD
- Green-PC spec support. **Priority: B**
- Stand-by Mode with internal stand-by timer (as in 6235)

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- Suspend Mode I/O or pin in all modes (LCD, CRT,Simulscan)
- *Light Sleep ?? - better not for this chip as it requires too much h/w Priority: F*
- Panel Power Sequencing: automatic or under I/O control (as in 6235)
- Reduced Active Power in Panel Only Operation: < 60mAmp @3.3V **Priority:A**
- Reduced Suspend Current: < 0.5mAmp. **Priority: A**

2.1 Inputs from the Nordic-1M Features Meeting of 09/10/93

- 24bit DAC if not too expensive (VAR)
- mclk @5V max 65MHz, @3V max 50MHz
- vclk and fpvdclk @5V max 85MHz, @3V max 65MHz
- **panels:**
  - TFT 1280x1024? ##, **1kx768 ##, 800x600 ##**, 640x480
    24bit,18bit, 12bit, 9bit color, 6bit mono
    NEC analog output? ##
  - STN 800x600 dual scan color, 640x480 ds color 16bit
    640x480 ss color 8bit
    640x480 mono bit 8bit and 4bit
  - horiz ## and vertical centering
  - normal 9dot font in 800x600 text ##
  - simulscan for 800x600 and 1kx768 panels ## (need to run all modes at 800x600 or 1024x768 rezolutions -> option to clock panel till h&v Blank)
  - support for two alternate fonts 10x24 for 800x600 (10x18 actual with spacing) and 12x25 for 1kx768 ## difficult !!
  - h&v text expansion in 800x600 and 1kx768 panels ## ?
  - color text enhancement ## : bright white instead of white
  - *on chip cross-talk reduction ##* ? - any improvement ?
  - *shading look-up tables ##* ? - only if not too large
- ***NO Whisper support even on the bus side - out !***
- ***NO one 256Kx16 DRAM support - out !***
- **h/w icon support:** with h/w cursor, up to 4 simultaneously. Horizontal position controlled in increments of 64 pixels.
  Icon attributes: off/on, 4 colors/3colors + transparent, no_blink/blink, (simple/double).
  H/W cursor goes over the h/w icon (visually). Uses independenly mapped color in RAMDAC RAM. Start at scan-line 64.
- PC98 integration? ## - to be negotiated
- reserve pins for SDRAM-s and CDRAM-s ##
- ***NO true dual display***!

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2.2 Inputs from Compaq 09/10/93

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- 50MHz 486DX bus
- 75Hz refresh rate
- **need one 256Kx16 support with Audio and some video for Contura - build one motherboard for Contura and LT Lite. Two DRAM-s only on LT Lite.**

- think that 8KB/buffer of audio buffer is not enough
- want to use Analog Devices for Audio
- No clear winner on conpression. They are watching. Need Indeo driver
- Play-back zoom is required. At least pixel replication.
- Very interested in Compressed Live Video. WAnt to talk more.
- need h/w icon 64x64 with 3col+transparency or 4 color. with pixel replication to 128x128.

2.3 Inputs from AST 09/15/93

- They prefer horizontal icon

2.4 New Features as of 10/04/93

- 4bit/pel packed support for Windows Chicago
- 8bit/pel video out to the Feature Connector for conversion to NTSC-out with Nordic running 640x480 interlaced mode.
  Another idea was to use some of the panel outputs in this case and extend the data out to 16bits.
- The h/w icon can be horizontal or vertical using the Motion Video Window as implementation vechicle -> is it worth?
- IBM Raleigh asked for 12 and 16dots wide fonts for h/w assisted Kanji. 10/04/93
- IBM Raleigh asked for 8bit monochrome TFT panel support. 10/04/93

3.0 Important Additions to 5428 Data Base

1. **32 bit CPU Data bus in VESA VL bus support**
2. **PCI bus support**
3. **Mono and color, STN and TFT Flat Panel support (incl. hfb).**
4. **Live video in a true color window with Windows running in planar VGA mode, without a video port (using PCMCIA standard bus and Sasha's decompression technique).**
5. **CINE PAK decompression accelleration**
6. **Audio Port support for CS4215**
7. **Power Management: panel power sequencing, stand-by mode, suspend mode**
8. **Mixed Voltage, 3.3V operation and low active/suspend/standby power**
9. **h/w icon support, with a h/w cursor support**
10. **BLT performance improvements: Memory Mapped BLT I/O, patternning, 16 byte Source buffer**

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11.*[dual display 1024x768 on CRT with 640x480 on LCD, using the same RAMDAC] - if decided to do now*

4.0 Detailed List of Features

4.1 WAS: On the Cross Talk Reduction Technique -> not in - 1M

This part was deleted from Nordic-1M spec starting rev. 3.8 (09/11/93).

4.2 Green PC Spec Support (Based on VESA DPMS Proposal 1.0p rev. 0.53p)

This specification refferes to CRT Monitor power management. Additionally, Nordic will

TABLE 1. Display Power Management Summary

State	HSYNC	VSYNC	Video RGB	Compliance	Power Savings	Recovery Time
CRT On	Pulsese	Pulsees	Acuve	Mandatory	None	NA
CRT Stand-by	No Pulses	Pulses	Blanked	Optional	Minimal	Short
CRT Sus-pend	Pulses	No Pulses	Blanked	Mandatory	Substantial	Longer
CRT Off	No Pulses	No Pulses	Blanked	Mandatory	Maximum	System Dependednt

control DAC power consumption. These power management CRT Monitor states are not necessarily related to the graphics controller power management states.

We'll define 2 bits - GRE[2:1] (the same as Alpine) that control HSYNC, VSYNC and DAC Power Off signal (or Blankn to the DAC).

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TABLE 2. GRE[2:1] Effect

GRE[2:1]	CRT State	Vsync	Hsync	DAC Power	Nordic Power Management State
0	On	pulsing	pulsing	on	active
1	Stand-by	pulsing	static at MISC[6] inactive level	off	active
2	Suspend	static at MISC[7] inactive level	pulsing	off	active or stand-by
3	Off	static at MISC[7] inactive level	static at MISC[6] inactive level	off	active, stand-by or suspend

If Nordic is in its own Suspend mode, the BIOS should program GRE[2:1]=3 to put the monitor (if any) in the Off state.

If Nordic is in its own Stand-by mode, CRT Suspend mode should be forced bt the h/w, as stand-by is a timer driven mode and no s/w gets to play.

If Nordic is in LCD only, the BIOS should set GRE[2:1] to 3 to power off the CRT that may be connected to the notebook computer.

If CRT only mode and CRT is in stand-by or suspend, the BIOS may reduce the video clock and even memory clock frequencies after saving the current values.

Except for the above restrictions, CRT Power Management modes are not related to Nordic power management modes: they can be independently programmed.

If MISC bit is programmed for positive polarity, the SYNC signal will be stopped L, otherwise it will be stopped H.

4.3 Play-back Decompression Accelleration (applicable to Cinepak as well as other compression standards) - old, kept here only for reference

4.3.0 The problem

a) When playback data is compressed on a CD ROM. it is encoded in 24bit/pel YUV with crominance sub-sampling. Due to CDROM reduced bandwidth the display window is 160x120 or 320x240. If this compressed data is decompressed at full pixel depth. it should be displayed as 24bit/pel RGB window under MS Windows As the play-back data is sent to the graphics controller from the CPU bus, it has to be placed in Video Memory in 320KB.

A standard VGA controller or even GD5428 are able to display the 24bit/pel play-back window only if MS Windows is run in 24bit/pel mode (for instance 1024x768 24bit/pel or 640x480 24bit/pel) by the driver. Under these conditions, the CPU will have to write the un-compressed 24bit/pel play-back data in the appropriate position in Video Memory, contigouus to the entire displayed data.
So, in order to display 24bit/pel in a play-back window, GD5428 needs the driver to run 24bit/pel at the maximum display resolution.
But, in order to run 640x480 at 24bit/pel we need 921.6KB of Video Memory and in order to run 1024x768 24bit/pel we need 2359.296KB of video memory. (Please note that 2M of memory has 2097.152KB).
Also, when running windows in 24bit/pel mode the performance will decrease 3 or 4 times relative to 8bit/pel mode, especially when using DRAM as Video Memory.

b) When running through MS Windows GDI, the driver can play-back data at 15fps or less (with a 486 33MHz). It is desirable to play-back data at 30fps.
This can be accomplished today only if the driver does not go through GDI.

c) If a picyure was stored on CDROM at low resolution (160x120 or 320x240) and it needs to be "zoomed", it has to be interpolated both horizontally and vertically for good picture quality. Vertical interpolation is expensive in h/w.

4.3.1 The Generic Solution - old, here for reference only

Today's Windows Accellerators run MS Windows, including the play-back window with the same pixel depth (8bit/pel), normally going through the RAMDAC, but using a split palette approach with 16 colors reserved for MS Windows and 240 colors reserved for the play-back window. The Cinepak driver writes data in video memory in 3:3:2 RGB format

(8bits/pel) which is created by the driver. Because of the s/w overhead involved in decompression as well as the GDI overhead, it is hard to go beyond 320x240 clips at 15fps, though the display quality is much lower than what Cinepak could achieve (240 colors versus 16 million colors).
To run Cinepak with 24pit/pel resolution, today's graphics controllers would require to run MS Windows in 24bit/pel mode, requiring almost 1MB in 640x480 and over 2MB-s in 1024x768 modes.

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A graphics controller that could run MS Windows in 8 or 16bit/pel mode while displaying only the play-back window in 24bit/pel mode would increase significantly picture quality without degrading too much MS Windows performance with play-back. would reduce significantly the amount of Video Memory required for the same picture quality and would allow a higher frame rate for the play-back.

Further, if the play-back data is stored in Video Memory in a semi-compressed format that requires less than 24bit/pel this would further decrease the Video Memory requirements and it may even reduce the video memory band-width requirements.

When zooming the play-back window from 160x120 to 320x240 or higher it is important to interpolate. Vertical interpolation can be done in s/w but with a relatively large overhead. It may be possible to do vertical interpolation on key frames, but there is no practical way of doing vertical interpolation on inter-frames either in s/w or with h/w assist on the CPU write side of the graphics controller. If s/w driven vertical interpolation on key frames is not a solution, then vertical interpolation can be only achived in h/w on the CRT read side and this requires either one or two 16bit/pel line buffers or a big penalty on video memory bandwidth (the equivalent of reading 32 or 48bits/pel).

Horizontal interpolation can be done before play-back data is displayed, without s/w help.

Please note that there are multiple ways to solve the play-back problems. In Nordic-1M we'll try to strike a ballance between the complexity of the h/w solution and the quality of the play-back image.

To a large extent, the solution adopted in Nordic-1M will be generic, not tied to Cinepak, though it will be first applied to Cinepak.

4.3.2 Nordic-1M old Play-back Accelleration Solution -> canned, kept here for reference

a)Nordic-1M will run Cinepak at 1:1 scale exactly the same way as today's graphics controllers: in 8bit/pel MS Windows with 8bit/pel (3:3:2 RGB) play-back window.

b)Nordic-1M will run 1:2 scale (zoom) in 8bit/pel 1024x768 MS Windows with 24bit/pel (8:8:8 RGB) pixel depth in the play-back window, horizontally interpolated and vertically doubled. Play-back data will be stored in video memory as 16bit/pel (Y0 U01 Y1 U01).

c)Nordic-1M will run at 1:1 scale in 16bit/pel 1024x768 MS Windows with 24bit/pel pixel depth in the play-back window. Play-back data will be stored in video memory as 16bit/pel (Y0 U01 Y1 U01). This mode is good for programs that store data in 320x240 format.

Because today large play-back windows look bad, while small ones look OK, this solution will improve picture quality to a large extent.

Concerns:

Many play-back programs today don't even have a zoom option. To this extent, mode "b" may not be needed.

Mode c could be implemented today with 16bit/pel RGB (555) in s/w and the only improvement we provide is 24bit/pel capability and h/w color conversion (some level of accelleration). So mode "c" may not be needed as a special h/w.

If this is the case, maybe we do not need to do anything in h/w for Cinepak !

One idea: should we run 24bit/pel MS windows stored in 4:2:2 (Y0 U01 Y1 U01) format? This will allow us to run 24bit/pel MS Windows and use 16bit/pel memory space with no loss of quality. The windows driver could compress the data and the h/w could decompress it.

4.4 Nordic-1M Motion Video Architecture

Sasha Eglit, Rakesh Bindlish, Vlad Bril and Dave Keene are important contributors to the Motion Video Architecture definition.

4.4.0 The Problems to Solve & Generic Solutions

Nordic-1M is supposed to support CDROM play-back and live-video under Microsoft's Video for Windows. With all of today's VGA Compatible Graphics Controllers, the play-back picture pixel depth has to be the same as the surrownding MS Windows pixel depth. In other words, we have to run MS Windows in a 24bit/pel mode in order to display 24bit/pel in the play-back window.
The only way we can run today live video is from a Video Port (= Feature Connector). In this case we'll use an overlay or a color key to define the live video window.
Due to CDROM player, s/w interface complexity, CPU bus and Video Memory limitations, only small clips at 15fps or less can be playd-back today. So today we need a lot of Video Memory to run small clips in slow motion at low rezolution. Nordic-1M will try to use less Video Memory, increase the clips size, their resolution and speed.

Nordic-1M is supposed to support:

- accellerated play-back for all popular CDROM compression standards, especially Cinepak and Indeo
- live video from a PCMCIA card in a system with a standard PCMCIA host adapter, for a "Multimedia-Ready Notebook Computer"
- live video from a Feature Connector, preferably VESA Advanced Feature Connector compatible, for a Multimedia Notebook Computer with direct NTSC input (full mother-

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board solution).

What will Nordic-1M bring to the Video plate:

A. Nordic-1M will break the dependency between the pixel depth of MS Windows and the pixel depth of the live-video / play-back window. By doing so, Nordic-1M will be able to run 24bit/pel LV/PB while running MS Windows in 8bit/pel or 4bit/pel (even planar) This will lead to high quality live-video and play-back, while minimizing Video Memory requirements.

B. Nordic-1M will further reduce Video Memory requirements as well as Video Memory Bandwidth requirements by storing data in compressed form. 4:2:2 YUV (16bit/pel), 4 1 1 YUV (12bit/pel) or Sashapak YUV (2.6bit/pel)

C. Nordic-1M will define one architecture and work-frame to run both play-back and live-video in a unitary way for both s/w and h/w.

D. Nordic-1M will support up to two active LV/PB windows at the same time.

E. By providing h/w YUV->RGB conversion and 1:2 zoom Nordic-1M will accellerate playback for most standards, but mostly for standards that allow us access to their decompressor like Cinepack (for whose decompressor we have a licence).

Nordic-1M will not provide Cinepak specific accelleration (custom BLT).

On the Live Video from Feature Connector (or Video Port)

Due to pin-out limitations, the VAFC implementation has to be limitted to 8 pins of data requiring external muxing of 16bit data to Nordic. Further, the VAFC solution will be restricted to 5428 type support: overlay and color key (no memory video port). The only additions to the 5428 support will be the internal YUV-> RGB converter able to accept sequential 4:2:2 YUV (16bit/pel in avarage: Y0,U,Y1,V) and display it as a 24bit/pel RGB in the overlay/color-key window. We may also support horizontal 1:2 zoom with avaraging. Nordic-1M will be back-wards compatible to 5428 and it will support also 16bit 5-5-5 RGB Sierra and 5-6-5 RGB XGA pixel formats. As in 5428, live video from the Feature Connector can be executed only from mode 5F (640x480 256 colors).

In the following we will refer mostly to the other two modes of operation: play-back and live video from a PCMCIA card, which we'll call compressed live video, because due to PCMCIA bus bandwidth limitations, we assume that video data received by Nordic is compressed with Sashapak (see Sashapak detailes further in this spec). Please note that due to its huge advantages, it makes sense to use Sashapak as a mother-board solution too. The main reason we continue to support the Feature Connector based live video is the availability of drivers for 5428 which will give Nordic an early start in the live video arena.

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Video Memory Band-width Constraints

Please note that, even with a 32bit wide Video Memory, there are severe memory band-width limitations when running 16bit/pel and 24bit/pel graphics modes.

Assumming that Nordic-1M does 8 CRT fetches in a row and 1 CPU cycle, for a CRT or TFT panel, here are the minimum frequency requirements for memory clock frequency at different rezolutions and pixel depths:

24bit/pel:
R+7P+R=12m+14m=26m with 1 CPU cycle per CRT FIFO fill fetches data for 32B/3B=10pixels
R+7P = 6m+14m = 20m with no CPU cycle during non-display time
min mclk freq = 65MHz / 50MHz @ 640x480 -> Nordic-1M upper limit at 5V CVDD
= 104MHz / 80MHz @ 800x600 -> too high
= 169MHz / 133MHz @ 1024x768 60Hz -> too high

16bit/pel:
R+7P+R=12m+14m=26m / R+7P = 20m fetches data for 32B/2B=16pixels
min mclk freq = 40.6MHz / 36MHz @ 640x480 -> OK even at 3V
= 65MHz / 50MHz @ 800x600 -> Nordic-1M upper limit at 5V CVDD
= 105MHz / 83MHz @ 1024x768 60Hz -> too high

12bit/pel:
R+7P+R=12m+14m=26m / R+7P=20m fetches data for 32B/1.5B=21pixels
min mclk freq = 30.9MHz / 23MHz @ 640x480 -> OK even at 3V
= 49.5MHz / 38MHz @ 800x600 -> OK even at 3V
= 80.4MHz / 64MHz @ 1024x768 60Hz -> too high

8bit/pel:
R+7P+R=12m+14m=26m fetches data for 32B/1B=32pixels
min mclk freq = 20.3MHz @ 640x480 -> OK even at 3V
= 40.6MHz @ 800x600 -> OK even at 3V
= 52.8MHz @ 1024x768 60Hz -> OK at 5V

We may conclude that Nordic-1M will be able to run 24bit/pel only at 640x480 rezolution, 16bit/pel up to 800x600, 12bit/pel up to 800x600 and 8bit/pel up to 1024x768 rezolution. These results apply only to CRT or TFT and single scan STN panels.
Please note that for dual scan STN panels the memory requirements increase significantly.

These severe memory bandwidth limitations lead us to attempt to minimize video memory traffic. If we store **Cinepak data in 4:2:2, with an avarage of 16bit/pel**, independent of Cinepak window size, **Nordic-1M will not be able to run Cinepak above 800x600.** Any attempt to execute vertical zoom with interpolation, even with two points interpolation will further aggravate this memory band-width bottleneck. The next step should be 100MHz SDRAM-s with a large CRT FIFO (32x32) or 64bit wide memory data bus. These considerations apply to any playback compression standard that stores data in video-memory as 16bit/pel in avarage. The key to a successful compression standard would be one that does decompresssion on the CRT memory read and stores data in memory as 8bit/pel or less, in avarage.

As we store live video at 2.6bit/pel and fetch it as if it was 8bit/pel with Sashapak, Nordic-1M should be able to run live video even at 1024x768.

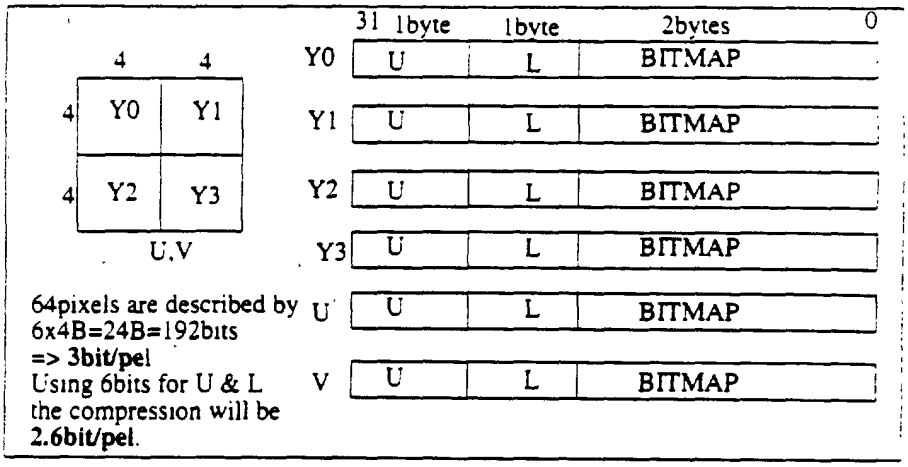
If we defined a new CDROM play-back standard based on Sashapak, then we could run even 1024x768 with 24bit/pel accuracy and keep it memory as an 8bit/pel. **Keith and Ken are actually working on it, with Sasha's help.**

4.4.1 On Sashapak

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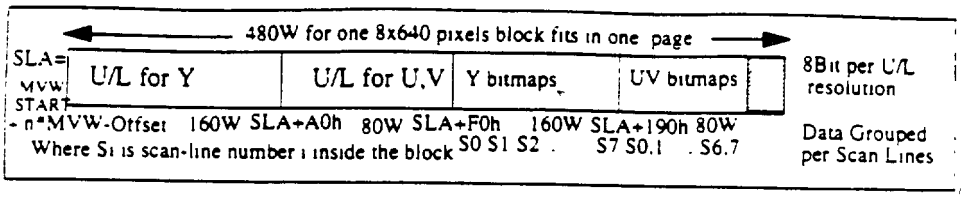
Sashapak is a highly assymetric, lossy "Block Truncation" compression algorithm optimized for visually equivalent image processing.
Data is proccessed as Y,U,V one byte each. U and V are sub-sampled, characterizing one 8 by 8 pixel array, while Y is characterizing a 4x4 pixel aray. Actually one of two values is assigned to each pixel inside the 4x4 (for Y) and 8x8 (for U and V)
At compression time, the compression chip determines a threshold and two values U&L for each group of sixteen (4x4) pixels. This way all pixels above threshold will be assigned the value U, all pixels below threshold will be assigned the value L



At decompression, the bitmap will control a mux between the U and L values. This way the decompression is straightforward.
The main drawback of this approach is that a BITMAP contains Y data from 4 scan lines and U,V data from 8 scan lines. When data is read from memory to be displayed only data from one scan line is used. Similarly the U/L values apply to several scan-lines and the same value will be read in each scan line. The same data will be read again and again in each scan line raising the actual memory bandwidth requirements to an equivalent of 16bit/pel map.
In order to overcome this problem and reduce memory bandwidth requirements, Sasha proposed a **scan line oriented, segregated mode of data organization**. This would require the Sashapak compression chip to write compressed data in a specific way puting the strain on the compresion chip address generator. The basic principles of the new organizations are:
1. Data is organised in the MV Window in chunks of 32 sequential pixels.
a)For **8bit U/L resolution**, as one Y covers 4 pixels, 8 U/L sequential values are needed, 16bits each -> **8x16/32=4W** (8x12/32=3W for 6bit res. U/L) (where W is a 32bit word).
b)U and V U/L data is packed together in the same word (16bits for U U/L and 16 bits for V U/L -> total 32bits=1W) and as one pair of U and V applies to 8pixels, 4 such values are needed for 32 sequential pixels -> **4x32=4W**. (4x12x2/32=3W for 6bit res. U/L)
c) The mask data is also scan-line oriented: all 32bits of Y mask of sequential 32pixels are placed in one 32bit word and due to sub-sampling on U and V, all 32bits of U and V mask of sequential 32pixels are placed in one 32bit word. So in 2W data for 32 sequential pixels on one scan line is packed. -> **2W** (the same for 6bit resolution for U/L)

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d) For 640x480 window size, even at 8bit U/L resolution, data for 8 scan-lines fits in one DRAM page (symetric DRAM-s assumed): 320WY+80WU+80WV=480W < 512W page



f) The key to memory bandwidth optimization is the fact the the compression chip will organize data sequentially over 32 pixels instead of 8. This will be done for the mask bits which will be organized sequentially by scan line and for the U/L data. This way a 32bit word of Mask data contains only information for the current scan line and no extra memory fetches are required. The main reason we segregate U/L for Y and U/V is the fact that we want to use 6bit U/L. In this case it is easier to identify the proper U/L info chained within 32bit words if the words are sequential and we have a fix relationship between their address and the 6bit U/L quantities.

g) If we calculate now the amount of data we need to fetch to display 32 sequential pixels:

- for 8bit per U/L: 4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B
  --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
- for 6bit per U/L: 3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B
  --> 32B/32pixels = 8bit/pixel

This is a very good data fetch ratio, much better than the 16bit/pel we'd get without the optimization.

g) When reading data from the Motion Video Window the controller will generate the following sequence of addresses, all of them in the same DRAM page (8bit per U/L):

- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset, +1, +2, +3
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h, +1, +2, +3
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h
- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset+4, +5, +6, +7
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h+4, +5, +6, +7
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h+1
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h+1
- now the MVW FIFO is full.
- chunks of ten 32bit words will be proccessed for every 32pixels displayed
- the MVW FIFO gets empty after the first 10 words being read for decompression and display.

Please note that all data for every 8 scanlines starting from the top of the MVW is in the

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same DRAM page.
Because we have to fetch the MVW Data before we start displaying it, and because at that time the CRT FIFO does not empty as fast as it is needed (unless MS Windows is running at the same pixel depth as the MV Window), it is necessary to have a separate FIFO for the MVW or at least half the FIFO (at least 10W for 8bit per U/L and at least 8W for 6bits per U/L)
h) When we run 6bit per U/L, because the Video Memory band-width requirements are as if we were running 8bit/pel, we could do vertical zoom with avaraging But there should not be a need for zoom with Live Video because there is enough CPU and memory band-width to run 640x480 windows even when MS Windows is run as 1024x768 4 or 8bit/pel

Conclusion: With Sashapak we can get data organized in memory such that the memory bandwidth is as for 10bit/pel (8bit U/L) or 8bit/pel (6bit U/L) pixel depth. The actual memory area will be close to 3bit/pel or 2.6bit/pel depending on the resolution of U/L values - 8 or 6bits per value.
Please note that the memory area will be slightly larger due to the fact that we use only 480 words in a page of 512.

4.4.2 YUV to RGB Conversion Algorithm

The ideal YUV to RGB transformation is:
R=Y+1.37V
B=Y+1.73U
G=Y-0.699V-0.336U

After defining an objective way of measuring color error, Sasha came up with the following Conversion algorithm:
R=Y+1.375V=Y+1 3/8 V
B=Y+1.75U=Y+1 3/4U
G=Y-0.375U-0.75V= Y-(3/8U+3/4V).

This algorithm can be implemented with 8 9bit adders and it should support excess 128 or two's complement U,V formats (U,V may be negative while Y is always positive).
This algorithm will be used with Live Video.
For Cinepak, the YUV->RGB converter will be reconfigured to the Cinepak YUV->RGB conversion rule:
R=V+Y
B=U+Y
G=Y-V/2-U/4

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4.4.2 Motion Video Architecture Functional Blocks

Instead of treating play-back and live-video as two separate modules, we'll isolate several generic functions to be used by both:

- Display Window Generation Block:
allows s/w to define one or two play-back or live video **window(s)**
The MV Window is defined in memory cycles relative to the start of line in horizontal and frame in vertical direction. Horizontally the unit of measure is different outside relative to the inside of the window: the horizontal window start coordinate is expressed in memory cycles for the surrounding pixel depth (MS Windows pixel depth, normally 4 or 8 bit/pel), while the width of the MVW is expressed in memory cycles for the MVW pixel depth (8bit RGB, 16bitRGB, 422YUV spacial, 422 YUV linear, 411YUV linear, Sashapak).

- **XS** = MVW Horizontal Start Coordinate (in surrounding pel depth memory cycles)
The horizontal position is programmed with 8 pixel resolution (0,8,16,... pixels starting from the left side of the screen)
XS register CR34[7:0] -> 8 bits
(up to 1K pels in increments of 8 pels)
To get an early warning, we will require XS to be programmed 8 pixels less than the actual position: 0 is zero, 1 is 16pels, 2 is 24 pels,...
- **XW** = MVW Horizontal Width (MVW pel depth memory cycles)
XW register CR35 [7:0] -> 8 bits
(up to 1K pels in increments of 8 pels)
To get an early warning, we will require XW to be programmed 8 pixels less than the actual width: 0 is zero, 1 is 16pels, 2 is 24 pels,... width.

- **YS** = Vertical MVW Start (in true scan-lines not affected by scan-line doubling or panel vertical expansion)
10 bits in CR36[1:0] (msb-s) and CR37[7:0] (lsb-s).
- **YE** = Vertical MVW End
(all bits are programmed, in true scan lines)
10 bits in CR36[3:2] (msb-s) and CR38[7:0] (lsb-s).
- **SAdOf=** Surrounding Address Offset (a number to be added every line to the surrounding CRT Address Counter value to allow it to jump over the MVW without counting through it. This allows calculating the surounding restart address.) This number depends on the surrounding mode resolution. Assuming a maximum line of 1024 pels, in increments of 4 pels per address (8bits/pel), 256 addresses is enough -> 8bits.
8bits in CR39[7:0]
- **WMAdS** = MVW Memory Address Start in increments of 16KB = 4KW (a phisical address 00000:3FFFF for 1MB or 00000:7FFFF for 2MB Video Memory).
7bits in CR3A[6:0]

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- **WMAdOf = MVW Memory Address Offset** (A number to be added to the current MVW Start Address to get the next MVW start Address). Having this s/w model allows panning through a large image for the MVW. The actual image stored in memory may be as large as 1K pixels

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at 16bit per pixel (2 per word) -> 9bits.
9bits -> in CR36[4] (msb) and CR3B[7:0] (lsb)

Because the CRT Address Counter counts surrounding memory cycles. during the MVW display it would count a wrong number corresponding to the MVW pixel depth. To avoid this wrong count, the CRT Address Counter is stopped while MVW is displayed and loaded with the value corresponding to the end of MVW and restart of the surrounding display. As this address value changes every line, an offset is specified and will ba programmed by the MS Windows driver depending on the MVW size and pixel format The horizontal size of the window is controlled by a different counter counting to XW During the MVW display the adddress will be generated by the same CRT Address Counter which will be loaded with a MVW Memory Address Start (WMAdS).

- **XW8P = MVW Horizontal Width in 8 pixel units**. Defines the size of the window in 8 pixel units. It is used to terminate the window horizontally. It may require to program the value minus one or two. To be Defined Later. Register CR3D[6:0] will contain this value.

Every scan-line

MVW Scan-Line Start Address = Previous Scan-Line MVW Start Address + WMAdOf

Scan-line doubling for "zoom" should be taken into account when designing the MVW Architecture: on the address generation block.

- **Off-screen MV Memory Addressing and Access Control.** This includes data type tag generation based on MV memory Address and the circuitry placing the tags in the CRT-FIFO. This block has provisions for scan line replication by repeating the MV address generated on the previous scan line of the MV window (only).

As Cinepak needs 4:1:1 rectangular format the MV Memory Address Counter needs to count in a non sequential way:

Y0Sn Y1Sn Y2S(n+1) Y3S(n+1) U V

implies an address counter that can skip over two numbers, or maybe **a second address counter that starts counting from 2 instead of zero.**

- **One tag bit is generated based on CRT Address and is 1 if the data in the CRT FIFO is from the MVW, other-wise is 0.** This tag bit, called the **steering bit** will be delayed through the entire data path and end up controlling the final video data mux just before the DAC.

Other tag bits called "data-type" tag bits encode the type of 32bit word in a given data format and are used by MVW Decoder/Serialiser to steer CRT-FIFO data at CRT-FIFO read.

For instance, in 4:1:1 linear data format, data is stored in memory and in the CRT-FIFO as Y0Y1Y2Y3 U03V03Y4Y5 Y6Y7 U47V47, 3 groups of 32bits. Two "data-type tag bits will mark the three types of 32bit words so that steering logic knows where to place the three words in the data serialiser.

Similarly Sashapak will need 3 "data-type" tag bits to encode 8 32bit words (for 6bit per U/L) or 4 "data-type" tag bits to encode 10 32 bit words (for 8 bits per U/L).

16bit RGB 5:6:5 and 5:5:5 and 8bit RGB 3:3:2 can either use the **standard VGA data**

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path, which in 5428 was extended to 16bit wide (used for 16bit/pel 1kx768 interlaced) or the new data path, **if a phisically new data path will be actually created**.

- **MV Data Path .** This is area wise the largest piece. It consists of a new 16bit wide data-path with the same delay as the VGA data path, that takes MV data from the MV prefetch cache and the CRT FIFO, treats it appropriately depending on the MV data format encoded in the MV tags and converts it to 24 bit YUV first and 24bit RGB second. Horizontal zoom with avaraging (or maybe 5 levels of interpolation) is in this block too

- Larger (26 or 24 stages) CRT-FIFO, Variable CRT-FIFO threshold and its control. Because the MS Windows pixel depth and MVW pixel depth don't match, it is necessary to reserve CRT-FIFO space to fill in enough high pixel depth data before the MVW display starts. In Sashapak this means 10 or 8W (for 8 or 6bits per U/L respectively).

This function can be implemented as a dinamic threshold size modification of the CRT-FIFO. If the CRT-FIFO has 24 stages instead of 16 but only 16 stages are used before the MVW but it is switched to 24 when MVW fetches start, there will be 8 more stages to fill at that time ensuring more prefetched data in the CRT-FIFO at the beginning of each MVW scan-line.

In normal operation the threshold is 8 (or 6).

Here is the sequence of events that follow the detection of MVW start:

1. **Drop CRT-FIFO threshold to 1 to get immediat service & make 10 (or 8) more stages available in the CRT-FIFO.**
2. **Start fetching MVW data till CRT-FIFO is full. (BLT in progress will increase latency)**
3. **Increase threshold to 10.**
4. **Proceed as such till end MVW.**
5. **Load the CRT Address Counter with its last contents + SAdOf**

(where SAdOf = Surrounding Address Offset)

7. **Continue fetching based on the new address (start with random cycle). CRT-FIFO threshold remains the same - at least 10 or 8. CRT-FIFO size is still 26 or 24.**
8. **At the end of line, upon flushing the CRT-FIFO before prefetch, decrease CRT-FIFO size back to 16 keeping the threshold the same.**
9. **Go back to #1 for the next scan-line.**

This sequence is applied if MVW pixel depth is higher than surrounding pixel depth. If MVW pixel depth is lower than surrounding pixel depth, then the action described at #1 above takes place at the end of MVW, instead of the beginning. ***In other words, FIFO depth extension takes place when a switch from low to high pixel depth occurs.*** **If MVW pixel depth is the same as the surrounding, only the address is switched. In this case the CRT FIFO depth and the threshold remain the same.**

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- Steering logic decode the tags comming out of the special addition to the CRT-FIFO and the pre-fetch buffer and controls the decompression, formatting and serialization.

(they tell the formatter what data is Y, U or V).

- What about the video serializer load and the CRT FIFO read signal? What hapens to them when in MVW? They are one signal today.
WHEN the data path switched to display MVW data, what hapens with the VGA Video Data Path is don't care as we do not display that data, except for the h/w cursor anf the h/w icon that do not go through the standard VGA serializer. So we'll probably stop the VGA data path untill the point h/w cursor and h/w icon are combined into it, to save power, as we will stop the MVW data path when not in use, for the same reason.
So, the Video Serializer Load may be stopped while MVW data is displayed, **but the CRT FIFO read will be going on, with a frequency and shape depending on the data format loaded in the CRT FIFO for display.**
In RGB 3:3:2 8bit/pel direct color mode CRT-FIFO read will be generated every 4 vclks.
In standard RGB 5:5:5 or 5:6:5 16bit/pel modes CRT-FIFO read will be generated every two vclks.
In YUV 4:2:2 24bit/pel (Y0 U Y1 V on one scan line) the CRT-FIFO read will be generated also every two vclks.
IN Sashapak 10 (for 8bit per U/L) or 8 (for 6bit per U/L) CRT-FIFO read pulses will be generated every 32 vclks.
- The MVW Address Counter, loaded at the beginning of each MVW scan-line with a start address calculated based on the Start MVW Address and the MVW Address Offset, will count at format dependent rate for as long as the CRT-FIFO is not full. Because the CRT-FIFO will be emptied faster in the MVW (in general the pixel depth will be higher in the MVW) there will be requests for more memory cycles when displaying in the MVW

- If either h/w cursor or h/w icon are on, they should be displayed even if the direct data path is used. In this case both video data pathes will clock and the steer tag will point to the VGA data path when either h/w cursor or h/w icon or both are displayed, even on top of a MV window. Please note that neither the h/w cursor, nor the h/w icon data go through the CRT FIFO or the VGA Data path except for the final pixel address block and the RAMDAC RAM, though they have a special path in the RAM. So we could stop most of VGA data path (including the internal palette) but not all of it even if we are in 16bit/pel mode (the new one that goes through a separate 16bit data path).

- If we are in a 16bit/pel mode with no h/w cursor or h/w icon, or in a 640x480 MVW mode filling the screen, we can stop the VGA data path to save power.

- The off-screen MVW memory will be a programable start memory array normally placed towards the end of the memory, but before h/w cursor, h/w icon and the half frame buffer, even the color one. The start of the MVW memory will be programable in increments of 4KW (16KB) as a physical address -> 7bits to program.
CR3B[6:0] is the MVW Memory Array Start Address.
2MB configuration will support enough memory to support:
- one 640x480 3bit/pel window or up to two 320x240 3bit/pel (Sashapak) -> 32KW
- one 640x480 16bit/pel window or two 320x240 16bit/pel windows
(153.6KW=614.4kB out of 256KW or 512KW available depending on the memory con-

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figuration)

- all of the above at the same time up to a total of two windows though.

1MB configuration will support:

- one 640x480 3bit/pel Sashapak window or two 320x240 Sashapak windows or
- two 320x240 16bit/pel windows.

Please note that about 24KW are needed for 800x600 DS Color STN HFB. the h/w cursors and h/w icons while about 18KW are needed for 640x480 DS Color STN HFB and that

- 640x480 4bit/pel requires 38.4KW
- 800x600 4bit/pel requires 60KW
- 1024x768 4bit/pel requires 98.3KW
- 640x480 8bit/pel requires 76.8KW
- 800x600 8bit/pel requires 120KW
- 1024x768 8bit/pel requires 196.608KW

Video Motion Formats supported are:

- 8bit RGB 3:3:2 going through the palette (RGB 3:3:2)
- 16bit RGB (5:5:5 Sierra and 5:6:5 XGA) not going through the palette -> this is a 16bit/pel that does not require double dotclock !!
- 4:1:1 array converted to 4:2:2 Y0 Y1 Y2 Y3 U V -> Y0UY1V Y2UY3V for Cinepak (with Y2Y3 for the next scan line)
- 4:2:2 linear Y0UY1V from TV Decoder
- Sashapak format (we'll support only 6bit/pel)
  - for 8bit per U/L:
    4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B
    --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
  - for 6bit per U/L:
    3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B
    --> 32B/32pixels = 8bit/pixel

CR3C[3:0] will encode the pixel format for the first motion video window data.

0h = 0000 = 8bit RGB 3:3:2 going through the palette
1h = 0001 = 16bit RGB Sierra (5:5:5)
2h = 0010 = 16bit RGB XGA (5:6:5)
3h = 0011 = 4:2:2 YUV Y0UY1V
4h = 0100 = 4:1:1 YUV linear Y0Y1Y2Y3UV
5h = 0101 = 4:1:1 YUV array Y0Y1Y2Y3UV but Y2Y3 are in next scan line
6h = 0101 = Sashapak 6bits for U/L
7h = 0110 = Sashapak 8bits for U/L
8h:Fh = 0111:1111 = reserved

CR3C[4] = Enable Motion Video Window
CR3C[5] = Enable Live Video in Full Screen
CR3C[7] = MVW horizontal zoom (doubling)
CR3C[6] = MVW vertical zoom (doubling)

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Note: We will not support 4:1:1 linear from TV decoder, for design simplicity.

Memory data formats:
- 8bit and 16bit RGB, as in 5428.
- 4:1:1 Cinepak converted to 4:2:2 by writing a 4:2:2 Code-Book
first scan line -> Y0UY1V -> One 32bit Word
---
second scan line in memory -> Y2UY3V -> One 32bit Word
- 4:2:2 linear will be mapped in memory as follows:
first scan line Y0UY1V
first scan line Y2UY3V
---
consecutive data in the same scan line.

The tags that accompany the motion video data through the CRT-FIFO mark both the data format and the type of data inside the format (U/L for Y or U,V or mask for Y or U,V in Sashapak, Y0, Y1,U or V in 4:2:2).

Double Buffering for MVW Video Memory Data

In order to get a high quality Live Video full frames should be displayed at all times. This assumes that writing the video buffer and displaying it are in sync, which is normally not the case.
To solve this problem and provide a simple interface between MVA h/w and the driver, Nordic will support a double buffer approach.

Addressing with Sashapack:
Sashapack stores data for eight scan-lines in one memory page (works only with synchronous DRAM-s). But due to U,V sub-sampling diferent data types are not read from memory uniformly.
On Y U/L the first four scan-lines read at offset 0 in the page, but the second four scan-lines read at offset 50H in the page.
On U,V U/L we read the same data for each scan-line. So we repeat reading the same data at all times, for eight scan-lines. Page addresses to read are A0:EF. If the scan-line is shorter it will end sooner.
On Y Map the data should be sequential, scan-line oriented: first pixels 0 to 639 on the first scan line, than pixels 0 to 639 on the second scan line and so on till the 8-th scan line If the lines have less than 640 pixels, Sasha wants them cropped for the first 4 scan lines, and then starting again from the half for the next four scan-lines. This is in sync with Y U/L where the last four scan-lines start from mid.
On U,V Map, because of the vertical subsampling, the same data is read for two scan lines, so there are four scan-lines worth of data but each scan-line is read for two consecutive scan-lines. Even if the scan-line is shorter, there will be a gap every-scan-line: there are fix page addresses for each scan-line up to 640 pixels wide.

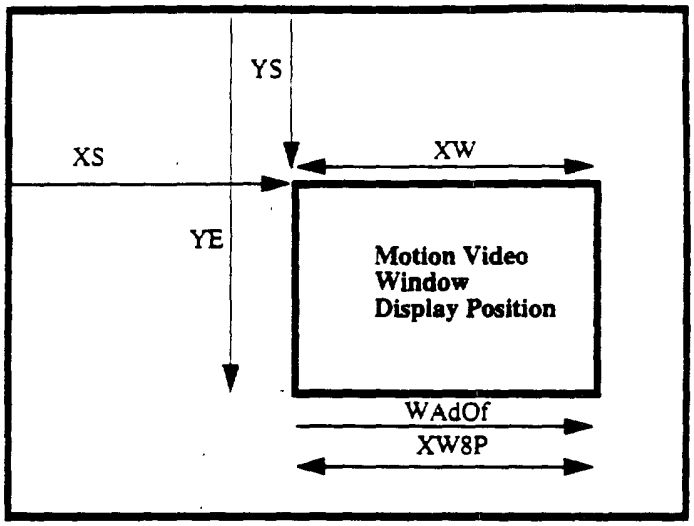
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Full Screen in a given graphics mode



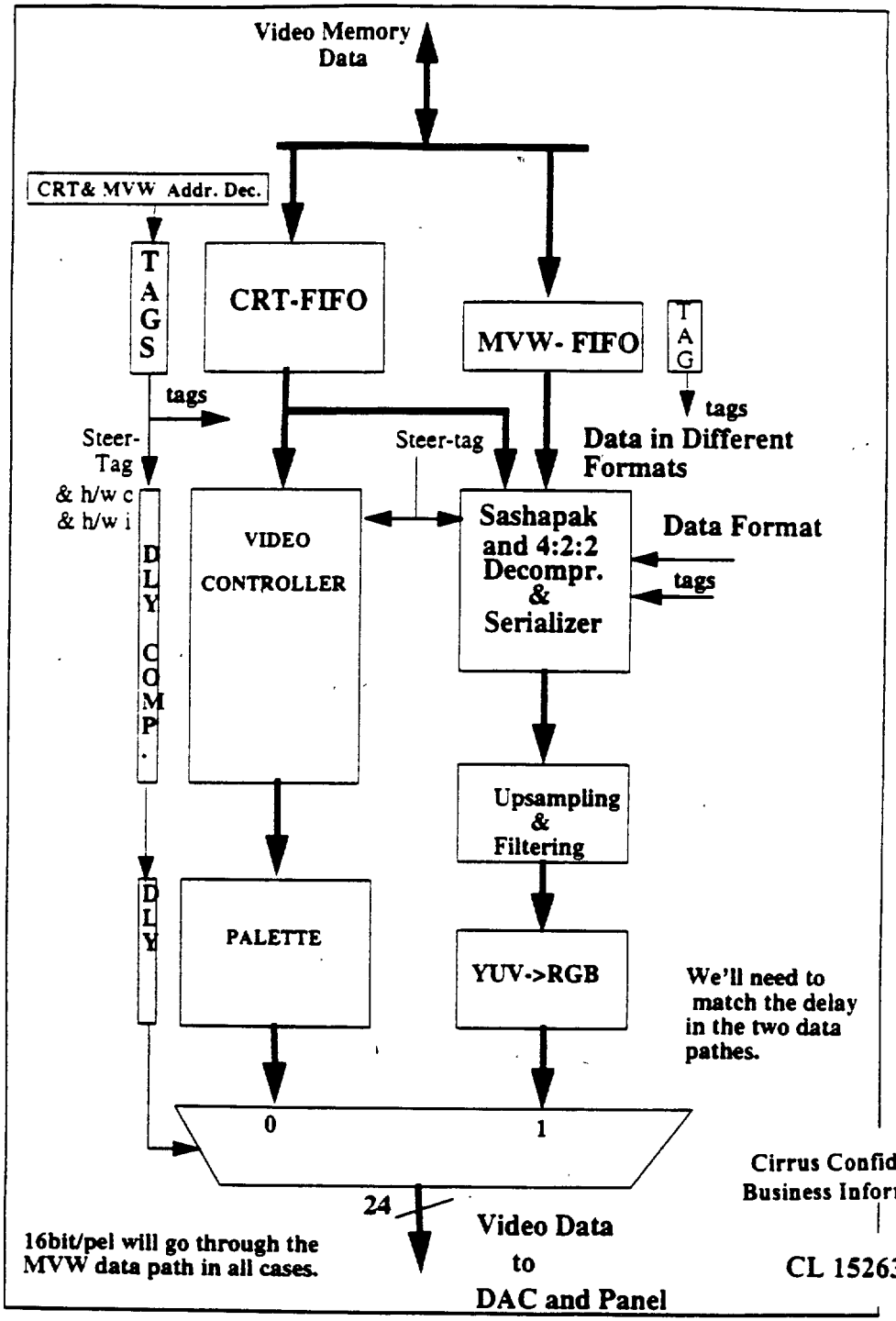
Where:

- **XS** = MVW Horizontal Start Coordinate (in surrounding pel depth memory cycles)
- **XW** = MVW Horizontal Width (MVW pel depth memoty cycles)
- **YS** = Vertical MVW Start (in true scan-lines not affected by scan-line doubling or panel vertical expansion)
- **YE** = Vertical MVW End (all bits are programmed, in true scan lines)
- **WAdOf** = MVW Address Offset (a number to be added every line to the CRT Address Counter to allow it to jump over the MVW without counting through it.
- XW8P = MVW horizontal width expressed in 8 pixel units

Please note that MVW horizontal width is defined twice in different units:
XW defines it on the memory side in memory cycles
XW8P defines it on the CRT side in 8 pixel units.

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Video Memory Data
CRT& MVW Addr. Dec.
TAGS
CRT-FIFO
MVW- FIFO
TAG
tags
tags
Steer-Tag
& h/w c
& h/w i
Steer-tag
Data in Different Formats
DLY COMP.
VIDEO CONTROLLER
Sashapak and 4:2:2 Decompr. & Serializer
Data Format
tags
Upsampling & Filtering
DLY
PALETTE
YUV->RGB
We'll need to match the delay in the two data pathes.
0
1
24
Video Data to DAC and Panel
16bit/pel will go through the MVW data path in all cases.
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4.5 Feature Connector Support

Nordic-1M will support 5428 Feature Connector so that it is compatible to Media Manager.
Nordic-1M will support VAFC (Vesa Advanced Feature Connector) in the 8bit VSVPC passthrough compatibility mode.
The main difference beteen 5428 FC and Nordic FC is the fact that 5428 FC has one EDCLKn control pin controlling the direction of the DCLK pin, while Nordic-1M as well as VAFC have a FCDCLK output pin and a FCVCLK input pin.
Dave Keene believes that 5428 FC is VAFC compatible. To ease the design, I kept 5428 FC pin names (not VAFC pin names).
On VAFC compatibility here are some comments:
- GENCLK can be applied on XVCLK if SR22[3]=1.
  But, if SR22[3]=1 (select xclk) & SR24[7]=1 (VAFC enabled), then XMCLK should get OSC and MCLK Synthesizer operates normally, except that the reference frequency comes from XMCLK instead of OSC pin. If SR22[3]=1 & SR24[7]=0, then MCLK comes directly from XMCLK pin and the MCLK and VCLK Synthesizers are powered-down !!
- GRDY signal is similar to OVRW.
- VRDY is similar to EVIDEO if EVIDEO is dinamically switched as a valid data in signal.
- EGENn is not needed if we configure Nordic-1M in the right configuration with SR22[3] (XCLKPU) and SR24[7] (VAFCPU).
- As VAFC maximum FCVCLK frequency is 37.5MHz, VAFC supports a mode in which data is sent at 37.5MHz to the DAC and it each pixel will be displayed twice if the chip is running at 75MHz pixel clock. This allows only 8bit/pel data to be displayed. To display 16bit/pel data we should use both phases of the FCVCLK and pack the data into one pixel. I think that this is already done in 5428, if not Man-Shek and Fong-Jim are modifiying the 5429 RAMDAC to support this mode -> we need to support it too
- VAFC requires FCDCLK to be switchable under s/w control beteen 1x and 1/2x the pixel clock. If we took this out of Nordic-1M data base, we should put it back, but the divide by two should affect only FCDCLK going out of the chip.

Check VESA VAFC Proposal 1.0p rev. 0.31 07/15/93 for VAFC timing info.

Nordic-1M FC Pins Functional Description

Most of this is from 542X Data Sheet page 3-26:

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VSYNC and HSYNC	TO	The standard CRT pins tri-stated when FCESYNCn is L. Thes pins have programable polarity.
FCBLANKn	I/O	BLANKn in 5428. If FCESYNCn is H, this is an output and it supplies the actual composite BLANKn CRTC signal. VAFC requires this to be the composite Display Enable (no borders). If this is the case, we'll need a bit for VAFC that puts DE = HDE & VDE inverted on BLANKn.

If FCESYNCn is L, FCBLANKn is an input and it forces RAMDAC RAM outputs to 0 (black), but it should force them black before they go to the panel.

It seems that by connecting OVRW output to BLANKn as input we can display FC data in a window - this will work though only if OVRW internally controls the pixel address mux between normal VGA data and the FC data.

FCP[7:0] I/O P[7:0] in 5428.
If FCEVIDEOn is H, these pins are outputs and represent the pixel address of the RAMDAC.
IF FCEVIDEOn is L, these pins are inputs and represent the pixel address to the RAMDAC.
CR1A[3:2] control the way the FCP[7:0] are muxed with the normal data.

FCDCLK O (the actual pin is I/O) outputs VCLK or VCLK/2 if selected through s/w.

FCESYNCn I ESYNCn in 5428. Controls HSYNC, VSYNC and FCBLANKn (H-> outputs, L-> H/VSYNC are tri-stated, FCBLANKn is tri-stated.).

Nordic does not have EDCLKn input as FCDCLK and FCVCLK are not shared.

OVRW O OVRW in 5428 = Overlay Window. **This active Low** signal, is generated by the BLANKn VT and HT logic (shared) and is supposed to be used to create an Overlay Window in which data from the Feature Connector is displayed. *I don't know why we output this signal. It should be controlling the MUX between the normal pixel address and the FC originated pixel address.*

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4.5.1 On the Video Port for TFT Panels

A Video Overlay live video solution requires a TV Decoder Chip Set, a de-interlacer (at least a line buffer, but usually a full frame buffer), a scalar/filter/color converter chip (like CL-PX0072, CL-PX0070 or the more expensive CL-PX2070). To display live video in a window at 800x600 or 1024x768 a full frame buffer is needed and some frame level synchronization needs to be achieved.

Is there a cheap way to display full screen TV on a 640x480 panel?
Is a video port a cheap system solution to the above problem?

Can we design a system that uses a universal TV Decoder like SAA7151A and feeds data directly to a Video Port that displays live video at 640x480 30fps with no additional components? This is what customers require!

Problems to solve:

1. Accept 7151 data format: 4:2:2 YUV at 6.75MHz or 4:1:1 YUV at 3.375MHz, interlaced.
2. Synchronize at frame level.
3. De-interlace. Optionally display only odd fields with scan line doubling (according to Sasha this looks better than displaying true de-interlaced picture).
4. Get enough memory bandwidth with a 32bit wide DRAM.
5. Have enough storage space on the Graphics Controller to go over the CRT horizontal non-display memory refresh & prefetch time while Live Video Data comes at normal TV display speed.

4.5.1.1 Data Format

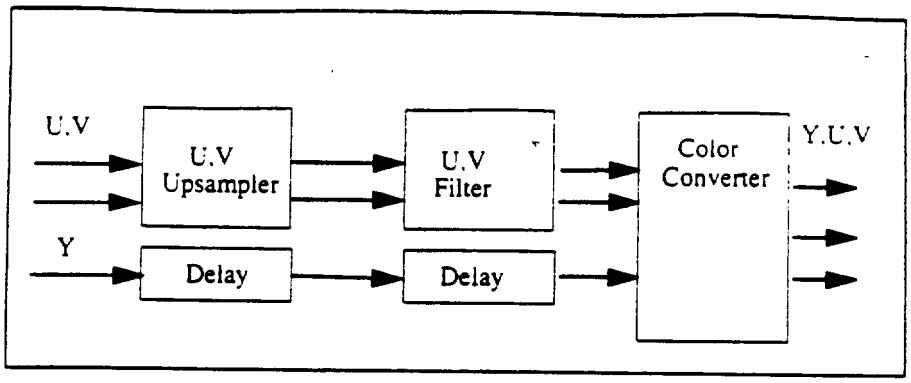
In order to accept YUV data, we need good up-sampling filters on U and V. After up-sampling and filtering we need a Color Space Converter with 2-th complement (for 7151) or excess 128 (for other TV decoders). A good 4:1:1 UV up-sampling filter is quite complex and requires many stages of pipe-lining (9 or 11) . A good 4:2:2 UV up-sampling filter requires less than 5 stages of pipe-lining.

As data is stored in TV decoder format, up-sampling, filtering and color conversion are done on the CRT read side at dot-clock rate.

Please note that 4:1:1 data requires 48 bits of storage (two data packs will fill 3 32 bit words).

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4.5.1.2 Synchronize at Frame Level

To avoid moving objects jagging we should display only full frames. In many systems today this requirement is not met. For instance play-back systems display as fast as possible without any regard for frame synchronization. According to Sasha this is not good for TV. How bad it is remains to be seen.
If the CRT/TFT display runs at 27MHz (double TV dot-clock rate) it is possible to use a double buffer scheme in which we display twice each frame while writing one TV frame in the other video buffer and alternate the two buffers. For a 640x480 display at 4:2:2 YUV we'd need 2MB of DRAM, as the buffers are embedded in the Video Memory (614.4KB per buffer needed).
Even with this scheme, external VSYNC from the TV Encoder should be used to synchronize (= reset) Nordic vertical counter, so that TV and Graphics frames start at the same time. SAA7151 outputs VS (TV VSYNC) which can be used as external SYNC by Nordic.
If only odd fields are displayed, half data is stored reducing Video Memory requirements to 307KB per frame (614KB total which fits in 1MB). This is not a bad idea especially if the picture looks better!

4.5.1.3 De-interlace

This is naturally done by writing data in the Video Memory. If only odd fields are displayed, Nordic has to determine the field boundary by counting HS (TV HSYNC) pulses.

4.5.1.4 Memory Bandwidth with 32bit Wide DRAM

There are two cases: 4:2:2 YUV and 4:1:1 YUV.

A. 4:2:2 YUV Bandwidth Requirements

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CRT-dot-clock frequency = 27MHz, TV-clock frequency = 13.5MHz
R=6m, P=2m

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a. TV-FIFO = 16 stages with 8 to write 8 to read .

CRT-FIFO = 16 stages with 8 to write and 8 to read
2xCRT-FIFO-fills + TV-FIFO-empty < 2x16 CRT-dotclks=16 TV-dotclks=1185ns
2x(R+7P) + R+7P + 3m = 3R+21P+3m=18m+42m+3m = 63m < 1185ns
mclk-period < 1185ns/63 = 18.8ns -> 53MHz mun mclk frequency

b. TV-FIFO = 32 stages with 16 to write and 16 to read.
CRT-FIFO = 16 stages with 8 to write and 8 to read
4xCRT-FIFO-fills + TV-FIFO-empty < 4x16 CRT-dotclks=32 TV-dotclks=2370ns
4x(R+7P) + R+15P + 5m = 5R+43P+5m=30m+86m+5m = 121m < 2370ns
mclk-period < 2370ns/121 = 19.58ns -> 51MHz min mclk frequency

c. CRT-FIFO = 32 stages 16 to write and 16 to read @ 27MHz
TV-FIFO = 16 stages 8 to write and 8 to read @ 13.5MHz

CRT-FIFO-fills + TV-FIFO-empty < 32 CRT-dotclks=16 TV-dotclks=1185ns
(R+15P) + R+7P + 2m = 2R+22P+2m=12m+44m+2m = 58m < 1185ns
mclk-period < 1185ns/58 = 20.43ns -> **48.9MHz min mclk frequency**

Please note that Nordic already has 32 (or 36 stages of CRT FIFO - MVA FIFO) and 24 stages of FB-FIFO (write + read). So if we use all the buffering area available we can meet case c requirements and run direct live video at 48.9MHz mclk.

d. CRT-FIFO = 24 stages (12/12)
TV-FIFO = 12 stages (6/6)
CRT-FIFO-fills + TV-FIFO-empty < 24 CRT-dotclks=12 TV-dotclks=888ns
(R+11P) + R+5P + 2m = 2R+16P+2m=12m+32m+2m = 46m < 888ns
mclk-period < 888ns/46 = 19.3ns -> 51.8MHz min mclk frequency

B. 4:1:1 YUV Bandwidth Requirements

a. CRT-FIFO = 24 stages (12/12)
TV-FIFO = 12 stages (6/6)
CRT-FIFO-fills + TV-FIFO-empty <,32 CRT-dotclks=16 TV-dotclks=1185ns
(R+11P) + R+5P + 2m = 2R+16P+2m=12m+32m+2m = 46m < 1185ns
mclk-period < 1185ns/46 = 25.7ns -> 38.8MHz min mclk frequency

Because 3x32bit house 8 pixel data, it is advisable that the number of stages in the FIFO-s are a multiple of 3 for 4:1:1.

For 4:1:1 YUV, the picture quality is not that good as for 4:2:2, the control requirements are harder to meet, the filter on U and V is expensive, but the bandwidth requirements are easy to meet.

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4.5.1.5 Covering the Memory Refresh and CRT-FIFO Prefetch Time

During each horizontal non-display time, Nordic executes memory refresh (normally 3 with an option of 1 - all random cycles), h/w icon and CRT-FIFO prefetch cycles.

At that time the TV data comes at normal rate and has to be stored in the TV-FIFO Let's see how long it takes to execute all these cycles.

a. With reference to case A.c. 4.5.1.4
(4:2:2 YUV the case that meets bandwidth requirements at 48.9MHz mclk)

x. CRT-FIFO = 32 stages, 3 refreshes, h/w icon 64x64x2 (4 h/w icon cycles)
R+31P + 3R + R+3P + 3m = 5R+34P+3m=30m+68m+3m=101m < 1185ns
-> m < 1185ns/100m=11.7ns -> min mclk freq. is 85MHz
(off by about 42mclks to get to 50MHz mclk).

y. CRT-FIFO = 32 stages, 3 refreshes, h/w icon but prefetch 16 CRT-FIFO stages (no need to fill the FIFO at the beginning of the line).
R+15P + 3R + R+3P + 3m = 5R+18P+3m=30m+36m+3m=69m < 1185ns
-> m < 1185ns/69m=17.17ns -> min mclk freq. is 58.2MHz

z. CRT-FIFO = 32 stages, 1 refresh, h/w icon but prefetch 16 CRT-FIFO stages (no need to fill the FIFO at the beginning of the line & use extended refresh DRAMs).
R+15P + 1R + R+3P + 3m = 3R+18P+3m=18m+36m+3m=57m < 1185ns
-> m < 1185ns/57m=20.78ns -> **min mclk freq. is 48.1MHz**

This case meets the minimum requirements for non-display time buffering.

b. With reference to case B.a. 4.5.1.4
(4:1:1 YUV the case that meets bandwidth requirements at 38.8MHz mclk)

x. CRT-FIFO = 24 stages, 3 refreshes, h/w icon 64x64x2 (4 h/w icon cycles)
R+23P + 3R + R+3P + 3m = 5R+26P+3m=30m+52m+3m=85m < 1185ns
-> m < 1185ns/85m=13.9ns -> min mclk freq. is 71MHz
(off by about 26mclks to get to 50MHz mclk).

y. CRT-FIFO = 24 stages, 1 refreshes, h/w icon but prefetch 16 CRT-FIFO stages (no need to fill the FIFO at the beginning of the line & extended refresh DRAMs).

R+11P + 1R + R+3P + 3m = 3R+14P+3m=18m+28m+3m=49m < 1185ns
-> m < 1185ns/49m=24.18ns -> **min mclk freq. is 41.3MHz**

Case b.y will do it for an mclk frequency above 41.3MHz.

Note: If required, we could disable the h/w Icon and h/w Cursor when in full screen live video from Video Port.

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Conclusion on Video Port Cheap System Solution

It is possible to achieve a minimum cost mother-board solution for full screen 640x480 30fps live video by interconnecting directly a digital TV decoder to Nordic Video Port under the following conditions:

1. **Prefetch only half CRT-FIFO instead of the entire FIFO**
2. **Do one refresh per line (eventually use extended refresh DRAMs)**
3. **To display 4:2:2 YUV use 32 CRT-FIFO stages and 16 TV-FIFO stages (between CRT-FIFO and MVA-Buffer we have enough storage now, but it has to be reconfigured). Minimum memory clock frequency is 48.9MHz**
4. **To display 4:1:1 YUV use 24 CRT-FIFO stages and 12 TV-FIFO stages. Minimum memory clock frequency is 41.3MHz.**

Under the same conditions, it is possible to display live video in a window with a 640x480 TFT panel, but the image has to be scaled-down and filtered with PX0070 or PX0072 - a more expensive solution. Also, during the actual live video display time, CPU and BLT will get very few cycles. This is not a factor with full screen live video as the CPU does not need to access the Video Memory at that time.

The question is now: how much cheaper is this solution relative to a full screen TV with overlay ? Sasha is working on a cheap solution with overlay.

Minutes of the Meeting on MM in Nordic in Nov. '93

With D.Keene, Keith, Del and Nordic Team on

- Video Port with 32bit memory is bwth. limitted. It is not a good solution for 32bit bus - better use Overlay or Sashapak.

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4.6 On WavePort Architecture and Audio Driver

Starting from Dave Keene's WavePort Specification, Rakesh, Sasha and Vlad came-up with some ideas which could greatly simplify the design work for WavePort, reduction the complexity and the number of gates of the WavePort.
We'll start with the small issues and move towards more important issues.

4.6.1 AUXS1 and AUXS2 Pin

A. Dave proposed to share this pin with PDN (Power Down) WavePort Pin and configure it as AUXS2 when using 4231S.
We noticed that 4231S does have a PDN pin which we'd like to use to save power
We'll put AUXS2 on another pin.

B. Dave proposed to have a fully programmable location for AUXS1 and AUXS2 CPU I/O map with a default at 530H and 388H. This is costly (4 registers and fast comparators) and very difficult to design at required speed: will slow down address range decode for I/O a lot affecting command to command parameters.
We suggest to have a fix address for these ports: 530H and 388H.
Two register bits (one per address) can disable the chip from answering to these I/O addresses.
If we are not sure where to place these ports, we can leave it as a metal option for future modification or have one more alternative for each, but the address should be fix for fast decode.
GR58:GR5B are no longer needed if this option is accepted. We'll need two bits to disable 530H and 388H address decode and eventually two other bits to select other two alternate I/O addresses. We should always decode 16 addresses: 530:53F and 388:397 (not 4 or 16).

4.6.2 WavePort R/W Buffer Location and Size

To simplify the h/w and reduce verification work-load , WavePort R/W Buffer Size should be fix: 32KB for each, enough for at least 180msec of operation -> 90msec for half buffer. Every 90msec the CPU will have to fill and/or empty half Audio Buffer (write or read respectively).
It is also possible to place the WavePort memory buffer in a fix memory location, common for both desktop and portable architectures. We could place it in Memory in the upper part
(in high address area), just before the h/w cursor. If the h/w cursor takes the upper 16KB of the memory, we could use the next 64KB for the WavePort buffer.
Going down in memory, in Nordic we'd place the h/w icon in the next 16KB (only 4KB needed now... but leave some room for expansion) and the Half Frame Buffer for monochrome and color panels in the next 32KB and 96KB respectively.

Total:

96KB for CRT/TFT/SS STN panels,
128KB for monochrome panels and
192KB for dual scan color STN panels.
out of 1MB or 2MB memory available.

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When the memory is expanded, all these fix components should move automatically in the upper side (towards the end of memory).

This places the WavePort buffer at:
- **for 1MB** of memory by 32 (256Kx32 -> 00000:3FFFF) **3B000:3EFFF**
- **for 2MB** of memory by 32 (512Kx32 -> 00000:7FFFF) **7B000:7EFFF**

If we adopt this solution, GR43 is not needed.

4.6.3 On Host Access to WavePort Buffer

In order to ensure independence between the Graphics s/w Driver and the Audio Driver, taking into account AVGA limitation of no CPU accesses during BLT operation, Dave proposed a separate path for WavePort Host Accesses. This involves a separate 4 stage by 32bit write and read buffer and separate arbitration for the Audio cycles. The buffer is shared by WavePort read and write operations and an I/O to an extension register bit is needed in order to switch from a read operation to a write operation or vice-versa.
Dave also proposed that the host address be dependent on GR6 CPU address map bits such that the video and audio address maps don't overlap.
Please note that this approach prevents debug with a Hercules card when in graphics.

In the following an alternate scheme is proposed:
- There is one register bit that enables WavePort memory write accesses and one register bit that enables WavePort memory read accesses. When one of these bits is asserted ,the chip expects only host accesses for the WavePort: the host address will be automatically translated to a memory address inside the WavePort buffer. The access will be fully linear, 32bit only, **graphics mode independent** (like in extended 8bit/pel). The Graphics block will be forced to this mode and all planes will be automatically enabled. On the Host side, the WavePort buffer will be placed always at A000:0000 - A000:FFFF -> 64KB with 32KB for read buffer (the upper side) and 32KB for write buffer (the lower side of this 64KB segment).
- The CPU Data Path is the same as for any other CPU cycle: no special FIFO, no special arbitration are required. The Audio Driver and The Graphics Driver communicate through interrupts: There is an interrupt for BLT completed (Dave's idea when presented with this proposal) and an interrupt for Audio Buffer Full (or Audio Transfer Completed). When the BLT is completed, if Audio is enabled on the chip, the BLT Completed interrupt allows the Audio Driver to check if there is any need to service the Audio and vice-versa. If possible, the Graphics driver should restrict the extent of the BLT operations to less than 160msec or so (leaving at least 20msec to start filling the WavePort buffer).

- There is no on chip CPU WavePort address generation. The CPU address in the range A0000:AFFFF (incremented by 4 every cycle for DW accesses) is translated to physical memory address 3B000:3EFFF. If host side WavePort pointers are used, the host address is latched and translated for comparison with the Codec pointers generated on chip.

Adopting this scheme would greatly simplify the extent of the design and verification work for WavePort: 8 weeks at least will be saved.

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4.6.4 On the Audio Driver

Dave proposed that the Graphics Controller has h/w to compare the WavePort pointers and generate interrupts. The Codec pointers are I/O readable by the host as well as several buffer status bits (Audio-IN buffer Full, Audio-In buffer half-full, Audio-Out buffer half-empty, Audio-Out buffer empty,...).

Nordic-1M will support Dave's proposed interrupt driven interface.
In this case the only important difference for the driver will be that it will have to generate the buffers address and not rely on the h/w to do this (Dave suggests that CPU will write and read always the same address A000:0 or B000:0 and the actual address on the host side is generated on the chip - we sugest to change this and let CPU generate the address)

Because CPU has to wait untill the a BLT operation is complete and the BLT has to wait for Audio buffer to be full or the transfer completed, two more interrupts are needed: BLT operation completed and Audio transfer completed. This way the Audio Driver and the Video driver can communicate with each other.

The Read and Write CPU side pointers will be generated by latching the last read and write WavePort CPU address (lower 16bits only) after translation to physical memory address. Comparators on the host and codec pointers will generate Buffer Full and Buffer Empty signals.

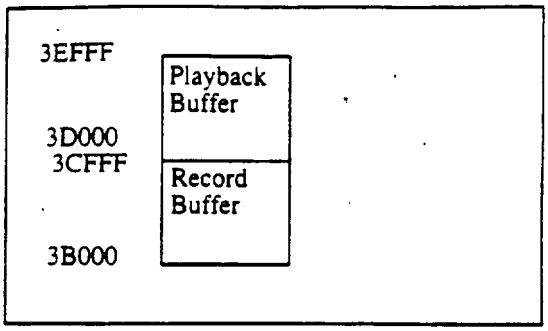
Jeff Ort drew our attention to the fact that the driver transfers a certain size block and needs an interrupt anytime half of what was placed in the Audio buffer was read by the Codec (the play-back buffer is half empty). To make things simple for the h/w, we propose to give Jeff an interrupt when the CODEC side playback buffer read pointer reached a preprogrammed value, value the driver programs everytime it transfers a block of a certain size in the playback buffer. For instance, if the driver put 2KB of data in the playback buffer starting from phisical address 3B000 (host address A000:0) and wants on interrupt when the first 1KB was read by the CODEC, it should program 3B0FF in the playback interrupt register, as 1KB = 256 32bit words. The register will have 16bits and the driver will program B0FF to get an interrupt when the CODEC reads 3B0FF or 7B0FF playback buffer address.

Similarly, on the record side, there will be a programable interrupt on the CODEC side to be used to tell the driver when the Record buffer is half full.
So we'll need two 16bit indexed registers for these programable interrupts. For each WavePort interrupt we also need a status bit to say that the interrupt happened, an enable bit to enable the particular interrupt. As Dave proposed, GR4D is the Interrupt Status register but bits [0] and [2] will be the programable interrupts status bits. The interrupts and the status bits will be cleared after this register is read (automatic clear in h/w).

We could use registers GR58:5B as high and low byte for the programable interrupt

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on Record and Play-back buffers respectively.



The write-buffer (or Audio-Out =the one in which the CPU writes) is empty one Wave-Port write cycle to memory after

WRBUF-Write-Pointer = WRBUF-Read-Pointer+1

(this condition will activate set an empty flag).

The write-buffer is full one WavePort write cycle to memory after

WRBUF-Read-Pointer = WRBUF-Write-Pointer + 1

The same equations apply to the WavePort read-buffer, only this time the read-pointer is on the host side and the write-pointer on the Codec side.

Shouldn't be a Audio-Out buffer full interrupt and a status bit for it?

Threshold detect mechanism will require to increment host pointers, but the CPU is supposed to read this pointer and generate the proper address when going above the threshold. The idea of the threshold detector is that by incrementing the Audio-In read pointer every-time the write pinter is incremented if the Audio data is under the threshold value, the delta between the pointer remains the same and the buffer does not fill in with sub-threshold value. This was true if the half-full detection had been generated based on the delta between pointers. After talking to Dave, there are some clarifications to be made on the threshold detect mechanism for record:

For one record sesion, this is a one time event mechanism: if the threshold was passed once after being enabled, its effect is lost - even if the sound level goes below the threshold the record buffer read pointer works normally. The threshold will help only in the initial stage before the first actual voice pattern is detected, but it does not have any effect after the intitial triggering event - once the sound leved passed once the threshold.

With this driver approach, GR43 and GR58:5B will not be needed.

Five registers are saved. Twenty One register are still needed (plus two reserved = 23).

Another possible approach for the driver uses extensively the Vertical Interrupt:

In this case every Vertical Interrupt, the Audio Driver reads the Codec side pointers, compares them with the Host side pointers, the driver generates based on the CPU address it last wrote to or read from and makes its own decisions. The driver will also check the BLT completed status bit.

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In other words, every 18msec (@60Hz), on the Vertical Interrupt the Audio driver can process data from the Codec pointers, calculate based on the last address if the WavePort buffer is full or empty and decide how many more WavePort accesses to execute. As at least 180msec worth of data is in a full Waveport Buffer, the driver has 6 opportunities to find out that the buffer is empty and start filling it before half WavePort buffer is empty.
On chip h/w is still needed to stop sending data to the Codec after sending all data and to read all data from the WavePort read memory buffer on the host side. Because the CPU decides when the buffers are full, half full or empty there is no need for registers for the pointers on the CPU side, but the CPU address will still be latched to generate the host side pointers.
The "BLT operation completed" and the "Audio transfer completed" interrupts are needed anyway bacuse we share the data-path for BLT and CPU cycles.

By adopting this mechanism in the driver, no special h/w is needed to preserve pointers on the Host side, to compare the Host side pointers (read and write) with the Codec pointers and to generate interrupts and status bits. The only interrupts needed are Standard VGA Vertical Interrupt as a time base, BLT completed Interrupt and Audio Completed interrupt.

We can still implement the threshold detect.

GR44,GR45, GR48 and GR49 won't be needed.
Nine registers are saved. Seventeen register are still needed (19 with two reserved registers).

Conclusion
The above proposal, if OK for the WavePort driver, would reduce significantly the amount of design and verification work on the WavePort. This document was written in order to get feedback and reach an agreement ASAP. Our goal is to have a unique s/w model for the WavePort, but we'd like to cut the amount of work if possible.

Rakesh's notes on the discussion with Jeff Ort and Dave Keene, 11/03/93

1. Since in Nordic, we do only 1R + 1P always, what happens if the bit is disabled for the host read at a time when ODD number of FIFO stages are filled? At Present we assume that while recording some SILENCE is inserted at the end of recording session and thus we can disable the bit as soon as driver disable it.
Jeff and Dave Kenne both agree that even though no SILENCE is inserted at the end, it is still valid to disable the memory transfer immediately after the bit is negated.

2. Threshold Issue.
If threshold mechanism is enabled, we keep putting the samples into the AUDIO BUFFER.
If the data in buffer is more than the programmed value (GR74 and GR75) and input data crosses the threshold value, the interrupt is generated immediately. But if data amount is less than the

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value in the registers GR74-GR75 and input data has crossed the threshold value then we wait till it crooses this value(GR74 and GR75) and then interrupt is generated.

Dave's specs talk about two pointers on the RECORD buffer, one for the CPU read and another for CODEC write. Both of these pointers are accessable by the CPU in his specs So he suggests that before the threshold is met we should fill up the buffer till half full condition. Once the buffer is half full, any more writes to RECORD buffer by the CODEC should increment both of these pointers. In this case whenever the threshold is met we are guaranteed to have some information about the history of audio samples just before the threshold is met. At the time when threshold is met the generated interrupt should tell CPU that CPU can read the data from the location pointed to by CPU read pointer.

But in NORDIC, the CPU read pointer is not accessible by CPU. Thus we keep putting the samples in the RECORD buffer and not generate the interrupt till the threshold is met even though we might pass the programmed value for the interrupt. At the time when the threshold is met, the interrupt is generated if CODEC write pointer is past programmed number. If threshold is met before the CODEC write pointer passes the programmed number, we wait till it does cross the programmed number. So the driver for Nordic should store the CPU address at the time when the threshold mechanism is enabled. So at the time of interrupt CPU can calculate the amount of samples in the BUFFER.

3. Independent control for IN / OUT mono / stereo .

Codec read and write are independently controllable for mono or stereo input / output.

4. Jeff agrees with the usage of OFFSET register GR9 to generate the CPU side adress for audio, instead of NORDIC generating the adress automatically.

Minutes of 11/20/93 Meeting with Keith, Del and Dave Keene

1. We need to check if WavePort accesses work with linear addressing (SR7 - aperture register).
2. Make sure that OverRun Status is there even if OverRun Interupt is disabled.
3. Enable looking for threshold only after you reach the given address.
4. Bit GR6E[6] should move to GR6E[3].
5. Talk about programable address for AUX1 and 2.
6. Check out arbitration for audio throughly.
7. Check overrun interrupt during threshold... always programmed interrupt after crossing threshold. ?? Rakesh may understand this!!

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4.6.5 Registers specs for the AUDIO of NORDIC1-M.

GR60 Wave Port Control 1

7. Reserved
6. Reserved
5. Enable audio for host accesses.
4. Select 4215
3. Stereo for reciever (i:e STEREO CODEC)
2. Stereo for transmitter (i:e STEREO NORDIC)

1:0 Data Format select

- 00 16 bit
- 01 8 bit
- 10 4 bit
- 11 reserved.

GR61 Waveport control 2

7. Reserved
6. powerdown control ---> 0 will force low on PDN.
5. Enable command mode. 4215 must have been placed in COMMAND mode by forcing low on D/C* pin.
4. input level in SDI in command mode.
3. output level on SDO in command mode.
2. output level on SCLK in command mode.
1. output level on FSYNC in command mode.
0. output state of D/C* pin.

GR62 Input Audio Threshold setting.

7:0 Available only for 16bit mode. Only +ve data is compared i:e if msb of left data is 1 no compare is performed.

GR65

7. Enable Threshold detect mode.

6:0 Reserved

GR66 7:0 Audio Input Codec write pointer low byte

GR67 Audio Input Codec write pointer high byte

7. Enable input from codec to audio buffer.

6:0 Audio Input Codec write pointer (low 7 bits of 15 bit pointer)

GR6A 7:0 Audio Output Codec Read pointer low byte

GR6B Audio Output Codec Read pointer high byte

7. Enable output to codec from audio buffer.

6:0 Audio Output Codec read pointer (low 7 bits of 15 bit pointer).

GR6C : Interrupt Control.

7:6 Reserved.

5. Standard VGA Interrupt disable.
   - 0 --> Allow VGA interrupt
   - 1 --> Disable VGA interrupt.

4:2 Reserved.

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1. Audio Input interrupt control -----> DURING RECORD SESSION
   0 --> disable this interrupt source.
   1 --> Enable input buffer full OR programmed full interrupts.
0. Audio Output interrupt control -----> DURING PLAY SESSION.
   0 --> disable this interrupt source.
   1 --> Enable Output buffer empty OR programmed empty interrupts

GR6D : Interrupt Status.

Indicates any active enabled interrupt. Reading this register will clear the interrupt state and reset the status. No effect on the standard VGA interrupt status or interrupt.

For All of the following 1 in the bit means PENDING INTERRUPT

7:6 Reserved.
5. Standard VGA Vsync interrupt (state of 3C2(7)).
4. Reserved.
3. Record Buffer FULL (OVERRUN).
2. Record Buffer PROGRAMMED FULL.
1. Play Buffer EMPTY. (UNDERRUN)
0. Play Buffer PROGRAMMED EMPTY.

GR6E : AUX1 and AUX2 control

7. Enable Aux Sel 1 low-true output on adress match 530-53Fh.
6. Enable Aux Sel 2 low-true output on adress match 388-397h.
5:0 Reserved.

GR6F: Code status.

7:4 Reserved
3. Timer status (ADI) time slot 6 bit 7
2. overrange (OVR) time slot 7 bit5
1. PIO1 input status. time slot 7 bit 7
0. PIO0 input status. time slot 7 bit 6

GR70: Codec control DWORD from Nordic to codec. byte D7:0
GR71: Codec control DWORD from Nordic to codec. byte D15:8
GR72: Codec control DWORD from Nordic to codec. byte D23:16
GR73: Codec control DWORD from Nordic to codec. byte D31:24

GR74:75 Interrupt value for audio IN buffer.

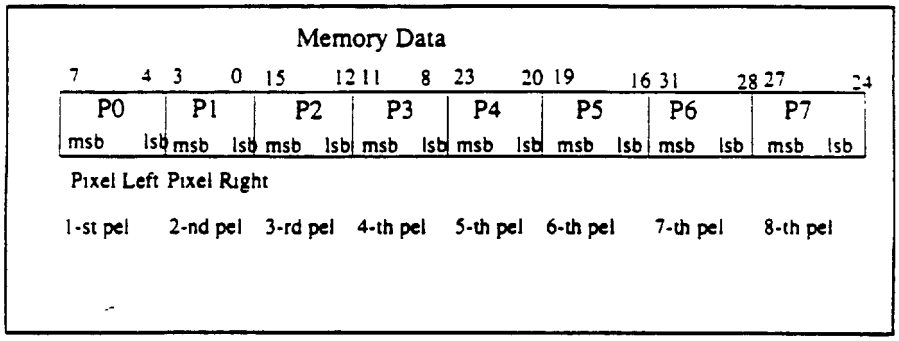
When CODEC reaches the programmed adress -1, an interrupt is generated during the record session.

GR76:77 Interrupt value for audio OUT buffer.

When CODEC read pointer reaches the programmed adress -1, an interrupt is generated during the play session.

4.7 Four Bit per Pel Packed Format

To fully support Windows Chicago, Nodric-1M should support 4bit/pel packed format. CPU will be able to write only 8bits or more at a time. To modify only 4bits the CPU will do read modify write and mask four bits (bring them from CPU latches).
The following picture shows the actual format:



In order to get Nordic-1M to support this mode, we need to place the VGA Video Data Path in 8bit per pixel mode with pixel doubling (mode 13) but disable the mechanism that concatenates adjaisant 4bits to make one 8bit pixel displayed twice (at a divided by two RAMDAC VCLK) and disable as well dividing by two the RAMDAC VCLK.

On the CPU side chain 4 address scrambling should be disabled and data should be shifted right like in extended 256 color modes.
In nordic-regs-rev9.lst we assigned SR26[0] to enable this graphics mode.

4.8 Robin's Ideas on High Resolution Panels for Nordic-1M

Nordic's objective is to be able to center and fill the screen on 800x600 panels and to center an 800x600 picture on 1024x768 panels. The main focus is 800x600 panel support TFT and dual scan STN.
In TEXT there will be three options:

- horizontal and vertical centering with 9x16 fonts (disable 640x480 force to 8dots font)
- auto-expand the font to fill the screen
- special font to fill the screen

In Graphics there will be tree options:

- horizontal and vertical centering
- use a driver to run at maximum resolution
- automatic expand to 800x600 (only if s/w verification shows it being OK).

In all cases horizontal and vertical options will be decoupled (different enable bits).

Here's a list of what needs to be done:
a. Expand horizontal and vertical centering capability from 640x480 to 1024x768.

b. Shadow all H/V CRTC registers except HDE and VDE.
The vertical registers are shadowed now, but the horizontal registers are not.
We need to shadow CR0, 2, 3, 4 and 5. These registers will be written by the BIOS at POST. The same mechanism to enable/disable vertical shadow is used to enable/disable horizontal shadow.

c. Support 10dot character-clock and CRT-FIFO-Read / Shift/Load (Video-Serializer Load). Now only 8dot and 9dot character-clocks are supported. For smooth-scrolling the pel-pan has to be expanded to 10 positions (0:9).

d. TEXT auto-expand will be as follows:
- horizontal: replicate the last pixel once for 9 dots wide fonts and twice for 8 dots wide fonts.
- vertical: replicate all odd scan-lines

TABLE 3. Font Expansion for Different Panel Sizes

Font-Size/Panel-Size	480	600	768
8x14	8x19	10x21	10x21 + center
8x8 with scan-ln. doubling	8x19	10x24	10x24 + center
9x16	8x19	10x24	10x24 + center

Please note that in text vertical expansion is done on the scan-line counter as well as the vertical display line counter, but it does not affect the vertical non-display line counter.

e. Graphics modes expansion (to be implemented only after s/w verification)
Graphics expansion is less important as it is assumed that important applications will run at maximum panel resolution with a driver.
We'll need to supply drivers for many applications with high res. panels !!
Vertical expansion:
- 350lines -> replicate all odd scan-lines
- 400lines -> replicate all odd scan-lines
- 480 lines -> replicate every 4-th line

Horizontal:
- center
- duplicate every 4-th pixel
- ~~duplicate every 4-th pixel with dragonal shift~~

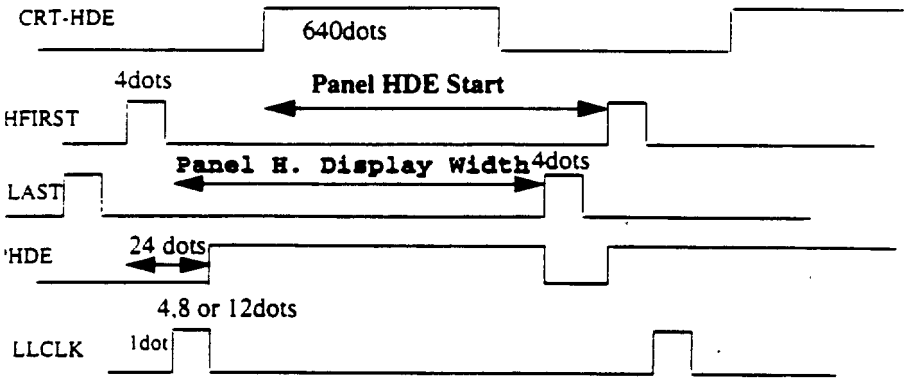
~~(scan-line 0 -> 1st pel, scan-line 1 -> 2nd pel, scan-line 2 -> 3rd pel, scan-line 3 -> 4th pel).~~

f. Please note that when character clock is expanded to 10 dots, h/w cursor also needs to be positioned at 8 or 9, so it needs one more bit of fine position.
SR2E[0] will be the msb of h/w cursor (default zero) to be used in this case.

4.8.1 Panel Horizontal Timing Control in Nordic

If in Terminator all panel timing is based on HSYNC and VSYNC programing, in Nordic it will be independent of HSYNC and VSYNC programming.

Horizontal Timing for 800x600 panel with 640x480 picture:



Registers for Panel Horizontal Timing Control

This set of four registers are used to generate horizontal panel timing with 640x480 or 800x600 panels and to center horizontally a 640dots or 720dots picture on an 800x600 panel.

CR40 No Center Panel HDE Start Register

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. This register is used to program Panel Line Clock Start and Panel Display Enable Start with both 640x400 and 800x600 panels any time no horizontal centering is needed.

CR41 Panel HDE Start Register to Center 720 dots

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register

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will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 720 dot mode (text or graphics - RIX mode only) is centered on an 800x600 panel. If horizontal expansion is on CR40 is used.

CR42 Panel HDE Start Register to Center 640 dots

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 640 dot mode (text or graphics) is centered on an 800x600 panel. If horizontal expansion is on CR40 is used.

CR43 Panel HDE Dot-Clock Skew Control Register

[7:6] Panel Line Clock Width:
- 0 = 4 dot-clocks
- 1 = 8 dot-clocks
- 2 = 12 dotclocks
- 3 = reserved

[5:4]CR42 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

[3:2]CR41 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

[1:0]CR40 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

By programming this skew, it is possible to compensate internal delays on Panel HDE for diferent types of panels. If all delays are matched the skew fields should be zero to

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align with character clock.

Automatic switching between these three registers will be done based on CRTC and Sequencer programming and the type of panel used
(640x480 or 800x600).

CR 44 Horizontal Panel Display Width Register

The value in this register is expressed in 4 dot-clocks (never divided by two).

[7:0] Panel Display Width in hex expressed in 4 dot-clock chunks. As it is used to compensate for internal delays, this value is close but not exactly 640/4 or 800/4.

4.8.2 Horizontal CRTC Registers Shadowing

In order to run VGA programs on 800x600 panels, Nordic needs to shadow the horizontal timing registers except the display enable end, which is application dependent.
(T1 has shadows only for horizontal total.)
This is because all horizontal timing registers but HDE have to be set-up for 800x600 in order to run an 800x600 panel. Symulscan with 800x600 panels runs even the CRT as an 800x600 display in all graphics modes.
In T1 as well as in Nordic, vertical panel registers are mapped at R2x, R3x,... accesible when CR2D[7] = 1. In nordic these registers remain there.
IN T1 there are two registers: **R0x and R1x** which represent HTot shadows, accessible with **CR2D[7]**. They are no longer used in Nordic, **but there is a replacement for them, independent of CR2D[7]**.

In Nordic, H Total, H Retrace Start and End, H Blank Start and End are shadowed. Each entity has two values to chose from: a value for dclk/2 and a value for dclk not divided by two. The effect selection is done automatically based on SR1[3] value, but for access there is a selection bit: CR2C[4] to control which of the two sets of registers gets read or written.

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Here is a summary of the horizontal shadow registers and its controls.
CR2C[5] write protect for horizontal shadow:

1 -> write both the shadow registers and the corresponding standard VGA registers fields (some registers are not accessed entierly but only in their timing part)
read back the shadow registers

0 -> write only the standard horiz. timing VGA registers (the shadow registers are write protected). Changing onlt the value of these registers does not have any effect over the CRTC timing.
read back the standard VGA horiz. timing registers

CR2C[4] Select the set of horizontal timing shadow registers to be used (low rez or normal). This bit is reutilsed from T1: it was low power RAMDAC mode - tie now the logic L) .
0 -> select Ry for access
1 -> select Rz for access

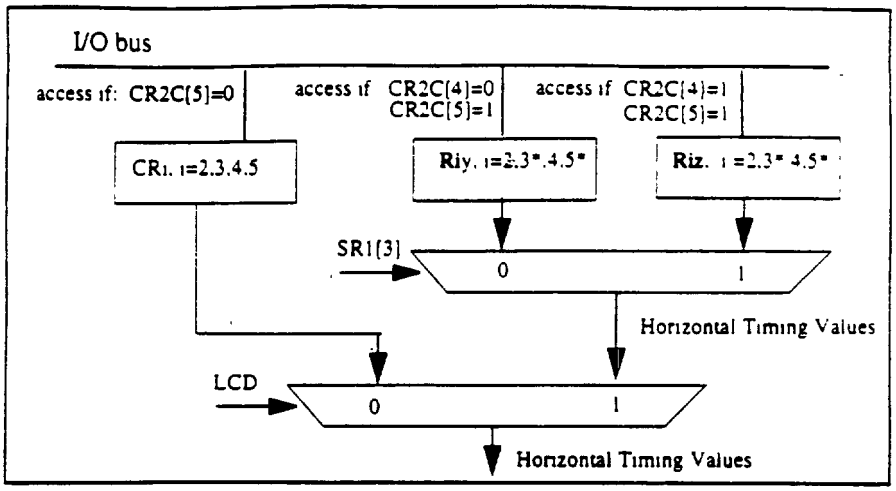
To diferentiate from the Rx registers which still exist as in T1, and are vertical panel registers, we'll call the two sets of horizontal shadows mapped in the same address space Ry and Rz (Ry = normal, Rz = dclk/2 case)
The effect of Ty and Rz is controlled by SR1[3] (dclk/2 bit).

The Horizontal Timing shadow registers are:
R0y,z R02y,z R03y,z (only lower bits) R04y,z R05y,z (only lower bits)

When CR2D[7] =1 we can access only the panel registers: R2x,... RBx. In this case we cannot access either the VGA standard registers or the horizontal timing shadow registers. **Please note that R0x and R1x are reserved in Nordic. Their function is replaced by R0y,z.**

Standard VGA CR0,2,3,4,5 horizontal timing registers (only the timing fields) do not have any effect on the CRTC: only the shadow registers have effect.

Note: Vertical Blank registers CR15 and CR16 are only write protected in T1 - not shadowed. This seems to be an error... so they should be shadowed in Nordic.
When using blank as overlay, DEn becomes blank and the shadow registers create the overlay both horizontally and vertically, but they are no longer write protected by CR2C[3] or [5]... As in 5428, they will not be write protected at all as the overlay is used only under MS Windows which is a controlled environment.



4.9 TV-Out Support in Nordic-1M

Nordic's objective is to be able output data to an analog TV Encoder chip thus supporting a cheap way of displaying on a TV. The main application is graphics, probably under windows. TV display and tape-recordig are of interest.
Nordic will run in a locked interlaced mode at 13.5MHz for NTSC and it will use the LCD panel supprt shadowing mechanism (the shadow Horizontal and Vertical CRTC registers) to prevent the application from changing the CRTC set-up. Even the dotclock frequency will be locked. Horizontal and vertical display enable will be open to the application.
Nordic will provide analog RGB, Composite SYNC, NTSC/PAL and TV-ON to the TV encoder. AD720 and MC1377 analog TV encoders that accept RGB input will be supported directly (with no glue logic).
Nordic will have edge skew h/w on the appropriate signals in order to meet the TV Standards timing requirements .
In this mode Nordic will not be able to run a panel or a CRT monitor... no simulscan supported with TV-OUT. But the same system will display on a panel, a CRT monitor or a TV with minimum glue logic.

Digital TV Encoders are not supported.

All standard VGA modes plus 640x480 8bpp can be supported, though special set-modes are required, as they all run interlaced. I suspect that we'll end up supporting only a few important modes. Should we compress text to 8dot wide fonts?

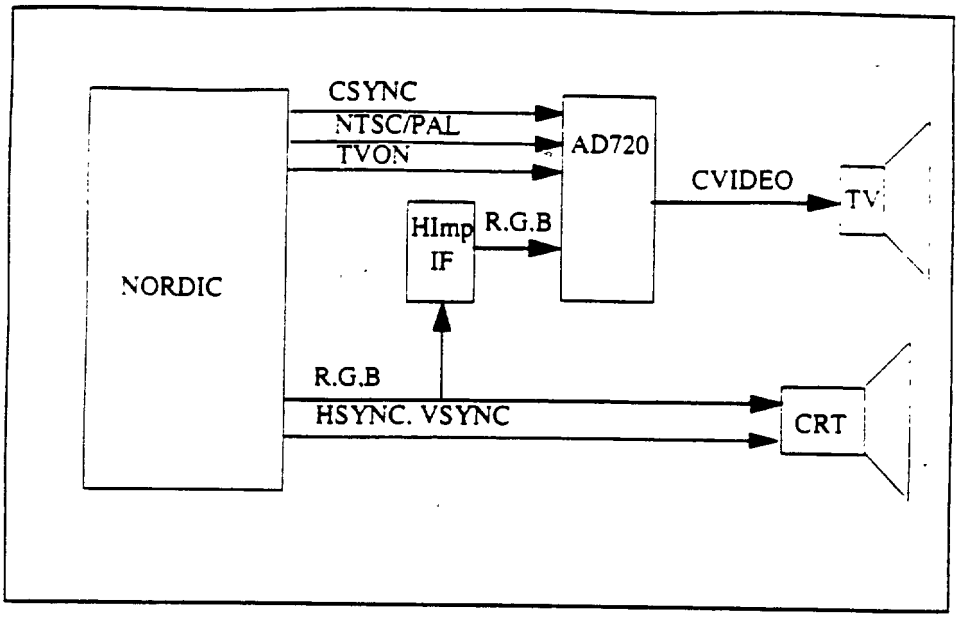


TABLE 4. Data on TV Standards

PIXCLK	Multiples of Line Frequency	Active Pixels per Line	Field Rate
12.2727MHz	780xFH	640	60Hz
14.75MHz	944xFH	768	50Hz
13.5MHz	858xFH	720	60Hz
13.5MHz	864xFH	720	50Hz

Signals to be supplied by Nordic:

- CSYNC = Composite SYNC signal
- NTSC/PAL = a programable output selecting the TV Standard NTSC (1) or PAL (0) The value of CR30[2] comes out on the pin.
- TVON = H for the TV Encoder to be ON, L for it OFF. The value of CR30[3] comes out on the pin. If CR30[3] =0, CSYNC and NTSC/PAL pins are L.

In Nordic-1M all these signals will come out to the panel pins when a certain configuration bit is enabled.

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Vertical Timing

Vertical Blank and the appropriate CRTC registers are programmed to generate Blank which in TV case is the actual Display Enable.

For NTSC program 9 lines of VBlank.

For PAL program 7 lines of VBlank. In h/w Nordic will generate 7.5 lines of VBlank in this case by delaying the trailing edge by 0.5 line

Vertical Sync Registers will be programmed for Field Sync generation.

For NTSC program 3 lines.

For PAL program 3 lines and get 2.5 lines by delaying the leading edge by half line.

Horizontal Timing

Two basic pulses are generated:

- HREF1 = Horizontal Reference 1 which is HSYNC start with 64 dotclocks width CR30[1:0] controls the fine skew of this edge by increments of two dot-clocks.
- HREF2 = Horizontal Reference 2 which is a pulse marking the middle of the line between two HSYNC start edges. CR19[7:0] are used to program the start of this pulse.

CR30[1:0] controls the fine skew of this edge by increments of one dot-clock.

Note that HREF1 and HREF2 skews are in sync: HREF2 skew is half HREF1 skew. Horizontal Total is 858 dot-clocks at 13.5MHz for NTSC and 864 dot-clocks at 13.5MHz for PAL.

Composite SYNC Logic Equation is:

CSYNC = [(HREF1 + HREF2) & VS] trigg368dclk-pls + -> Field Sync (serration)
[(HREF1 + HREF2) & VS*&VB] trigg32dclk-pls + -> Equalization
[HREF1 & VB*] trigg64dclk-pls -> standard sync during display time

Where: VS is Vertical Sync programmed time
VB is Vertical Blank programmed time
* is a logic negation
trig32dclk-pls means: on the rising edge of this signal generate a 32 dot-clocks wide pulse.

There are four ways to connect the video encoders and the CRT. We are now in the process of deciding which one is the best:

1. The simplest way to connect the TV decoder is to assume that the CRT Monitor should not be hooked to the notebook computer at the time the TV is. In this case we can put a high resistance voltage divider (2KOhm) to get the required 0.7V or 1.0V full swing to the decoder. The 2KOhm voltage divider will not practically affect the 50 Ohm resistance on the CRT, when the CRT is hooked on. The disadvantage of this method is that it requires a CRT to be disconnected from the note-book computer when connecting a TV. The TV encoders get RGB input through an AC connection (a capacitor) so the DC source may be a high resistance.

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The advantage is that it is simple and low cost.

2. There are no buffers or other resistors than usual. We control the RSET resistor value on the LM334 current source depending on the presence of the CRT Monitor hook-up or not. If the CRT Monitor is not hooked-up, we adjust IRef so that DAC-s full swing output voltage is 0.7V (or 1.0V) with a 150 Ohm load. If the CRT Monitor is detected to be hooked up, RSet will be left as it is now. The adjustment is done automatically with a transistor. This approach requires a programmable output (from Nordic or Core Logic) to control RSet value. The detection of the CRT Monitor presence is done by s/w the standard VGA way.

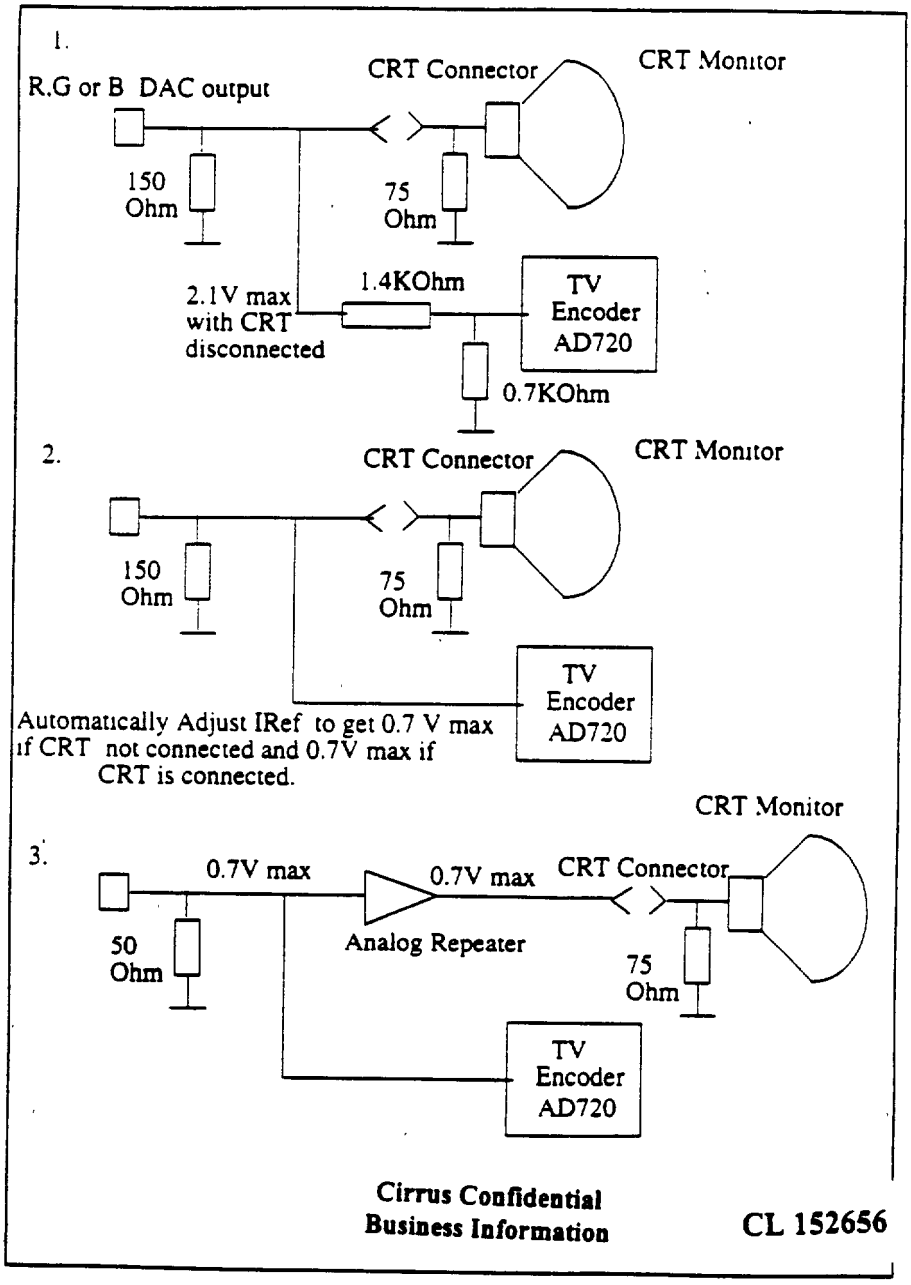
3. Put 50 Ohm load on the DAC output and feed it to the TV encoder and to an Analog Voltage Repeater that drives the CRT Monitor RGB lines. This way DAC output is always 0.7V full swing independent if the CRT Monitor is hooked to the notebook or not.
This approach works for AD720 but not for MC1377 which requires 1V full swing.
With this approach the presence of the CRT monitor cannot be detected VGA style (incompatibility issue ?).

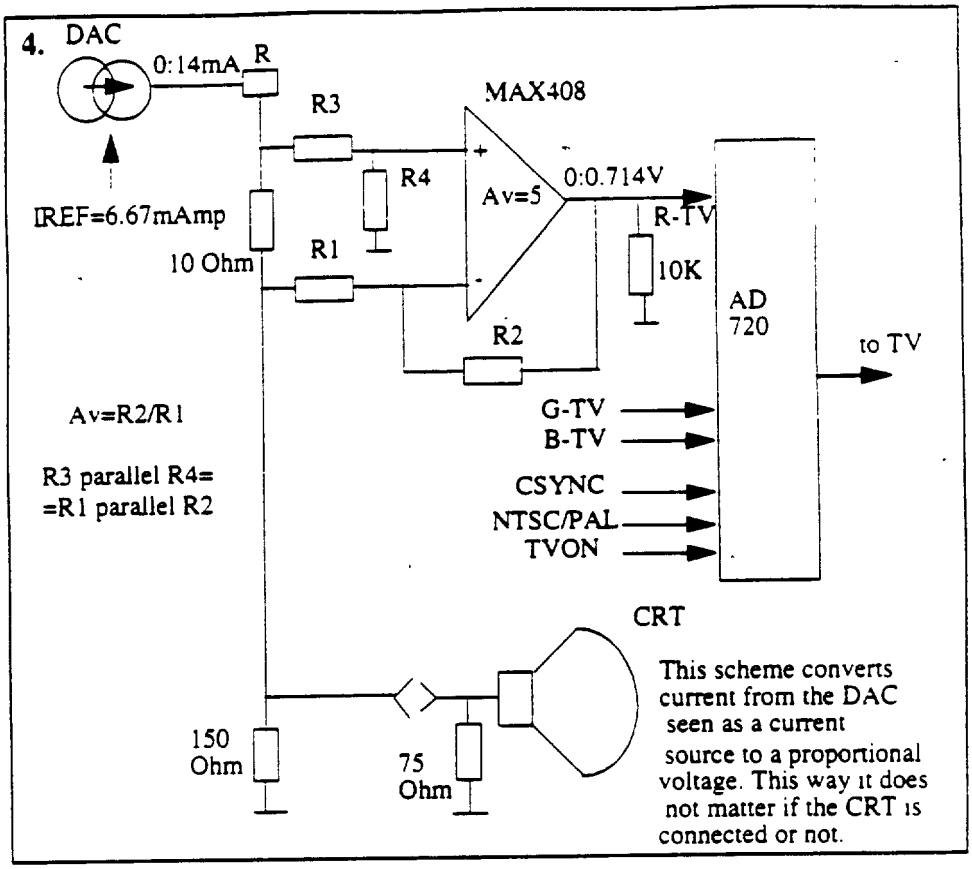
4. Leave the CRT path unchanged, except for a low resistor shunt added in series.Convert the constant current delivered by the DAC into voltage that is amplified to NTSC/PAL level depending on the type of encoder used. Requires fast operational amplifiers on each gun, but allows operation with or without CRT connected and color compare.
This looks to be the best scheme but it is also the most expensive. The op-amp can be used also as a filter to limit the spectrum and avoid cross talk in color modulators.

Note: According to Fong-Jim Nordic DAC has some oprtational limitations: at 5V DACVDD, if the load is 150 Ohm and the DAC input is all ones (FFH) the output will be indeed 2.1V as expected.
If the load decreases (to more than 150 Ohm) , the output voltage will be increasing up to 2.7 V. At that point it will stop increasing: the DAC will be out of its operational range
This is OK for what we are trying to do with TV-OUT.
At 3.3V though, according to Fong-Jim the DAC output will follow the load only up to about 1.1V. This would require a 50 Ohm load at all times. With a 50 Ohm load the maximum DAC voltage at both 5 and 3.3V is 0.7V, within the operation range.
The question is: how to add a 75 Ohm load when there is no CRT in there?

I see two simple solutions: either use TV-OUT at 5V DACVDD (switch CVDD and DACVDD to 5V for TV-OUT) or make an external connector similar to a CRT connector that one plugs into the back of the notebook when the CRT is not in use. This connector should have 75 Ohm resistors to GND on RGB lines.
There may be other solutions too... everyone is invited think.

Three possible ways to connect an Analog PAL/NTSC TV Encoder to DAC output.




4. DAC
0:14mA
R
R3
MAX408
R4
Av=5
0:0.714V
R-TV
IREF=6.67mAmp
10 Ohm
R1
10K
AD
720
R2
to TV
Av=R2/R1
G-TV
B-TV
R3 parallel R4=
=R1 parallel R2
CSYNC
NTSC/PAL
TVON
CRT
This scheme converts current from the DAC seen as a current source to a proportional voltage. This way it does not matter if the CRT is connected or not.
150
Ohm
75
Ohm

4.10 H/W ICON Support for Nordic-1M

Nordic-1M will support a h/w icon with the following features:
- Up to 4 64x64 Icons displayed at the same time as a vertical bar.
- All Icons move together and they are inedex by 64 scan lines.
  The Icon start reference point is top left corner.
- Horizontal Resolution is one pixel programed coarse as character clocks and fine as pixels exactly as a h/w cursor.
- Vertical Resolution is one scan-line.
- Each Icon has inependent display control for
  - icon number i enable for display (i=0:3)
  - display mode: 3colors + transpency or 4 colors
  - blink enable at text cursor rate (or half of it)
  - horizontal pixel doubling (extendes towards right)
  - vertical scal line doubling (extends down)
  - mamory map selection: two maps available per icon
- H/W Cursor goes on top of H/W Icon
- Icon memory model is and phisical address space are very similar to h/w cursor.
  Actually the icon resides in memory in h/w cursor area: Nordic supports half the number of h/w cursor maps 5428 does and uses the remaining space for icon maps. Eight 64x64 icon maps are supported: two for each icon we can display. Icon memory map assignment is fix.

H/W Icon S/W Model

Icon position will change at set mode if it is not compensated. BIOS should service the icon so that it keeps the position stable in all graphics modes: read current position and translate in the same position in the new graphics mode. The BIOS should have a call to set-up the h/w icon position and another call to control which icon is displayed and how

What we need:

a. Horizontal Start Position in character clocks and pixels
  Will be programmed exactly as h/w cursor at SR10,30,50,70,90,B0,D0,F0.
  (or SR "odd" "zero"). The upper 3 bits of index define the fine (vclk) position.
  SR2A[6] is the fine postion msb to be used with 9 and 10dots fonts.See 542X Reference Manual page 9-13, SR10 description.

Note: 1. If character clock or vclk change (8/9/10 dot cclk or vclk/2) the horizontal position should be adjusted.

2. As with h/w cursor the horizontal and vertical position of the icon are synchronized: s/w writes the horizontal position first, but the new position effect takes place only after vertical position was updated.

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b Vertical Start Position in scan lines.
  Will be programmed exactly as h/w cursor at SR11,31,51,71,91,B1,D1,F1.
  (or SR "odd" "one"). The upper three bits of index define the low order three bits

of position in scan lines. See 542X Reference Manual page 9-14, SR10 description.
How will Nordic know to program icon or cursor?
One bit will tell if icon is programmed instead of cursor As the icon position is programmed seldom, this mechanism does not affect performance while saving address decode h/w.

c. Enabling icon position modification by CPU is done in the same register h/w cursor is enabled: SR12.

SR12[3] Enable CPU access for Icon Position Modification
(default:0 = disable = use the same I/O address for cursor position modification).
This bit affects both horizontal and vertical position.

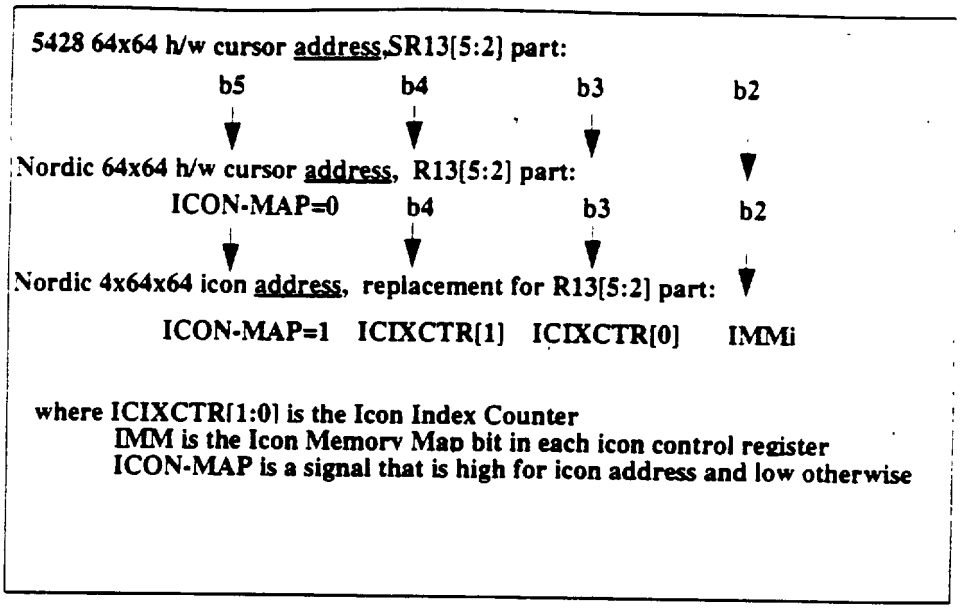
d. Icon and h/w cursor memory map selection:
5428 uses SR13[5:0] for 32x32 h/w cursor memory map selection (64 maps) and SR13[5:2] for 64x64 h/w cursor memory map selection (16 maps).

In Nordic, SR13[4:0] still select h/w cursor memory map, but the memory address bit which in 5428 is controlled by SR13[5] is no longer controlled by SR13[5]. It is controlled by an internal signal whose value is always 0 when a h/w cursor is addressed and 1 when icon is addressed. So in Nordic SR13[5] is no longer used to select a h/w cursor map. Only half of the 5428 h/w cursor memory is available for Nordic h/w cursor memory map. In Nordic there are 32 32x32 and 8 64x64 h/w cursor memory maps available.

The icon address is generated exactly as the h/w cursor address, but the source of the address map selection is no longer SR13[5:0] (it cannot be as SR13 is used for h/w cursor). SR13[5] is also noy used. To generate icon mamory map select, a two bit counter counts the first, second, third and fourth set of 64 scan lines on the Vertical Total Line Counter (the one not affected by vertical expansion). This two bit counter output, called the Icon Index Counter (ICIXCTR) will replace SR13[4:3] in Icon Memory Map Address generation.
A signal called ICON-MAP will be generated during Icon addressing. This signal is 1 if an icon data is to be fetched from memory and 0 otherwise (including when h/w cursor data is to be fetched from memory).
ICON-MAP signal will replace SR13[5] in both h/w cursor and icon memory map selection address.
One register bit in each icon control field will select the first or second memory map for each icon to be retrived from memory. This bit called Icon Memory Map (IMM) will

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replace SR13[2] in icon memory map generation.



e. Icons Control Registers

Each Icon has a field of bits attached to it

0.- icon i enable for display (i=0:3)
1.- display mode: 3colors + transpency or 4 colors
2.- blink enable at text cursor rate (or half of it)
3.- horizontal pixel doubling (extendes towards right)
4.- vertical scal line doubling (extends down)
5.- mamory map selection: two maps available per icon

Six bits per icon, all defaulting to zero. The icon enable bits select which icon is displayed
Start at SR2A register.
Use **SR2A,2B,2C,2D[5:0]** for Icon 0,1,2,3 control.
If an icon is not enabled, do not generate the memory cycles for its data... if it is not difficult to do, and do not display that icon.

f. SR2A[7] is Icon Test bit. Normally it is zero, only in test mode it will be 1.

g. The colors for the Icon are in the 16 location RAM extension at location 258.
See SR12 description in 5428 Technical Reference Manual.
Locations 256 and 257 are accessible with pixel address 0 and F for h/w cursor access.
Locations 259, 260, 261 and 262 are accessible with pixel address 3,4,5,6 as icon colors 0,1,2 and 3.
When three colors plus transparent attribute is used, the pixel addresses will be 4,5,6, for colors 1,2,3 (so pixel address 3 and color 0 of the 16 location special RAM are not used).

h. **SR2A[6]** is the most significant bit of fine horizontal position for the h/w icon:

SR2A[6] SRX[7] SRX[6] SRX[5] --> bit3 bit2 bit1 bit0

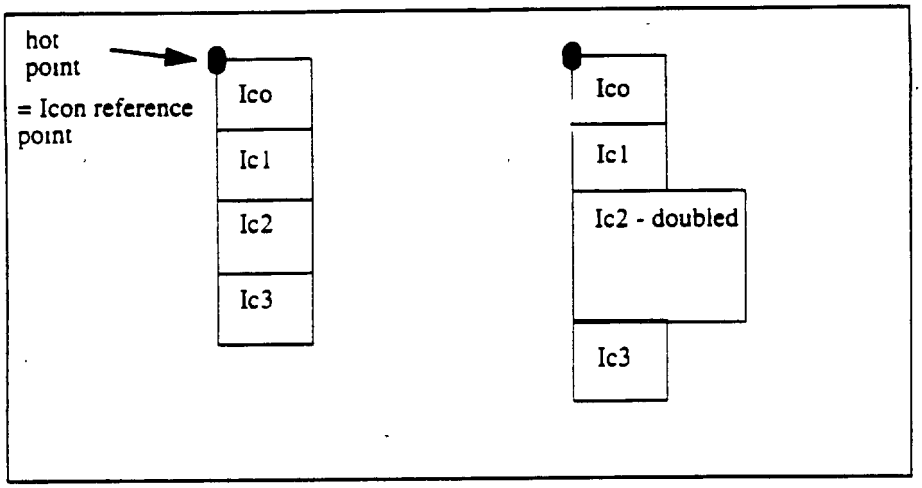
Please note that SR2A[6] will be used only in 9 or 10 dots text when the fine position is 8 or 9.

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1. Please note that when character clock is expanded to 10 dots, h/w cursor also needs to be positioned at 8 or 9, so it needs one more bit of fine position.
SR2E[0] will be the msb of h/w cursor (default zero) to be used in this case.

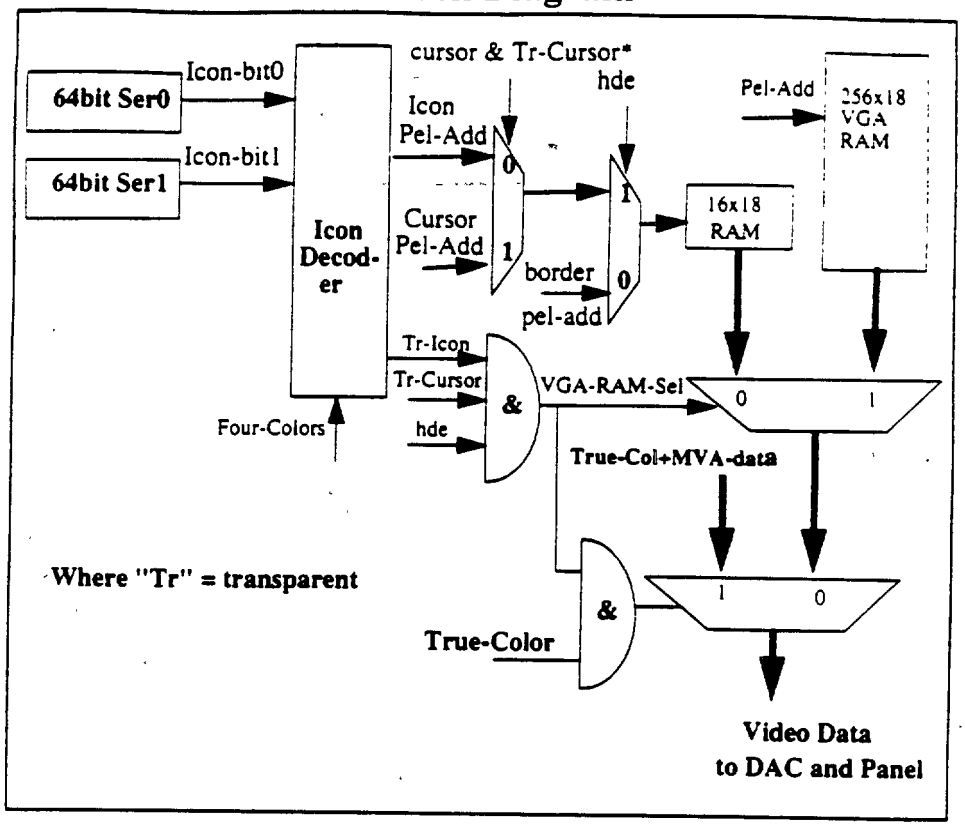
H/W Activity for Icon

1 Horizontal and Vertical Window
2. Address Generation including the independent scan-line counter for Icon
3. Memory cycle generation (at the end of line, after h/w cursor if icon and cursor are on the same line)
4. Icon Latch, Serializer and Data Path including icon blink
5. Horizontal and Vertical Doubling



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Icon Data Path Block Diagram



4.11 Dithering in Nordic

Due to new pixel depth modes and for increased flexibility the dither block in Nordic is diferemt than T1.
In Nordic the dithering is subtractive, (not additive like in T1). This moves the dither error (= double shade) to black where it is less obvious than it was before (when it was white).

CR4C - Input Resolution Override Register for Dithering

Bit	Definition
[7]	Enable Input Resolution Override (default disable) Normally the graphics mode resolution is decoded and fed to the dither block. For all graphics modes that go through the RAMDAC RAM - 6bits/gun is automatically the input resolution. For 5:5:5 RGB or 5:6:5 RGB or 8:8:8 RGB we use

a diferent input resolution: 5 for 5:5:5 and 5:6.5 and 8 for 8:8:8 RGB.
In all cases the proper input resolution is automatically selected
If there is a need to overide this value, than we willl use this bit to enable the override and write the new value in bits 3:0. For 8 bit per gun we write 8 (1000). for 6 bits per gun -> 6 (0110) and for 5 bits per gun -> 5 (0101).

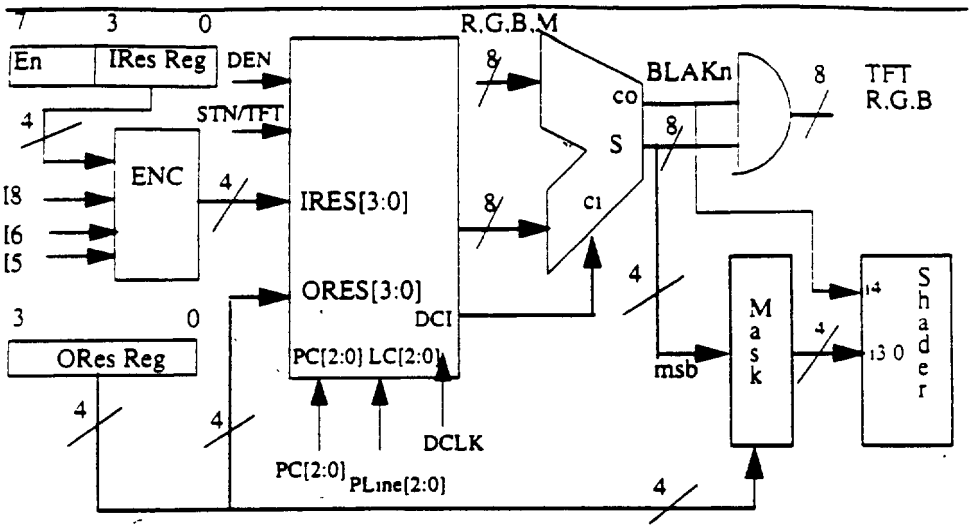
[6:4] Reserved

[3:0] The binary value of the override input resolution.
1000 -> 8bit/gun
0110 -> 6bit/gun
0101 -> 5bit/gun

CR4D - Output Resolution Register for Dithering

Bit	Definition
[7:4]	Reserved
[3:0]	The binary value of the output resolution for dithering 1000 -> 8bit/gun (TFT) 0110 -> 6bit/gun (TFT) 0100 -> 4bit/gun (TFT or 16 shades STN) 0011 -> 3bit/gun (TFT or 8 shades STN) 0010 -> 2bit/gun (4 shades STN) 0001 -> 1bit/gun (2 shades STN)

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TFT: 8,6,4,3 bits/gun

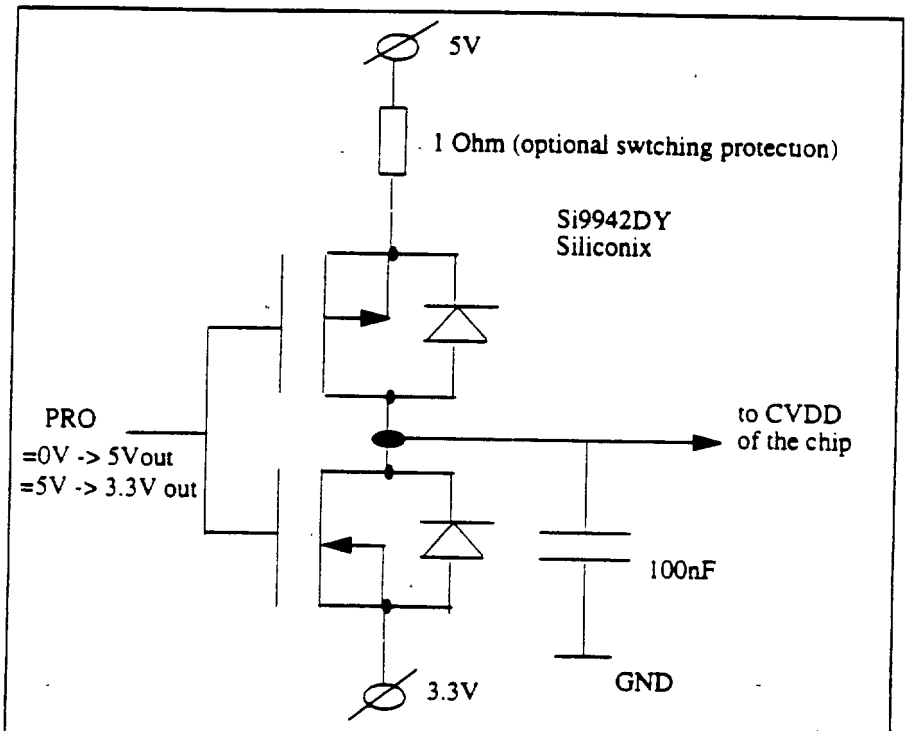
STN: 4,3,2,1 bits/shade (16+1,8+1,4+1,2+1 shades, +1 = force black)

Nordic Dithering

4.12 Core-VDD Control

Because Nordic can run higher frequency memory-clock at higher Core VDD (5V) but it offers maximum power savings at low Core VDD (3.3V), we look for a mechanism to dinamically switch at set-mode or when going into suspend from 5V to 3.3V and vice-versa.

This would allow for instance to run 24bpp 640x480 mode at 5V CVDD while switching back to 3.3V when going into suspend mode or when switching to a 4 or 8bpp mode All Nordic needs to do in this case is supply a programable output to be used to switch an external circuit.



SEL3.3VI = Suspend + Reg-Bit
Use PAL/NTSC pin and CR30[2] as power control pin,when TV-OUT capability is not ever used in the system.
Use PRO pin and CR30[7] as power control pin, when TV-OUT is used.

The value written in CR30[2] always reflects on the NTSC/PAL pin which thus can be usd as a generic programable output.

In a system without TV-OUT capability, NTSC/PAL bit and its output pin can be used to

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control when CVDD is 5V or 3.3V .This way, in most modes the chip may be optimesed for power running at a lower mclk frequency, while in certain modes it will be optimised for performance, running at 5V CVDD and a high frequency mclk (higher than what can be run at 3.3V). Because NTSC/PAL pin is tied to CRTVDD which is 5V in most systems, this bit is the first choice for the CVDD switching function.

5.0 Nordic-1M Pinout Specification 208 pin package:

System Interface (reference is VESA VL bus): 74

(on BVDD)

DAT31:0
HIMEM0/ADR[24] (normally used as ADR[24], but it can be used as any upper address or any logic combination of upper addresses. The valid value of this pin for Nordic address space is programable in VESA VL and PCI bus.
HIMEM1/ADR[25] (normally used as ADR[25], but it can be used as ADR31 and leave 2GB of upper address space reserved for MPEG/JPEG boards). The valid value of this pin for Nordic address space is programable in VESA VL and PCI bus.
With these two pins, Nordic can directly decode up to 64MB of CPU address space in VESA VL bus.
ADR[23:2]
BE3n,BE2n,BE1n,BE0n
LADSn,LDEVn,RDYn
M/IOn, W/Rn
RESETn, LCLK
RDYRTNn,
EBROMn/SLEEPIn (Enable BIOS ROM Buffers on all busses or when not in ISA or SLEEP Input active L. If this pin is L, the chip goes in sleep mode as if 3c3[0] is 0 or 46E8[3] is 0. The ISAPU read-back register bit configures the pin for EBROMn. If not in ISA bus, this pin is configured as SLEEPIn and it should be tied H if not used.
INTR, CLK32K, OSC/XVCLK (14.318MHz or External VCLK)
SUSPI/BLI, SBYI/ACTI/FCEVIDEOn
(32KHz clock input,
Supend Input/ Back-Light Input
Stand-by Input/Activity Input/VAFC External Video Control Input - controlls the direction of FCP[7:0]. Pin configuration controlled by VAFCPU. Most systems will
use only one direction for VIDEO, probably video in, so the fact the FCEVIDEO is on BVDD should not require voltage translation).

Configurations: - VL/PCI/ISA bus, support/not BIOS, 8/16bit BIOS.
- Need a register bit to select SUSPEND Input or Back-Light Input Default is SUSPEND Input.
- Need a register bit to select Stand-By Input or Activity Input. Default is Stand-By Input.
- SUSPIn, BLIn, SBYIn, ACTIn are level triggered, active L inputs. In Nordic there is no Suspend pin polarity bit as in T1 (SR8[4])

Note: a.In PCI bus, Alpine used ADR17:2 as BIOSA15:0. We assume that all portable systems will use a motherboard video BIOS and do not support an adapter BIOS in PCI. We do support an adapter BIOS in VESA VL bus and ISA to facilitate demo board design.

b. EBROMn is active on all bus types: in ISA is generated on Address Decode and MEMRn, while in VL and PCI is unlatched address decode. In PCI bus the BIOS should be relocatable, an option we do not support. That is why we say that we do not support BIOS in PCI. We do support IOCHRDYn and RDYn/TRDYn for BIOS accesses too. All this logic should already be in 5428 (ISA and VL) and Alpine (PCI).

c. The 5428 Feature Connector pins are available in all buses. A register bit enables them early in the logic to save power when not in use.

d. In ISA RESETn has to be inverted outside the chip.

System/Bus Interface Signal Mapping

(See 54xx Reference Manual for Feature Connector Pins Description: FCyyyy)

TABLE 5. VESA-VL <-> PCI bus <-> ISA bus Pin Mapping

VESA-VL	Intel-PCI	ISA
HIMEM	--	--
ADR23:16	--	LA23:16
ADR15:9	--	SA15:9
ADR8	PAR	SA8
ADR7	STOPn	SA7
ADR6:2	--	SA6:2
BE3n	C/BEn3	SA1
BE2n	C/BEn2	SA0
BE1n	C/BEn1	SBHEn
BE0n	C/BEn0	RFRSHn
DAT31:22	AD31:22	--
DAT21:19	AD21:19	--
DAT18	AD18	MWRn
DAT17	AD17	IOCS16n
DAT16	AD16	IRQ
DAT15:0	AD15:0	SD15:0

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TABLE 5. VESA-VL <-> PCI bus <-> ISA bus Pin Mapping

VESA-VL	Intel-PCI	ISA
RESET	RESET	RESETDRV ??
LADSn	FRAMEn	BALE
LDEVn	DEVSELn	MCS16n
RDYRTNn	IRDYn	AEN
W/Rn	IDSELn	IORn
M/IOn	--	MRDn
LCLK	CLK	IOWn
RDYn	TRDYn	IOCHRDY
EBROMn/VADRn	VADRn	EROMn/VADRn
INTR	INTR	ZEROn

Notes: 1. SW2, SW0/MCLK/XMCLK and SW1 pins are normally used by the BIOS as panel type switches readable on SR24[2:0].

2. XMCLK and XVCLK (on OSC/XVCLK) are needed for manufacturing test of the chip. When they are used, SR24[1:0] will wiggle at clock rate and they should be masked on the tester.

3. MCLK and VCLK are needed for manufacturing test of the clock synthesizer and for chip debug.

DRAM Interface (for assymetric, dual WEn 256Kx16 DRAM-s): 50
(on DVDD)

MA9:0
MD31:0
RAS0n,RAS1n,CASn/WEn, OEn
WE0n/CAS0n,WE1n/CAS1n,WE2n/CAS2n,WE3n/CAS3n

Configurations: symetric/assymetric DRAM, dual WEn/CASn

Note: a) For dual CASn DRAMs, the WE0n:WE3n pins become CAS0n:CAS3n, while CASn becomes WEn.
b) Two RAS-es are used for two banks.
c) OEn is not actually needed as we use early write.

Clock Synthesizers: 6
(MAVDD, MAVSS feed mclk clock synthesizer, VAVDD, VAVSS feed dclk clock synthesizer)

MAVSS. VAVSS. MAVDD. VAVDD.
MFILTER. VFILTER
(Can we design a clock synthesizer without an external filter?)

CRT & TV-OUT Interface and RAMDAC related pins: 13
(DAVDD. DAVSS feed all RAMDAC custom layout)

R.G.B (analog)
IRef. DCVDD1. DCVDD2. DCVSS1. DCVSS2

On CRTVDD:
HSYNC , VSYNC TO (these two pins are on CRTVDD)
CSYNC O (Composit Sync to be used with any analog TV Encoders like AD720.
CSYNC is activated by SR25[4]=1, otherwise is forced 0.)

NTSC/PAL O
(A programable output that can be used to control a TV Encoder input that selects the TV standard. This pin is a generic programable output. Its value is not affected by SR25[4].)

On FPVDD:
TVON/RES O (Generic Programable Output controlled by CR30[3] .
It can be used to control AD720 TV Encoder Power Control Pin.)
TVON is on FPVDD (not on CRTVDD like the other TV-OUT pins)
This pin is also reserved for future use (DRAM-s).

Note: If TV-OUT feature is disabled CSYNC, NTSC/PAL and TVON are forced L (to avoid powering up the TV Encoder in case it is powered off when not in use).

FLAT PANEL and Power Management Interface (on FPVDD): 31

R7/SUD3. R6/SUD2, R5/SUD1. R4/SUD0. R3/SUD7. R2/SUD6. R1/FCP[3]. R0/FCP[2],

G7/SLD7/sud3/UD3/TD7, G6/SLD6/sud2/UD2/TD6, G5/SLD5/sud1/UD1/TD5, G4/SLD4/sud0/UD0/TD4, G3/SUD5, G2/SUD4, G1/SUSPSTn/FCP[1], G0/SBYSTn/FCP[0]

B7/SLD3/sld3/LD3/TD3. B6/SLD2/sld2/LD2/TD2. B5/SLD1/sld1/LD1/TD1. B4/SLD0/sld0/LD0/TD0. B3/MOD. B2. B1/OVRW. B0/FCVLK

(use slow edge pads and stagger them modulo 4)

FPVDCLK, LLCLK, LFS, FPDE, (use slow edge output pads)
FPVCC, FPBL, FPVEE

Notes:

b. R1:0, G71:0, B1:0 (24 bit TFT panel extra video data out pins)
c. We need also bits for SUSPST and STANDBYST, PANEL-ON/OFF, PANEL-IN-POWER-UP-or-DOWN. Dwarka, do we have this now ?
d. We assume that only STN panels need external MOD.
e. No NPD pin.
f. FCP[3:0] pins are I/O-s whose direction is controlled by FCEVIDEOn in VAFC configuration. FCVCLK is the clock that clocks them in and which should be used to clock them while they are displayed or at least to resynchronize them before being latched on the internal clock. FCVCLK is always an input when in VAFC configuration.

Nordic TFT Panel Data Pin Name versus the actual TFT Panel Data Signal for diferent types of TFT Panels

Nordic Pin Name-> /Panel Type	RGB7	RGB6	RGB5	RGB4	RGB3	RGB2	RGB1	RGB0
8bit/gun	RGB7	RGB6	RGB5	RGB3	RGB2	RGB1	RGB0	RGB0
6bit/gun	RGB5	RGB4	RGB3	RGB2	RGB1	RGB0	N.U.	N.U.
4bit/gun	RGB3	RGB2	RGB1	RGB0	N.U.	N.U.	N.U.	N.U.
3bit/gun	RGB2	RGB1	RGB0	N.U.	N.U.	N.U.	N.U.	N.U.

Where N.U. = Not Used for Panel Data with this type of panel.

~~Audio Port (on ADVDD): 6~~ **Removed on 12/24/93**

~~SDO (SErial Data Output to CODEC pin SDIN)~~
~~SDI (Serial Data input from Codec pin SDOUT)~~
~~FSYNC (Frame Sync Output)~~
~~SDCLK (Serial Data Clock I/O)~~
~~D/Cn/AUXS1 (Data/Control Select Output or CS4231S Chip Select for the ISA bus)~~
~~PDN (Power Down Output)~~
~~Note: These pins can be used as extensions for 24 bit TFT panels, in which case the chip does not support the audio port. Note also that CS4215 has Reset# pin.~~

Miscellaneous Pins: 12

Following pins on MVDD:

SW2/RES4CS I (Switch #2 or reserved for SDRAM support in the future)
SW1/RES4CKE I (Switch #1 or reserved for SDRAM support in the future)

SW0/MCLK/XMCLK I/O with PD controlled by XReset
(Switch #1 or mclk driver buffered output for tesing and debug or external mclk for testing; a special register bit disables this output in normal operation for power savings.
Default: Input on which either SW2 or XMCLK comes in.
Only if the special register bit is set, this input becomes output and outputs MCLK from the clock synthesizer for testing.
The special register bit defaults 0 = the pin is configured as Input. Please note that a h/w configuration PU/PD controlls if the actual internal mclk comes from an internal or external source, but this PU/PD does not control if SW2/MCLK/XMCLK is an input or an output.)

RES4PMS Free Pin with no buffer on it.

Following Pins on PVDD:

TRWn I (Test Latch Load Enable, active L - for pinscan & test mode)
VCLK/FCDCLK I/O (Switch #0 Input or vclk driver buffered output for testing and debug, or VAFC Dot-Clock Out ; Default for this pin is Input on which SW#0 is applied. VCLK and FCDCLK is the same signal, the name is diferent to ease reference to VAFC spec)
FCP[7:4] I/O Feature Connector Data Pins bits 7 to 4. The other Feature Connector pins are shared with some panel or host bus pins.
FCESYNCn/RES4SDCLK I 5428 Feature Connector ESYNCn pin - controlls the direction of FCBLANKn and its effect and tri-states HSYNC and VSYNC.
FCBLANKn I/O Feature Connector active low bidirectional Blank signal. Its direction is controlled by FCESYNCn.

Digital, Mixed Voltage Power Pins: 22

BVDD1, BVDD2, FPVDD1, FPVDD2, MVDD1, MVDD2, CRTVDD,
CVDD1:4,
VSS1:11

Total Pins Used: 208 (with two Reserved pins and three other pins that could be freed.).

Pinout Modifications in rev. 3.8 relative to rev. 3.7 09/11/93

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1. Took-out Whisper Support Pins: WWRn, WRdn, WAD[3:0], FPCn.

2. Reduced the number of CPU Address Pins: ADR[24:27] went-away Use HIMEM to place the chip outside 16MB of memory for linear addresing.

3. Killed CRTVDD and placed CRT Interface on Host Bus VDD.

4. Introduced VAFC pins in a unique pinout configuration in both VESA VL and PCI.
Added VAFCPU a pull-up to enable VAFC (VESA Advanced Feature Connector)
ADR[27:24] VAFC pins, and R[7:4], G[7:6], EROMn/VADRn, SUSPI/BLI, SBYI/ACTI get a configuration for VAFC -> total 14 pins.
SW0/VCLK will be used as VAFC VCLK, losing SW0 pin as panel type when VAFCPU is used.
In PCI bus, no ADR pin will be shared with VAFC.
ASW0PU (Alternate Switch 0) will be added on MD pins to replace SW0 pin when VAFC is enabled by VAFCPU. ASW0PU will read-back in the same register bit as SW0, so the BIOS will not feel any modification in the reporting scheme. The chip will draw more power in suspend with VAFC.

5. Moved SW2, SW1/MCLK/XMCLK the two reserved pins (one obtained by killing CRTVDD)and TRWn on MVDD to prepare for SDRAM pin compatible option in the next Nordic that supports SDRAMs. Marked them as "reserved for SDRAM pin name". It looks that TRWn will not be needed, but it was moved on MVDD so that in case it is needed, it is available (in this case we'll need an extra switch for SDRAM support or at least to disable TRWn test mode effect).

6. Rearanged VAFC pins as pins R4 and R5 were used by VAFC - an error.

Pinout Modifications done on 01/06/94 rev. 3.0

1 Update Panel Data Pins based on Robin's Table.
2 Move MOD pin on a Panel Data Pin used in 18bit TFT.
3. Move OVRW on a 24bit Panel Data Pin.
4. Removed pin configuration for TV-OUT support with digital encoders. All pins marked TV... were removed. As a result, some pins like LLCLK, LFS, FPDE, FPVDCLK have one function now
5. Removed WavePort pins, including AUDVDD: total 7 pins freed.
AUX2 and TVG muxed on EBROMn are no longer needed either.
6. Added one more CPU address pin: instead of HIMEM. Nordic has now HIMEM0 and HIMEM1, corresponding to CPU Address 24 and 25 or any other external decode of the high order CPU address bits. In the proccess of adding this pin, most CPU Interface pins on the right side were moved to the right by one pin.
7 Added CRTVDD supplying HSYNC, VSYNC, CSYNC, NTSC/PAL CRT and TV Interfaces output buffers.
8. EBROMn is shared with TVON, the power-on signal for AD720. So, in ISA bus with on chip BIOS support, AD720 power on cannot be directly controlled by Nordic.
9 Added pins for Analog TV Encoder support - AD720 and MC1377 :
a. CSYNC = Composit Sync signal
b. NTSC/PAL = 0 -> NTSC, 1-> PAL

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c. EBROMn/TVON (see #8)

10. ASW0PU "Alternate Switch 0 Pull-Up" pull-up on pin 155 MD[26] was removed, as SW0 is now not multiplexed.
11. Demultiplexed some of the pins previously multiplexed:
    a. Pin 168 TWRn/RES4PMS is now RES4PMS, a pin reserved for synchronous DRAM support.
    b. SUSPI/BLI/FCBLANKn is now SUSPI/BLI, not affected by the Feature Connector Enable Configuration
    c. As a consequence of b. pin 97 is FCBLANKn (not muxed with anything) Please note that FCEVIDEOn is still muxed with SBYI/ACTI as before, as Standby Input and Keyborard Activity are less important functions in a system.
    d. SW0 is no longer muxed on VCLK/FCDCLK. So VLK/FCDCLK is a pin but it moved to pin 103 in the PVDD area, to be consistent with FC power supply
12. SW1, muxed on MCLK/XMCLK (pin197) became SW0. This is just a name change to have the switches placed in a more consistent manner.
13. SW1 is now muxed with a reserved pin: RES4CKE, pin 148, which before was totally reserved. The idea here is to go for pu/pd with SDRAM-s for SW2 and SW1, while keeping SW0 on MCLK even with SDRAM-s.
14. Pin 147 is Reserved. It is actually one of the WavePort pins, but placed in-between Memory and Panel VDD busses (on MVDD) for maximum flexibility. To acheive this, the pins on its right were moved to the right by one
    FPVEE <BIAS> moved down to pin 98 (it was 105).
15. TRWn is now by itself on pin 96, on FPVDD.
16. The names of all flat panel data pins reflect the panel type table attached to this document.

Configuring Nordic-1M

If Terminator used specially assigned pins to configure the chip, **Nordic-1M will use some of the MD31:0 pins sampled on the Reset trailing edge,** similar to Mustang. The pad cells will have an active pull-down controlled by an **extended Reset** signal. The pull-down resistence will be about 75KOhm. An external pull-up less than 60KOhm is needed only if the option is used. In Suspend, the MD pads are inputs and the DRAM OEn is H so no DC current is drawn by the configuration h/w. An external resistor is needed only if the configuration pin has to be H at Reset. H/W configuration can be read via s/w too.

All h/w configuration latches are read accessible via I/O. The h/w configuration is latched on Reset trainling edge. (these latches were r/w, with s/w PU read, having

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only read is enough).
We'll define the configuration pins to minimize the number of external resistors:

CPU Bus Configuration:

On MD18:16 & -> no external PU = 32bits VESA VL bus at 33MHz or less bus clock
& MD23 -> MD16 PU = 32bits PCI bus with Burst PU called "PCIPU"
-> MD17 PU = 16bits ISA bus PU called "ISAPU"
ISAPU controls also the pin EBROMn/SLEEPIn
In ISA bus this pin is EBROMn output; otherwise it is SLEEPIn input to be tied H if not needed.
-> MD18PU = 32BIT VESA VL BUS AT 50MHZ BUS CLOCK
PU called "FVLPU
-> MD23 PU = 32bits PCI bus no Burst PU called "PCINBPU"
This is a reserved configuration in case burst does not work on a PCI bus.

Reads-back in SR22:

PCIPU on MD16 -> SR22[0]
ISAPU on MD17 -> SR22[1]
FVLPU on MD18 -> SR22[2]
PCINBPU on MD23 -> SR22[7]

Clock Configuration:

On MD19 (reads back on SR22[3])
-> no external PU = internal MCLK and VCLK clocks, from the internal clock synthesizer
-> MD19 PU = use external clocks from SW1/MCLK/XMCLK and OSC/XVCLK
PU called"XCLKPU"

This PU is used for manufacturing test.

One reg. bit is needed if internal clock is selected to control outputing mclk on the MCLK/XMCLK pin = 1 if use internal clock then output it on SW0/MCLK/XMCLK pin. -> SR23[0] is this bit.

Memory Configuration: SRF[0]
No Pins, Use Two Register Bits -> 2CAS/2WE bit=H 2WE, bit=L 2CAS (default =L)
-> Symetric/Asymetric bit=H Asym., bit=L Sym. (default=L)

BIOS Support: (reads-back on SR22[6] for BIOS8PU)

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Nordic-1M supports 16bit or 8bit BIOS and only in ISA bus configurations
The BIOS is always supported when in ISA.

On MD22 -> no external PU = 16bit BIOS
-> external PU = 8bit BIOS (no MEMCS16n decode on C000)
This option is mostly for debug in case 16 bit BIOS range decode is not fast enough.
If the BIOS support is disabled, this configuration is don't care. Called "BIOS8PU"
Please note that Nordic-1M supports C000 BIOS only in ISA.

In a normal note-book the BIOS is at E000:0 or C000:0 but it is not supported by Nordic: so no external component is needed.

Sleep Address Selection:

On MD21: Sleep Address Selection (reads-back on SR22[5]).
-> No external PU = sleep at 3C3[0] - to be used when Nordic is on the Mother-board (most cases)
-> External PU = sleep at 46E8[3] - to be used when Nordic is an adapter (like a PCMCIA card and/or an adapter to turn desktop into an environment friendly PC) Called: S46PU
Note that Nordic-1M comes-up awake.

Feature Connector Configuration: (reads-back on SR24[7])
On MD25:
-> No external PU = no Feature Connector Support: outputs used only for FC are forced L, I/O are forced inputs, I/O and inputs are forced on the chip so that they do not take power if not connected externally.
-> External PU = All pins needed for FC including OVRW are active.
Called: VAFCPU

~~On MD26: Alternate SW0 Selection (Reads-back on SR24[0] when SR24[7] is 1)~~

Total: 9 H/W PU configuration options.
In normal operation with FC enabled up to three external PU-s may be needed (bus type if not VL and FC).
In normal operation with FC disabled up to one external PU-s may be needed (bus type if not VL and FC)

Summary of PU/PD Configuration Pins and Register Bits where they can be read-back:

SR22 [7:0] H/W Configuration Read Register #1

Read only register, written on reset training edge by activating PU/PD on MDi pins. The PD-s are inside the pads active only during XReset (extended reset).

[7] 32bits PCI bus no Burst h/w PU configuration on MD23. It is called "PCINBPU" (read only bit).
This is a reserved configuration in case burst does not work on a PCI bus.

[6] Select 8 bit BIOS support (if 1). Otherwise 16 bit BIOS support if the BIOS support is at all enabled. PU on MD22.

[5] Resereved for Sleep Address Select: reads back S46PU (MD21).
1 = I/O address 46E8[3] as sleep address (needs external PU).
0 = I/O address 03C3[0] as sleep address (no external PU is needed).

[4] Reserved

[3] Select external clocks: MCLK and VCLK on SW0MCLK/XMCLK and OSC/XVCLK. (default: internal clock synthesizer, SW0 and OSC).
PU on XCLKPU on MD19.

0 = internal clocks with the pins used as inputs for panel type switch #1 and OSC. If SR23[4] and SR23[0] are 1, VCLK and SW0/MCLK/XMCLK, respectively become VCLK and MCLK outputs respectively, for test purposes (only if SR22[3]=0 MCLK can be seen, but VCLK can be seen even if SR22[3]=1 as long as SR23[4]=1)

1= SW0/MCLK/XMCLK and OSC/XVCLK become XMCLK and XVCLK inputs generating directly chip MCLK and VCLK without clock synthesizer. The clock synthesizers are powered down if SR22[3]=1.

[2] Select VESA VL Bus at 50MHz
1 = VESA VL bus at 50MHz selected (needs external PU on MD18)
0 = VESA VL bus at 50MHz not selected

[1] Select ISA Bus with PU on MD17.
1 = ISA bus selected (PU on MD17)
0 = ISA bus not selected (no PU on MD17)

[0] Select 32bit PCI Bus with PU on MD16.
1 = 32bit PCI bus selected (PU on MD16)
0 = 32 bit PCI bus not selected (no PU on MD16)

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If [1:0] = 00 (i.e. no external PU on MD17:MD16) 32bit VESA VL bus is selected.
No more than one PU on MD17:MD16 should be used.

Note: In AVGA3, CF14 is "Enable Local BUs Address Latching Interface". Alpine does

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not have this configuration bit. We need to do what was done in Alpine to get rid of this Configuration Pull-up/Pull-Down option. *CAN we? WAs this done, Dwarka?*

SR24 Panel Type Switches Register

[7] VAFCPU (VESA Advanced Feature Connector External Pull-up) Read-back. If external pull-up (the bit read-back 1) then all VAFC pins are configured for Video Port. Otherwise they have other functions or are disabled if no other function. (Disabled= the inputs are forced = the TTL and CMOST threshold controls are off & the outputs are tri-stated. It actually reads back what is latched on Reset on VAFCPU. VAFCPU is on MD25.

[2:0] SW2:0 pins read back (read only bits) ~~Please note that bit [0] reads back SW0 if VAFCPU (SR25[2]) is 0 and ASW0PU if VAFCPU is 1.ASW0PU is on MD26.~~

Configuration Register Bits needed:

Symetric/Asymetric DRAM -> SR8[7] in T1, CF13 in AVGA3
=> SRF[1] 0 = Symetric DRAM Default: 0
1 = Assymetric DRAM

This bit is read only in AVGA3 (reads back CF9), but it is writable in T1. It controlls MCLK frequency as an alternate to SR1F. We will use only SR1F to program MCLK frequency in Nordic. The default MCLK frequency will be 39.374MHz, corresponding to SR1F[5:0] = 18H=22D. This frequency fully meets the spec for -80 256Kx16 DRAM-s.

Two CAS or two WE DRAM -> pin 72 in T1, CF12 in AVGA3
=> SRF[0] 0 = 2 WE DRAM (Default:0)
1 = 2 CAS DRAM

16 or 32bit wide Video Memory (One or Two 256Kx16 DRAM-s or SDRAM-s)
-> not in T1, SRF[4:3] in AVGA3 (01=16bit, 10=32bit)
=> SRF[7,4:3] will be used in Nordic with the same encoding as in AVGA3. (11 is reserved for 64bit wide). Default: 10 (32bit). See Table next page. Please note that we have room to add other types of DRAM-s (SDRAM-s for instance).

In AVGA3 SR8[0] is "CS OUt to EEPROM" a feature Nordic does not Support. Nordic will not change the meaning of AVGA3 bits unless they are read only (like the pins or external PU read back).

SR8[2:0] are in T1 the read-back bits for SW2:0 input pins, but AVGA3 uses them for EEROM programming so we moved SW2:0 read back to SR24[2:0].

In T1 SR8[7] is symmetric/assymetric addressing... in Nordic this is SRF[1].

Two or one Bank 32bit wide DRAM

-> not in T1, SRF[7,4:3] in AVGA3 (00=8bit, 01=16bit, 10=32bit, 11=64bit, SRF[7] controls if 2MB of Video memory are available with 4x512kx8 -0- or with 4 256Kx16 DRAM-s, two banks -1-). *It seems that in AVGA3 to support 1MB with two 256Kx16 dram-s and 32bit wide bus, we select 32bit wide and SRF[7]... but I do not exactly know how this configuration is selected.*

=> SRF[7,4:3] in Nordic, will select the Video Memory Configuration slightly differently than in AVGA3 and Alpine. See the following table.

	SRF[7]	SRF[4]	SRF[3]	Memory Configuration
new	0	0	0	32bit, 2MB=4x512Kx8
	0	0	1	16bit, 512KB=1x256Kx16
	0	1	0	32bit, 1MB=2x256Kx16 (default)
	0	1	1	Reserved (64bit in Alpine)
new ?	1	0	0	32bit, 2MB=4x256Kx16, Two Banks
	1	0	1	Reserved
	1	1	0	Reserved
	1	1	1	Reserved

DRAM Timing select (short RAS or long RAS)

-> SRF[2] in T1 and AVGA3

=> SRF[2] in Nordic, default 1 = short RAS (3.5 L, 2.5H)

BIOS 48KB or 32KB -> not in T1; CF8 in AVGA3. In T1 SR8[4] is Suspend pin polarity. In Nordic Suspend pin is always active L (0 on pin puts the chip in Suspend).

=> SR23[2] in Nordic =0 32KB BIOS (default=0) C0000:C7FFF

=1 48KB BIOS : C0000:CCFFF

The initial BIOS code should be placed in the first 32KB starting at address C0000.

BIOS ROM ZERO* wait select in ISA and fast timing in VL bus

-> not in T1; CF1 in AVGA3

=> SR23[1] in Nordic =0 no ZERO wait state for BIOS in ISA

=1 ZERO wait state for BIOS in ISA, 8MHz bus

Output internal VCLK on VCLK/FCDCLK pin -> not in T1 or AVGA3

=> SR23[4] in Nordic =0

VCLK/FCDCLK is an output pin forced L

=1 either VCLK or

FCDCLK is outputed on this pin,

depending on VAFCPU (read back in SR24[7] value).

If SR24[7]=1 (Feature Connector pins enabled) than FCDCLK is outputed, otherwise, if

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SR23[4]=1 than VCLK is outputed. VCLK out is needed only for manufacturing test

Output internal MCLK on SW0/MCLK/XMCLK pin -> not in T1 or AVGA3
=> SR23[0] =0 this pin is an input namely XMCLK if SR22[3]=1 (enable external clocks) and SW0 otherwise.
=1 output mclk

This pin will normally be used as SW0, except for manufaturing test where mclk and xmclk functions are needed.

SuspendI/BLI bit -> not in T1 or AVGA3.
=> SR23[5] in Nordic, 0= Suspend pin in Suspend/BLI pin (default)
1= BLI pin on Suspend/BLI pin

SBY/ACTI/FCEVIDEOn bit. -> not in T1 or AVGA3
=> SR23[6] in Nordic, 0= SBY on SBY/ACTI pin (default)
1= ACTI on SBY/ACTI pin

If SR24[7] = 1 (VAFC pins enabled) this pin is FCEVIDEOn independent of SR23[6].

VAFC Enable bit -> not in T1 or AVGA3.
(read only bit, actually reflecting the status of an external configuration PU: VAFCPU on MD25 latched at RESET or under S/W Control)
=> SR24[7] 0= VAFC Disabled at pins.
All VAFC dedicated pins are disabled to save power: inputs are disabled, outputs are L. **I/O-s are disabled inputs (forced H)** internally. The shared pins are not in Feature Connector configuration.
1= VAFC Enabled at pins.
If any shared pins, they are now in Feature Connector Configuration.
All dedicated pins are active in this configuration.

Compressed Live Video (SashaPack) Enable bit -> not in T1 or AVGA3.
=> SR24[6] 0= disable (default)
1= enable

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~~Audio In (from CS4215 to Nordic) Enable bit -> not in T1 or AVGA3.~~
~~=> SR24[5] 0= disable (force inputs inactive and outputs L~~

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~~disable AI-FIFO and cycles,~~
~~1= enable~~

~~Audio Out (from Nordic to CS4215) Enable bit: -> not in T1 or AVGA3~~
~~=> SR24[6] 0= disable (as above but AO-FIFO)~~
~~1= enable~~

Panel Type Switch Read-back -> SR8[2:0] in T1 or SR7[6:4], not in AVGA3
=> SR24[2:0] in Nordic, read only, writable on Reset or under S/W Control (SR24[3])
When SR24[3] whose default is 0, transits from 1 to 0 SW2:0 pin value is latched into SR24[2:0 which cannot be written by I/O.

Please **note** that **R9x[1:0]** TFT Panel type field of T1 was expanded to support 24bit TFT panels:

00 -> 9bit (333) (as in T1)
10 -> 12bit (444) (as in T1)
01 -> 18bit (666) [was x1 in T1 covering both 01 and 10 !!]
11 -> 24bit (888) -> new in Nordic

Notes:

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0.1 a. If 24bit TFT panel is selected, all related pins will be configured for it and it has priority over panel pins configuration settings for cross talk reduction enabled.
b. MOD is selected only with STN panels.
c. If 24bit TFT is not selected and VAFC is not selected, then SUSPST is selected on
G1/SUSPSTn/FCP[1] and SBYST is selected on G0/SBYSTn/FCP[0].
d. Panel Data unused output pins are forced.0 when not in use (depending on panel type)

SR25 Timers S/W Reset, H/W Config. #2 & Packed Modes Register

[7] The 8514A RAMDAC address is decoded as valid RAMDAC address in addition to the standard VGA RAMDAC address.
[6] Allows use of EBROMn as external 8514A RAMDAC
In this case it bahaves like 5428.
[5] Enable 1bit/pel packed mode
[4] Reserved for 2bit/pel packed mode
[3] Enable 4bit/pel packed mode
[2] Configure PCI bus Nordic module for Faster PCI write
[1] Reset Stand-by Timer
[0] Reset Backlight Timer

Other Register Related Topics
(See nordic-regs-rev#.lst where # is the latest one)

BIOS SCratch Registers #5 and #6 (2 extra required) (r/w)

SR28:SR29[7:0] are scratch registers.
Note that SR9, SRA, SR14 and SR15 are AVGA3 scratch registers which we keep in Nordic. Also there are 13 18 bit scratch registers in the RAMDAC is SR12[1]=1.

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R9x - TFT Panel Data Format

---

[7] Reserved

[6:4 Select a 0 to 7 shift-clock delay from the internal character clock counter
(8 VCLK/Character Clock) to TFT panel HSYNC (LLCLK) signal -> as in T1.

[3:2] Panel size select:
00 -> 640x480
01 ->

[1:0] TFT Panel Type:

00 -> 9bit (333) (as in T1)
10 -> 12bit (444) (as in T1)
01 -> 18bit (666) [was x1 in T1 covering both 01 and 10 !!]
11 -> 24bit (888) -> new in Nordic

Registers that are Moved Relative to T1

CR1B[7,4,3,2] (R1B in schematics):

[7] Disable Text Cursor Blink in T1. Do we use this feature in T1?
Enable Blank End Extensions in AVGA3
[4] PCLKO (Panel Clock) no divide by two control in T1.
I am not sure this bit is actually needed in Nordic.
[3] IRQ Every Frame or Every Other Frame ? Is this bit used inT1?
[2] Not Used at All in T1.

I think that all these bits are not actually used. Are they needed ? -> Robin.

CR1C[7:0] & CR1D[7:0]

Are important LCD and Power Management Registers in T1 and Overlay Registers in Alpine. These registers are not in AVGA3, but because they are used in Alpine we may move them to **CR2C[7:0] and CR2D[7:0]**, which requires one more CRTC Index Register Bit. So:

CR1C -> CR2C & CR1D -> CR2D in Nordic relative to T1.

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SRF[7]

In T1 is CRT Refresh Disable. This bit gates /FB/RWC[5] in FB sheet 6. In AVGA3 is DRAM Two Bank Configuration select bit.
I don't think that this bit is used in T1 ? -> Robin.

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SR16

In T1 is used to control the pads for power and threshold. In AVGA3 is not used. In Alpine is CRT FIFO demand threshold and other things ([4:0] are used).

Move SR16 bits of T1 to SR20 to avoid contention with Alpine. Increase SRX Sequencer Register Index to 6 bits.

SR1A

In T1 is used as Test register. In AVGA3 and Alpine is Signature Generator Result Hi. Move T1 SR1A bits to SR21 if it is not replaced by a similar register in AVGA3.

Nordic Revision and Mask Codes

Nordic Microsoft ID CR2F: CD
Nordic Revision CR27 (4bits chip code, 7z , where z is BIOS rev. counting down): 2F
Nordic Mask Code CR25: 00
Nordic PCI ID: 1200H

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```
User name:    SHAW (11)                    Queue:   UIDESK/UNIX_UIMKGT
File name:                                 Server:  CLFPCD010
Directory:
Description: NORDIC29.
             December 21, 1998                          5:38pm
```

EXHIBIT
RX-581 C

```
 SSS  H   H   A   W   W
S   S H   H  A A  W   W
S     H   H A   A W   W
 SSS  HHHHH A   A W W W
    S H   H AAAAA W W W
S   S H   H A   A WW WW
 SSS  H   H A   A W   W


L      SSS  TTTTT
L     S   S   T
L     S       T     : :
L      SSS    T     : :
L         S   T
L     S   S   T     : :
LLLLL  SSS    T     : :
```

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NORDIC-1M Design Specification

by Vlad Bril, Robin Han, Sasha Eglit, Rakesh Bindlish, Dwarka Partani.
Jeff Ort
rev.5.2 December 21, 1998

1.0 Introduction & Table of Contents

Nordic is Cirrus Logic's Fourth Generation Flat Panel VGA Controller to be marketted in first half of 1994.
Nordic-1M is a mid-end member of the Nordic family. It is a GUI Accellerator with PCI support and Multi-Media Features.
Nordic-1M is targetted for the mid to high end of the **Note-book Computer Market** and for for the energy efficient **desk-top computers mother-boards**.
Nordic-1M is **not** targetted to the adapter market.

1.1 Table of Contents

This Specification will address the following:

1. Introduction and Table of Contents
2. Basic Feature Set
3. Detailed List of Features
4. Pinout and Pin Description
5 Architecture Specification
6 Register Specification - this is a diferent document
7. Product Implementation Plan - this is also a diferent document

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2.0 Nordic-1M Basic Feature Set

1. **Flat Panel VGA Compatible GUI Accellerator register and feature compatible to 5428 and Alpine I A/V. Priority: A (= highest).**
2. **32bit CPU, 32bit Video Memory, 32bit BLT and 32bit CPU to Video Memory Data Path. Priority: A (= highest).**
3. **208 pin QFP package.**
4. **Targeted to sample CY Q1'94, production CY Q2 '94. Priority: A (= highest).**
5. **Target cost: $12 to $10 -> less than 400mil [/] in C8 Foster City.**

6. **Multimedia Features**

- Part of a well defined **System Solution** for high performance **CD-ROM video and audio playback** for the portable market. **Priority: B**
- Part of a well defined **System Solution** for mid performance **low cost live NTSC Video and Audio with the NTSC decoder on a PCMCIA card. Priority: B**
- ~~**Audio Port to Display Memory**: Audio Buffer to Serial Interface for CS4248 Audio Codec. **Priority: C** (CS4215 is not fit for notebook computers).~~
- **Video Playback decompression accelleration for CinePak** including Color Space Conversion (YUV -> RGB). **Priority: B**
- **Live Video in a 320x240 or 640x480 Window** from a proprietaryly compressed TV decoded data source (at 30Hz) on TFT color panels. Data is stored compressed and it is decompressed to 18bit/pel or 24bit/pel in real time at display time. NTSC decoder and data compressor is on the PCMCIA card or the PCMCIA controller. Please note that due to live video bandwidth requirements on PCMCIA bus , a relatively non-expensive way to achieve the second feature is to implement this compression algorithm. **Priority: B**
- Color Key Live Video Overlay based on a 5428-like Feature Connector with PCI bus (only).

7. **Integrated in Nordic 1-M**

- Color Space Converter for CinePak. **Priority: B**
- 18bit DAC with direct color capability **Priority: A**
- *24bit RAMDAC with true color capability* **Priority: C**
- Clock Synthesizers for Video and Memory Clock (65MHz/3V, 110MHz/4.5V). **Priority: A**

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- DAC IRef Current Source on chip. **Priority: C.** *Boyd and ManShek are working on it*

8. **Direct Bus Interface**:

- 32bit VESA-VL bus (and 486 local bus) **Priority: A**
- 32bit PCI bus. No on chip BIOS ROM support in PCI. **Priority:** A
- 16bit ISA bus for demonstration and easy system validation. **Priority: B**
- 32K or 48KB BIOS ROM support in ISA and VESA VL bus **Priority: B** (only for BIOS/ system debug)
- At least 5 scratch pad registers: optimum 8 scratch pad registers. **Priority: A.**

9. **Performance Enhancements** to achieve 15-20MWinmarks at 1Kx768 8b/pel:

- 32bit BitBLT with memory mapped I/O BitBLT registers (as in 5428 ?or Alpine) Priority:A
- BLT buffer of 8 (~~or16~~) bytes for Source (and Destination ?) data, (5428 buffer is 8bytes, Alpine is 16bytes) (as 5428)
- *X/Y offset for Pattern BLT (as in Alpine)* **Priority:** C
- h/w graphic cursor 64x64 (as in 5428)
- color expansion (as in 5428)
- linear memory addressing (as in 5428)
- 4 stage 32bit wide write buffer and capability to page CPU cycles if accumulated in the write buffer (this is already in 5428)

10. **Display Memory:**

- *0.5MB (16bit wide)*, 1MB or 2MB memory addressing 32bit wide (as in 5428)
- *1 or* 2 256Kx16 one bank or 4 256Kx16 two banks (2 CAS symetric, 2 WE asymetric) (as in 5428)
- maximum memory clock frequency: 50MHz/3V, 65MHz/4.5V **Priority: C**

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11. **Flat Panel Support**: **[Priority: A]**

- Color TFT (24bit, 18bit, 12bit, 9bit)
- Color Dual Scan and *Single Scan STN* (16 and 8 bit, including dual clock panels)
- Monochrome TFT (8bit),
- Monochrome Dual Scan STN (8bit),
- Monochrome Single Scan (4 and 8bit) support

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- Simulscan with all Fast Panels (6.3MHz or equivalent) with 32bit wide memory
  No simulscan with 16bit wide memory with dual scan color panels
  No simulscan for 3MHz monochrome dual scan panels
- 640x480 single and dual scan support (Priority:A)
- 800x600 TFT *and no single and dual mono and color STN panel support (Priority: C)*
- 1024x768 TFT *and no single and dual scan STN panel support . (Priority: D)*

12.Display Features

- High quality monochrome and color shading, at least as good as 6440. Priority: A
- Shading option for fast panels. Priority: B
- Up to 8, 64x64 Hardware Icons independently mapped color+transparent background. **Priority: C**
- *Whisper Cross-Talk Reduction (If panels will be available in the time frame and if we can accomodate it with the shading algorithm).* ***Priority: C***
- ***"Office Productivity Booster Dual Display"*** 640x480 (panel) & 640x480 (CRT) 4 or 8b/pel or 640x480 (panel) & 1024x768 (CRT) 4 or 8b/pel ***Priority: E***
- Vertical Expansion in text and graphics (as in 6235 or 6440)
- Automatic Centering if not expanded (as in 6235)
- *Grey-Shades Maping options ?? Is this needed ? Priority: D*
- Text Contrast Enhancement options. (as in 6235 or 6440)
- *Inking Plane ?? Priority: D*
- *180 and 90 degree image rotation ?? Priority: D*
- *12 and 16dots wide font support ?? Priority: D*
- *h/w offset on h/w cursor ?? Priority: D*

13.Resolutions Supported:

- the same as 5428 at 5V (4.5Vmin)
- up-to 45MHz dotclk (1024x768, 60Hz interlaced) at 3.3V

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14.Power Management

- Mixed 3.3V and 5V operation: memory, host and flat panel independent VDD
- Green-PC spec support. **Priority: B**
- Stand-by Mode with internal stand-by timer (as in 6235)

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- Suspend Mode I/O or pin in all modes (LCD, CRT,Simulscan)
- *Light Sleep ?? - better not for this chip as it requires too much h/w. Priority: F*
- Panel Power Sequencing: automatic or under I/O control (as in 6235)
- Reduced Active Power in Panel Only Operation: < 60mAmp @3.3V **Priority:A**
- Reduced Suspend Current: < 0.5mAmp. **Priority: A**

2.1 Inputs from the Nordic-1M Features Meeting of 09/10/93

- 24bit DAC if not too expensive (VAR)
- mclk @5V max 65MHz, @3V max 50MHz
- vclk and fpvdclk @5V max 85MHz, @3V max 65MHz
- **panels:**
  - TFT 1280x1024? ##, **1kx768 ##, 800x600 ##**, 640x480
    24bit,18bit, 12bit, 9bit color, 6bit mono
    NEC analog output? ##
  - STN 800x600 dual scan color, 640x480 ds color 16bit
    640x480 ss color 8bit
    640x480 mono bit 8bit and 4bit
  - horiz ## and vertical centering
  - normal 9dot font in 800x600 text ##
  - simulscan for 800x600 and 1kx768 panels ## (need to run all modes at 800x600 or 1024x768 rezolutions -> option to clock panel till h&v Blank)
  - support for two alternate fonts 10x24 for 800x600 (10x18 actual with spacing) and 12x25 for 1kx768 ## difficult !!
  - h&v text expansion in 800x600 and 1kx768 panels ## ?
  - color text enhancement ## : bright white instead of white
  - *on chip cross-talk reduction ##* ? - any improvement ?
  - *shading look-up tables ##* ? - only if not too large
- ***NO Whisper support even on the bus side - out !***
- ***NO one 256Kx16 DRAM support - out !***
- **h/w icon support:** with h/w cursor, up to 4 simultaneously. Horizontal position controlled in increments of 64 pixels.
  Icon attributes: off/on, 4 colors/3colors + transparent, no_blink/blink, (simple/double).
  H/W cursor goes over the h/w icon (visually). Uses independenly mapped color in RAMDAC RAM. Start at scan-line 64.
- PC98 integration? ## - to be negotiated
- reserve pins for SDRAM-s and CDRAM-s ##
- ***NO true dual display***!

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2.2 Inputs from Compaq 09/10/93

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- 50MHz 486DX bus
- 75Hz refresh rate
- **need one 256Kx16 support with Audio and some video for Contura - build one motherboard for Contura and LT Lite. Two DRAM-s only on LT Lite.**

- think that 8KB/buffer of audio buffer is not enough
- want to use Analog Devices for Audio
- No clear winner on conpression. They are watching. Need Indeo driver
- Play-back zoom is required. At least pixel replication
- Very interested in Compressed Live Video. WAnt to talk more
- need h/w icon 64x64 with 3col+transparency or 4 color, with pixel replication to 128x128.

2.3 Inputs from AST 09/15/93

- They prefer horizontal icon

2.4 New Features as of 10/04/93

- 4bit/pel packed support for Windows Chicago
- 8bit/pel video out to the Feature Connector for conversion to NTSC-out with Nordic running 640x480 interlaced mode.
  Another idea was to use some of the panel outputs in this case and extend the data out to 16bits.
- The h/w icon can be horizontal or vertical using the Motion Video Window as implementation vechicle -> is it worth?
- IBM Raleigh asked for 12 and 16dots wide fonts for h/w assisted Kanji. 10/04/93
- IBM Raleigh asked for 8bit monochrome TFT panel support. 10/04/93

3.0 Important Additions to 5428 Data Base

1. **32 bit CPU Data bus in VESA VL bus support**
2. **PCI bus support**
3. **Mono and color, STN and TFT Flat Panel support (incl. hfb).**
4. **Live video in a true color window with Windows running in planar VGA mode, without a video port (using PCMCIA standard bus and Sasha's decompression technique).**
5. **CINE PAK decompression accelleration**
6. **Audio Port support for CS4215**
7. **Power Management: panel power sequencing, stand-by mode, suspend mode**
8. **Mixed Voltage, 3.3V operation and low active/suspend/standby power**
9. **h/w icon support, with a h/w cursor support**
10. **BLT performance improvements: Memory Mapped BLT I/O, patternning, 16 byte Source buffer**

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11.*[dual display 1024x768 on CRT with 640x480 on LCD, using the same RAMDAC] - if decided to do now*

4.0 Detailed List of Features

4.1 WAS: On the Cross Talk Reduction Technique -> not in - 1M

This part was deleted from Nordic-1M spec starting rev. 3.8 (09/11/93).

4.2 Green PC Spec Support (Based on VESA DPMS Proposal 1.0p rev. 0.53p)

This specification refferes to CRT Monitor power management. Additionally, Nordic will

TABLE 1. Display Power Management Summary

State	HSYNC	VSYNC	Video RGB	Compliance	Power Savings	Recovery Time
CRT On	Pulsese	Pulsees	Active	Mandatory	None	NA
CRT Stand-by	No Pulses	Pulses	Blanked	Optuonal	Minimal	Short
CRT Sus-pend .	Pulses	No Pulses	Blanked	Mandatory	Substantial	Longer
CRT Off	No Pulses	No Pulses	Blanked	Mandatory	Maximum	System Dependednt

control DAC power consumption. These power management CRT Monitor states are not necessarily related to the graphics controller power management states.

We'll define 2 bits - GRE[2:1] (the same as Alpine) that control HSYNC, VSYNC and DAC Power Off signal (or Blankn to the DAC).

TABLE 2. GRE[2:1] Effect

GRE[2:1]	CRT State	Vsync	Hsync	DAC Power	Nordic Power Management State
0	On	pulsing	pulsing	on	active
1	Stand-by	pulsing	static at MISC[6] inactive level	off	active
2	Suspend	static at MISC[7] inactive level	pulsing	off	active or stand-by
3	Off	static at MISC[7] inactive level	static at MISC[6] inactive level	off	active, stand-by or suspend

If Nordic is in its own Suspend mode, the BIOS should program GRE[2:1]=3 to put the monitor (if any) in the Off state.

If Nordic is in its own Stand-by mode, CRT Suspend mode should be forced bt the h/w, as stand-by is a timer driven mode and no s/w gets to play.

If Nordic is in LCD only, the BIOS should set GRE[2:1] to 3 to power off the CRT that may be connected to the notebook computer.

If CRT only mode and CRT is in stand-by or suspend, the BIOS may reduce the video clock and even memory clock frequencies after saving the current values.

Except for the above restrictions, CRT Power Management modes are not related to Nordic power management modes: they can be independently programmed.

If MISC bit is programmed for positive polarity, the SYNC signal will be stopped L, otherwise it will be stopped H.

4.3 Play-back Decompression Accelleration (applicable to Cinepak as well as other compression standards) - old, kept here only for reference

4.3.0 The problem **Cirrus Confidential Business Information** **CL 152692**

a) When playback data is compressed on a CD ROM, it is encoded in 24bit/pel YUV with crominance sub-sampling. Due to CDROM reduced bandwidth the display window is 160x120 or 320x240. If this compressed data is decompressed at full pixel depth, it should be displayed as 24bit/pel RGB window under MS Windows. As the play-back data is sent to the graphics controller from the CPU bus, it has to be placed in Video Memory in 320KB

A standard VGA controller or even GD5428 are able to display the 24bit/pel play-back window only if MS Windows is run in 24bit/pel mode (for instance 1024x768 24bit/pel or 640x480 24bit/pel) by the driver. Under these conditions, the CPU will have to write the un-compressed 24bit/pel play-back data in the appropriate position in Video Memory, contigouus to the entire displayed data.
So, in order to display 24bit/pel in a play-back window, GD5428 needs the driver to run 24bit/pel at the maximum display resolution.
But, in order to run 640x480 at 24bit/pel we need 921.6KB of Video Memory and in order to run 1024x768 24bit/pel we need 2359.296KB of video memory. (Please note that 2M of memory has 2097.152KB).
Also, when running windows in 24bit/pel mode the performance will decrease 3 or 4 times relative to 8bit/pel mode, especially when using DRAM as Video Memory.

b) When running through MS Windows GDI, the driver can play-back data at 15fps or less (with a 486 33MHz). It is desirable to play-back data at 30fps.
This can be accomplished today only if the driver does not go through GDI.

c) If a picyure was stored on CDROM at low resolution (160x120 or 320x240) and it needs to be "zoomed", it has to be interpolated both horizontally and vertically for good picture quality. Vertical interpolation is expensive in h/w.

4.3.1 The Generic Solution - old, here for reference only

Today's Windows Accellerators run MS Windows, including the play-back window with the same pixel depth (8bit/pel), normally going through the RAMDAC, but using a split palette approach with 16 colors reserved for MS Windows and 240 colors reserved for the play-back window. The Cinepak driver writes data in video memory in 3:3:2 RGB format

(8bits/pel) which is created by the driver. Because of the s/w overhead involved in decompression as well as the GDI overhead, it is hard to go beyond 320x240 clips at 15fps, though the display quality is much lower than what Cinepak could achieve (240 colors versus 16 million colors).
To run Cinepak with 24pit/pel resolution, today's graphics controllers would require to run MS Windows in 24bit/pel mode, requiring almost 1MB in 640x480 and over 2MB-s in 1024x768 modes.

A graphics controller that could run MS Windows in 8 or 16bit/pel mode while displaying only the play-back window in 24bit/pel mode would increase significantly picture quality without degrading too much MS Windows performance with play-back. would reduce significantly the amount of Video Memory required for the same picture quality and would allow a higher frame rate for the play-back.

Further, if the play-back data is stored in Video Memory in a semi-compressed format that requires less than 24bit/pel this would further decrease the Video Memory requirements and it may even reduce the video memory band-width requirements.

When zooming the play-back window from 160x120 to 320x240 or higher it is important to interpolate. Vertical interpolation can be done in s/w but with a relatively large overhead. It may be possible to do vertical interpolation on key frames, but there is no practical way of doing vertical interpolation on inter-frames either in s/w or with h/w assist on the CPU write side of the graphics controller. If s/w driven vertical interpolation on key frames is not a solution, then verical interpolation can be only achived in h/w on the CRT read side and this requires either one or two 16bit/pel line buffers or a big penalty on video memory bandwidth (the equivalent of reading 32 or 48bits/pel).

Horizontal interpolation can be done before play-back data is displayed, without s/w help.

Please note that there are multiple ways to solve the play-back problems. In Nordic-1M we'll try to strike a ballance between the complexity of the h/w solution and the quality of the play-back image.

To a large extent, the solution adopted in Nordic-1M will be generic, not tied to Cinepak, though it will be first applied to Cinepak.

4.3.2 Nordic-1M old Play-back Accelleration Solution -> canned, kept here for reference

a)Nordic-1M will run Cinepak at 1:1 scale exactly the same way as today's graphics controllers: in 8bit/pel MS Windows with 8bit/pel (3:3:2 RGB) play-back window

b)Nordic-1M will run 1:2 scale (zoom) in 8bit/pel 1024x768 MS Windows with 24bit/pel (8:8:8 RGB) pixel depth in the play-back window, horizontally interpolated and vertically doubled. Play-back data will be stored in video memory as 16bit/pel (Y0 U01 Y1 U01)

c)Nordic-1M will run at 1:1 scale in 16bit/pel 1024x768 MS Windows with 24bit/pel pixel depth in the play-back window. Play-back data will be stored in video memory as 16bit/pel (Y0 U01 Y1 U01). This mode is good for programs that store data in 320x240 format.

Because today large play-back windows look bad, while small ones look OK, this solution will improve picture quality to a large extent.

Concerns:

Many play-back programs today don't even have a zoom option To this extent, mode b may not be needed.

Mode c could be implemented today with 16bit/pel-RGB (555) in s/w and the only improvement we provide is 24bit/pel capability and h/w color conversion (some level of accelleration). So mode "c" may not be needed as a special h/w.

If this is the case, maybe we do not need to do anything in h/w for Cinepak !

One idea: should we run 24bit/pel MS windows stored in 4:2:2 (Y0 U01 Y1 U01) format? This will allow us to run 24bit/pel MS Windows and use 16bit/pel memory space with no loss of quality. The windows driver could compress the data and the h/w could decompress it.

4.4 Nordic-1M Motion Video Architecture

Sasha Eglit, Rakesh Bindlish, Vlad Bril and Dave Keene are important contributors to the Motion Video Architecture definition.

4.4.0 The Problems to Solve & Generic Solutions

Nordic-1M is supposed to support CDROM play-back and live-video under Microsoft's Video for Windows. With all of today's VGA Compatible Graphics Controllers, the play-back picture pixel depth has to be the same as the surrownding MS Windows pixel depth. In other words, we have to run MS Windows in a 24bit/pel mode in order to display 24bit/pel in the play-back window.
The only way we can run today live video is from a Video Port (= Feature Connector). In this case we'll use an overlay or a color key to define the live video window.
Due to CDROM player, s/w interface complexity, CPU bus and Video Memory limitations, only small clips at 15fps or less can be playd-back today. So today we need a lot of Video Memory to run small clips in slow motion at low rezolution. Nordic-1M will try to use less Video Memory, increase the clips size, their resolution and speed.

Nordic-1M is supposed to support:

- accellerated play-back for all popular CDROM compression standards, especially Cinepak and Indeo
- live video from a PCMCIA card in a system with a standard PCMCIA host adapter, for a "Multimedia-Ready Notebook Computer"
- live video from a Feature Connector, preferably VESA Advanced Feature Connector compatible, for a Multumedia Notebook Computer with direct NTSC input (full mother-

board solution).

What will Nordic-1M bring to the Video plate:

A. Nordic-1M will break the dependency between the pixel depth of MS Windows and the pixel depth of the live-video / play-back window. By doing so, Nordic-1M will be able to run 24bit/pel LV/PB while running MS Windows in 8bit/pel or 4bit/pel (even planar). This will lead to high quality live-video and play-back, while minimizing Video Memory requirements.

B. Nordic-1M will further reduce Video Memory requirements as well as Video Memory Bandwidth requirements by storing data in compressed form: 4:2:2 YUV (16bit/pel), 4:1:1 YUV (12bit/pel) or Sashapak YUV (2.6bit/pel).

C. Nordic-1M will define one architecture and work-frame to run both play-back and live-video in a unitary way for both s/w and h/w.

D. Nordic-1M will support up to two active LV/PB windows at the same time.

E. By providing h/w YUV->RGB conversion and 1:2 zoom Nordic-1M will accellerate playback for most standards, but mostly for standards that allow us access to their decompressor like Cinepack (for whose decompressor we have a licence).

Nordic-1M will not provide Cinepak specific accelleration (custom BLT).

On the Live Video from Feature Connector (or Video Port)

Due to pin-out limitations, the VAFC implementation has to be limitted to 8 pins of data requiring external muxing of 16bit data to Nordic. Further, the VAFC solution will be restricted to 5428 type support: overlay and color key (no memory video port). The only additions to the 5428 support will be the internal YUV-> RGB converter able to accept sequential 4:2:2 YUV (16bit/pel in avarage: Y0,U,Y1,V) and display it as a 24bit/pel RGB in the overlay/color-key window. We may also support horizontal 1:2 zoom with avaraging. Nordic-1M will be back-wards compatible to 5428 and it will support also 16bit 5-5-5 RGB Sierra and 5-6-5 RGB XGA pixel formats. As in 5428, live video from the Feature Connector can be executed only from mode 5F (640x480 256 colors).

In the following we will refer mostly to the other two modes of operation: play-back and live video from a PCMCIA card, which we'll call compressed live video, because due to PCMCIA bus bandwidth limitations, we assume that video data received by Nordic is compressed with Sashapak (see Sashapak detailes further in this spec). Please note that due to its huge advantages, it makes sense to use Sashapak as a mother-board solution too. The main reason we continue to support the Feature Connector based live video is the availability of drivers for 5428 which will give Nordic an early start in the live video arena.

Video Memory Band-width Constraints

Please note that, even with a 32bit wide Video Memory, there are severe memory band-width limitations when running 16bit/pel and 24bit/pel graphics modes.

Assumming that Nordic-1M does 8 CRT fetches in a row and 1 CPU cycle, for a CRT or TFT panel, here are the minimum frequency requirements for memory clock frequency at different rezolutions and pixel depths:

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24bit/pel:
R+7P+R=12m+14m=26m with 1 CPU cycle per CRT FIFO fill fetches data for 32B/3B=10pixels
R+7P = 6m+14m = 20m with no CPU cycle during non-display time
min mclk freq = 65MHz / 50MHz @ 640x480 -> Nordic-1M upper limit at 5V CVDD
= 104MHz / 80MHz @ 800x600 -> too high
= 169MHz / 133MHz @ 1024x768 60Hz -> too high

16bit/pel:
R+7P+R=12m+14m=26m / R+7P = 20m fetches data for 32B/2B=16pixels
min mclk freq = 40.6MHz / 36MHz @ 640x480 -> OK even at 3V
= 65MHz / 50MHz @ 800x600 -> Nordic-1M upper limit at 5V CVDD
= 105MHz / 83MHz @ 1024x768 60Hz -> too high

12bit/pel:
R+7P+R=12m+14m=26m / R+7P=20m fetches data for 32B/1.5B=21pixels
min mclk freq = 30.9MHz / 23MHz @ 640x480 -> OK even at 3V
= 49.5MHz / 38MHz @ 800x600 -> OK even at 3V
= 80.4MHz / 64MHz @ 1024x768 60Hz -> too high

8bit/pel:
R+7P+R=12m+14m=26m fetches data for 32B/1B=32pixels
min mclk freq = 20.3MHz @ 640x480 -> OK even at 3V
= 40.6MHz @ 800x600 -> OK even at 3V
= 52.8MHz @ 1024x768 60Hz -> OK at 5V

We may conclude that Nordic-1M will be able to run 24bit/pel only at 640x480 rezolution. 16bit/pel up to 800x600, 12bit/pel up to 800x600 and 8bit/pel up to 1024x768 rezolution. These results apply only to CRT or TFT and single scan STN panels.
Please note that for dual scan STN panels the memory requirements increase significantly.

These severe memory bandwidth limitations lead us to attempt to minimize video memory traffic. If we store **Cinepak data in 4:2:2, with an avarage of 16bit/pel**, independent of Cinepak window size, **Nordic-1M will not be able to run Cinepak above 800x600.** Any attempt to execute vertical zoom with interpolation, even with two points interpolation will further aggravate this memory band-width bottleneck. The next step should be 100MHz SDRAM-s with a large CRT FIFO (32x32) or 64bit wide memory data bus. These considerations apply to any playback compression standard that stores data in video-memory as 16bit/pel in avarage. The key to a successful compression standard would be one that does decompresssion on the CRT memory read and stores data in memory as 8bit/pel or less, in avarage.

As we store live video at 2.6bit/pel and fetch it as if it was 8bit/pel with Sashapak, Nordic-1M should be able to run live video even at 1024x768.

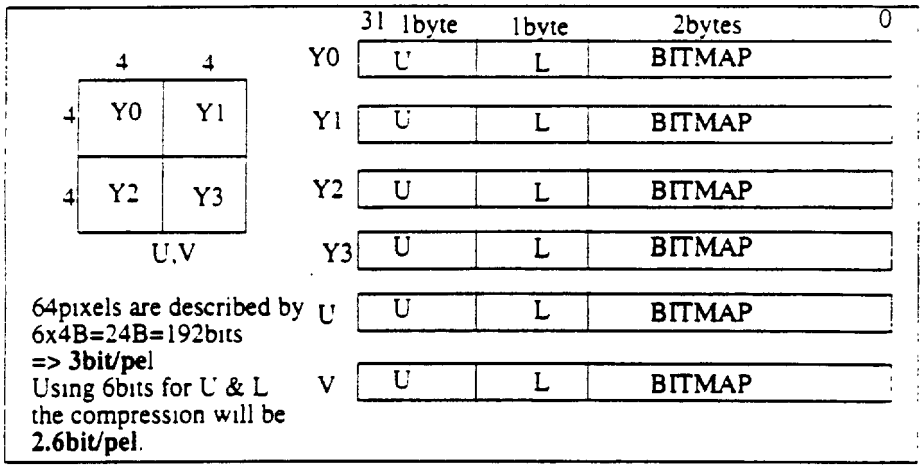
If we defined a new CDROM play-back standard based on Sashapak, then we could run even 1024x768 with 24bit/pel accuracy and keep it memory as an 8bit/pel. **Keith and Ken are actually working on it, with Sasha's help.**

4.4.1 On Sashapak

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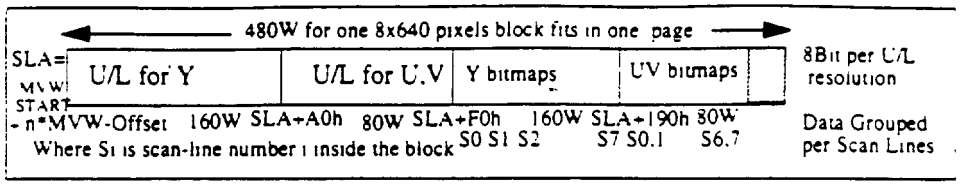
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Sashapak is a highly assymetric, lossy "Block Truncation" compression algorithm optimized for visually equivalent image processing.
Data is proccessed as Y,U,V one byte each. U and V are sub-sampled, characterizing one 8 by 8 pixel array, while Y is characterizing a 4x4 pixel aray Actually one of two values is assigned to each pixel inside the 4x4 (for Y) and 8x8 (for U and V)
At compression time, the compression chip determines a threshold and two values U&L for each group of sixteen (4x4) pixels. This way all pixels above threshold will be assigned the value U, all pixels below threshold will be assigned the value L



At decompression, the bitmap will control a mux between the U and L values. This way the decompression is straightforward.
The main drawback of this approach is that a BITMAP contains Y data from 4 scan lines and U,V data from 8 scan lines. When data is read from memory to be displayed only data from one scan line is used. Similarly the U/L values apply to several scan-lines and the same value will be read in each scan line. The same data will be read again and again in each scan line raising the actual memory bandwidth requirements to an equivalent of 16bit/pel map.
In order to overcome this problem and reduce memory bandwidth requirements, Sasha proposed a **scan line oriented, segregated mode of data organization**. This would require the Sashapak compression chip to write compressed data in a specific way puting the strain on the compresion chip address generator. The basic principles of the new organizations are:
1. Data is organised in the MV Window in chunks of 32 sequential pixels.
a)For **8bit U/L resolution**, as one Y covers 4 pixels, 8 U/L sequential values are needed, 16bits each -> **8x16/32=4W** (8x12/32=3W for 6bit res. U/L) (where W is a 32bit word).
b)U and V U/L data is packed together in the same word (16bits for U U/L and 16 bits for V U/L -> total 32bits=1W) and as one pair of U and V applies to 8pixels, 4 such values are needed for 32 sequential pixels -> **4x32=4W**. (4x12x2/32=3W for 6bit res. U/L)
c) The mask data is also scan-line oriented: all 32bits of Y mask of sequential 32pixels are placed in one 32bit word and due to sub-sampling on U and V, all 32bits of U and V mask of sequential 32pixels are placed in one 32bit word. So in 2W data for 32 sequential pixels on one scan line is packed. -> **2W** (the same for 6bit resolution for U/L)

d) For 640x480 window size, even at 8bit U/L resolution, data for 8 scan-lines fits in one DRAM page (symetric DRAM-s assumed): 320WY+80WU+80WV=480W < 512W page



f) The key to memory bandwidth optimization is the fact the the compression chip will organize data sequentially over 32 pixels instead of 8. This will be done for the mask bits which will be organized sequenually by scan line and for the U/L data. This way a 32bit word of Mask data contains only information for the current scan line and no extra memory fetches are required. The main reason we segregate U/L for Y and U/V is the fact that we want to use 6bit U/L. In this case it is easier to identify the proper U/L info chained within 32bit words if the words are sequential and we have a fix relationship between their address and the 6bit U/L quantities.

g) If we calculate now the amount of data we need to fetch to display 32 sequential pixels:

- for 8bit per U/L: 4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B
  --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
- for 6bit per U/L: 3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B
  --> 32B/32pixels = 8bit/pixel

This is a very good data fetch ratio, much better than the 16bit/pel we'd get without the optimization.

g) When reading data from the Motion Video Window the controller will generate the following sequence of addresses, all of them in the same DRAM page (8bit per U/L):

- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset, +1, +2, +3
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h, +1, +2, +3
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h
- fetch the YU/L for the first 32 pixels on scan-line n at addresses:
  MVW_Start+n*MVW_offset+4, +5, +6, +7
- fetch the UV U/L for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+A0h+4, +5, +6, +7
- fetch the Y BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+F0h+1
- fetch the UV BitMap for the first 32 pixels on scan-line n at address:
  MVW_Start+n*MVW_offset+190h+1
- now the MVW FIFO is full.
- chunks of ten 32bit words will be proccessed for every 32pixels displayed
- the MVW FIFO gets empty after the first 10 words being read for decompression and display.

Please note that all data for every 8 scanlines starting from the top of the MVW is in the

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same DRAM page.
Because we have to fetch the MVW Data before we start displaying it, and because at that time the CRT FIFO does not empty as fast as it is needed (unless MS Windows is running at the same pixel depth as the MV Window), it is necessary to have a separate FIFO for the MVW or at least half the FIFO (at least 10W for 8bit per U/L and at least 8W for 6bits per U/L).
h) When we run 6bit per U/L, because the Video Memory band-width requirements are as if we were running 8bit/pel, we could do vertical zoom with avaraging. But there should not be a need for zoom with Live Video because there is enough CPU and memory band-width to run 640x480 windows even when MS Windows is run as 1024x768 4 or 8bit/pel

Conclusion: With Sashapak we can get data organized in memory such that the memory bandwidth is as for 10bit/pel (8bit U/L) or 8bit/pel (6bit U/L) pixel depth. The actual memory area will be close to 3bit/pel or 2.6bit/pel depending on the resolution of U/L values - 8 or 6bits per value.
Please note that the memory area will be slightly larger due to the fact that we use only 480 words in a page of 512.

4.4.2 YUV to RGB Conversion Algorithm

The ideal YUV to RGB transformation is:
R=Y+1.37V
B=Y+1.73U
G=Y-0.699V-0.336U

After defining an objective way of measuring color error, Sasha came up with the following Conversion algorithm:
R=Y+1.375V=Y+1 3/8 V
B=Y+1.75U=Y+1 3/4U
G=Y-0.375U-0.75V= Y-(3/8U+3/4V).

This algorithm can be implemented with 8 9bit adders and it should support excess 128 or two's complement U,V formats (U,V may be negative while Y is always positive).
This algorithm will be used with Live Video.
For Cinepak, the YUV->RGB converter will be reconfigured to the Cinepak YUV->RGB conversion rule:
R=V+Y
B=U+Y
G=Y-V/2-U/4

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4.4.2 Motion Video Architecture Functional Blocks

Instead of treating play-back and live-video as two separate modules, we'll isolate several generic functions to be used by both:

- Display Window Generation Block:
  allows s/w to define one or two play-back or live video **window(s)**
  The MV Window is defined in memory cycles relative to the start of line in horizontal and frame in vertical direction. Horizontally the unit of measure is different outside relative to the inside of the window: the horizontal window start coordinate is expressed in memory cycles for the surrounding pixel depth (MS Windows pixel depth, normally 4 or 8 bit/pel), while the width of the MVW is expressed in memory cycles for the MVW pixel depth (8bit RGB, 16bitRGB, 422YUV spacial, 422 YUV linear, 411YUV linear, Sashapak).

  - **XS** = MVW Horizontal Start Coordinate (in surrounding pel depth memory cycles)
    The horizontal position is programmed with 8 pixel resolution (0,8,16,... pixels starting from the left side of the screen)
    XS register CR34[7:0] -> 8 bits
    (up to 1K pels in increments of 8 pels)
    To get an early warning, we will require XS to be programmed 8 pixels less than the actual position: 0 is zero, 1 is 16pels, 2 is 24 pels,...
  - **XW** = MVW Horizontal Width (MVW pel depth memory cycles)
    XW register CR35 [7:0] -> 8 bits
    (up to 1K pels in increments of 8 pels)
    To get an early warning, we will require XW to be programmed 8 pixels less than the actual width: 0 is zero, 1 is 16pels, 2 is 24 pels,... width.

  - **YS** = Vertical MVW Start (in true scan-lines not affected by scan-line doubling or panel vertical expansion)
    10 bits in CR36[1:0] (msb-s) and CR37[7:0] (lsb-s).
  - **YE** = Vertical MVW End
    (all bits are programmed, in true scan lines)
    10 bits in CR36[3:2] (msb-s) and CR38[7:0] (lsb-s).
  - **SAdOf=** Surrounding Address Offset (a number to be added every line to the surrounding CRT Address Counter value to allow it to jump over the MVW without counting through it. This allows calculating the surounding restart address.) This number depends on the surrounding mode resolution. Assuming a maximum line of 1024 pels, in increments of 4 pels per address (8bits/pel), 256 addresses is enough -> 8bits.
    8bits in CR39[7:0]
  - **WMAdS** = MVW Memory Address Start in increments of 16KB = 4KW (a phisical address 00000:3FFFF for 1MB or 00000:7FFFF for 2MB Video Memory).
    7bits in CR3A[6:0]

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  - **WMAdOf = MVW Memory Address Offset** (A number to be added to the current MVW Start Address to get the next MVW start Address). Having this s/w model allows panning through a large image for the MVW. The actual image stored in memory may be as large as 1K pixels

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at 16bit per pixel (2 per word) -> 9bits.
9bits -> in CR36[4] (msb) and CR3B[7:0] (lsb)

Because the CRT Address Counter counts surrounding memory cycles, during the MVW display it would count a wrong number corresponding to the MVW pixel depth. To avoid this wrong count, the CRT Address Counter is stopped while MVW is displayed and loaded with the value corresponding to the end of MVW and restart of the surrounding display. As this address value changes every line, an offset is specified and will ba programmed by the MS Windows driver depending on the MVW size and pixel format.
The horizontal size of the window is controlled by a different counter counting to XW
During the MVW display the adddress will be generated by the same CRT Address Counter which will be loaded with a MVW Memory Address Start (WMAdS)

- **XW8P = MVW Horizontal Width in 8 pixel units.** Defines the size of the window in 8 pixel units. It is used to terminate the window horizontally. It may require to program the value minus one or two. To be Defined Later. Register CR3D[6:0] will contain this value.

Every scan-line

MVW Scan-Line Start Address = Previous Scan-Line MVW Start Address + WMAdOf

Scan-line doubling for "zoom" should be taken into account when designing the MVW Architecture: on the address generation block.

- **Off-screen MV Memory Addressing and Access Control.** This includes data type tag generation based on MV memory Address and the circuitry placing the tags in the CRT-FIFO. This block has provisions for scan line replication by repeating the MV address generated on the previous scan line of the MV window (only).

As Cinepak needs 4:1:1 rectangular format the MV Memory Address Counter needs to count in a non sequential way:

Y0Sn Y1Sn Y2S(n+1) Y3S(n+1) U V

implies an address counter that can skip over two numbers, or maybe **a second address counter that starts counting from 2 instead of zero.**

- **One tag bit is generated based on CRT Address and is 1 if the data in the CRT FIFO is from the MVW, other-wise is 0.** This tag bit, called the **steering bit** will be delayed through the entire data path and end up controlling the final video data mux just before the DAC.

Other tag bits called "data-type" tag bits encode the type of 32bit word in a given data format and are used by MVW Decoder/Serialiser to steer CRT-FIFO data at CRT-FIFO read.

For instance, in 4:1:1 linear data format, data is stored in memory and in the CRT-FIFO as Y0Y1Y2Y3 U03V03Y4Y5 Y6Y7 U47V47, 3 groups of 32bits. Two "data-type tag bits will mark the three types of 32bit words so that steering logic knows where to place the three words in the data serialiser.

Similarly Sashapak will need 3 "data-type" tag bits to encode 8 32bit words (for 6bit per U/L) or 4 "data-type" tag bits to encode 10 32 bit words (for 8 bits per U/L).

16bit RGB 5:6:5 and 5:5:5 and 8bit RGB 3:3:2 can either use the **standard VGA data**

path, which in 5428 was extended to 16bit wide (used for 16bit/pel 1kx768 interlaced) or the new data path, **if a phisically new data path will be actually created**

- **MV Data Path .** This is area wise the largest piece. It consists of a new 16bit wide data-path with the same delay as the VGA data path, that takes MV data from the MV prefetch cache and the CRT FIFO, treats it appropriately depending on the MV data format encoded in the MV tags and converts it to 24 bit YUV first and 24bit RGB second. Horizontal zoom with avaraging (or maybe 5 levels of interpolation) is in this block too

- **Larger (26 or 24 stages) CRT-FIFO, Variable CRT-FIFO threshold and its control.** Because the MS Windows pixel depth and MVW pixel depth don't match, it is necessary to reserve CRT-FIFO space to fill in enough high pixel depth data before the MVW display starts. In Sashapak this means 10 or 8W (for 8 or 6bits per U/L respectively).

This function can be implemented as a dinamic threshold size modification of the CRT-FIFO. If the CRT-FIFO has 24 stages instead of 16 but only 16 stages are used before the MVW but it is switched to 24 when MVW fetches start, there will be 8 more stages to fill at that time ensuring more prefetched data in the CRT-FIFO at the beginning of each MVW scan-line.

In normal operation the threshold is 8 (or 6).

Here is the sequence of events that follow the detection of MVW start:

1. **Drop CRT-FIFO threshold to 1 to get immediat service & make 10 (or 8) more stages available in the CRT-FIFO.**
2. **Start fetching MVW data till CRT-FIFO is full. (BLT in progress will increase latency)**
3. **Increase threshold to 10.**
4. **Proceed as such till end MVW.**
5. **Load the CRT Address Counter with its last contents + SAdOf**

(where SAdOf = Surrounding Address Offset)

7. **Continue fetching based on the new address (start with random cycle). CRT-FIFO threshold remains the same - at least 10 or 8. CRT-FIFO size is still 26 or 24.**
8. **At the end of line, upon flushing the CRT-FIFO before prefetch, decrease CRT-FIFO size back to 16 keeping the threshold the same.**
9. **Go back to #1 for the next scan-line.**

This sequence is applied if MVW pixel depth is higher than surrounding pixel depth. If MVW pixel depth is lower than surrounding pixel depth, then the action described at #1 above takes place at the end of MVW, instead of the beginning. ***In other words, FIFO depth extension takes place when a switch from low to high pixel depth occurs.*** **If MVW pixel depth is the same as the surrounding, only the address is switched. In this case the CRT FIFO depth and the threshold remain the same.**

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- Steering logic decode the tags comming out of the special addition to the CRT-FIFO and the pre-fetch buffer and controls the decompression, formatting and serialization.

(they tell the formatter what data is Y, U or V)

- What about the video serializer load and the CRT FIFO read signal? What hapens to them when in MVW? They are one signal today.
WHEN the data path switched to display MVW data, what hapens with the VGA Video Data Path is don't care as we do not display that data, except for the h/w cursor anf the h/w icon that do not go through the standard VGA serializer. So we'll probably stop the VGA data path untill the point h/w cursor and h/w icon are combined into it, to save power, as we will stop the MVW data path when not in use, for the same reason.
So, the Video Serializer Load may be stopped while MVW data is displayed, **but the CRT FIFO read will be going on, with a frequency and shape depending on the data format loaded in the CRT FIFO for display.**
In RGB 3:3:2 8bit/pel direct color mode CRT-FIFO read will be generated every 4 vclks.
In standard RGB 5:5:5 or 5:6:5 16bit/pel modes CRT-FIFO read will be generated every two vclks.
In YUV 4:2:2 24bit/pel (Y0 U Y1 V on one scan line) the CRT-FIFO read will be generated also every two vclks.
IN Sashapak 10 (for 8bit per U/L) or 8 (for 6bit per U/L) CRT-FIFO read pulses will be generated every 32 vclks.
- The MVW Address Counter, loaded at the beginning of each MVW scan-line with a start address calculated based on the Start MVW Address and the MVW Address Offset, will count at format dependent rate for as long as the CRT-FIFO is not full. Because the CRT-FIFO will be emptied faster in the MVW (in general the pixel depth will be higher in the MVW) there will be requests for more memory cycles when displaying in the MVW

- If either h/w cursor or h/w icon are on, they should be displayed even if the direct data path is used. In this case both video data pathes will clock and the steer tag will point to the VGA data path when either h/w cursor or h/w icon or both are displayed, even on top of a MV window. Please note that neither the h/w cursor, nor the h/w icon data go through the CRT FIFO or the VGA Data path except for the final pixel address block and the RAMDAC RAM, though they have a special path in the RAM. So we could stop most of VGA data path (including the internal palette) but not all of it even if we are in 16bit/pel mode (the new one that goes through a separate 16bit data path).

- If we are in a 16bit/pel mode with no h/w cursor or h/w icon, or in a 640x480 MVW mode filling the screen, we can stop the VGA data path to save power.

- The off-screen MVW memory will be a programable start memory array normally placed towards the end of the memory, but before h/w cursor, h/w icon and the half frame buffer, even the color one. The start of the MVW memory will be programable in increments of 4KW (16KB) as a physical address -> 7bits to program.

CR3B[6:0] is the MVW Memory Array Start Address.

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2MB configuration will support enough memory to support:
- one 640x480 3bit/pel window or up to two 320x240 3bit/pel (Sashapak) -> 32KW
- one 640x480 16bit/pel window or two 320x240 16bit/pel windows

(153.6KW=614.4kB out of 256KW or 512KW available depending on the memory con-

figuration).

- all of the above at the same time up to a total of two windows though

1MB configuration will support:

- one 640x480 3bit/pel Sashapak window or two 320x240 Sashapak windows or
- two 320x240 16bit/pel windows.

Please note that about 24KW are needed for 800x600 DS Color STN HFB, the h/w cursors and h/w icons while about 18KW are needed for 640x480 DS Color STN HFB and that

- 640x480 4bit/pel requires 38.4KW
- 800x600 4bit/pel requires 60KW
- 1024x768 4bit/pel requires 98.3KW
- 640x480 8bit/pel requires 76.8KW
- 800x600 8bit/pel requires 120KW
- 1024x768 8bit/pel requires 196.608KW

Video Motion Formats supported are:

- 8bit RGB 3:3:2 going through the palette (RGB 3:3:2)
- 16bit RGB (5:5:5 Sierra and 5:6:5 XGA) not going through the palette -> this is a 16bit/pel that does not require double dotclock !!
- 4:1:1 array converted to 4:2:2 Y0 Y1 Y2 Y3 U V -> Y0UY1V Y2UY3V for Cinepak (with Y2Y3 for the next scan line)
- 4:2:2 linear Y0UY1V from TV Decoder
- Sashapak format (we'll support only 6bit/pel)
  - for 8bit per U/L:
    4W (YU/L) + 4W (UV U/L) + 1W (YM) + 1W (UVM)=10W=40B
    --> 40B/32pixels=320bit/32pixels=10bit/pel to fetch from memory
  - for 6bit per U/L:
    3W (YU/L) + 3W (UV U/L) + 1W (YM) + 1W (UVM)= 8W=32B
    --> 32B/32pixels = 8bit/pixel

CR3C[3:0] will encode the pixel format for the first motion video window data:

0h = 0000 = 8bit RGB 3:3:2 going through the palette
1h = 0001 = 16bit RGB Sierra (5:5:5)
2h = 0010 = 16bit RGB XGA (5:6:5)
3h = 0011 = 4:2:2 YUV Y0UY1V
4h = 0100 = 4:1:1 YUV linear Y0Y1Y2Y3UV
5h = 0101 = 4:1:1 YUV array Y0Y1Y2Y3UV but Y2Y3 are in next scan line
6h = 0101 = Sashapak 6bits for U/L
7h = 0110 = Sashapak 8bits for U/L
8h:Fh = 0111:1111 = reserved

CR3C[4] = Enable Motion Video Window
CR3C[5] = Enable Live Video in Full Screen
CR3C[7] = MVW horizontal zoom (doubling)
CR3C[6] = MVW vertical zoom (doubling)

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Note: We will not support 4:1:1 linear from TV decoder, for design simplicity

Memory data formats:
- 8bit and 16bit RGB, as in 5428.
- 4:1:1 Cinepak converted to 4:2:2 by writing a 4:2:2 Code-Book
first scan line -> Y0UY1V -> One 32bit Word
---
second scan line in memory -> Y2UY3V -> One 32bit Word
- 4:2:2 linear will be mapped in memory as follows:
first scan line Y0UY1V
first scan line Y2UY3V
---
consecutive data in the same scan line.

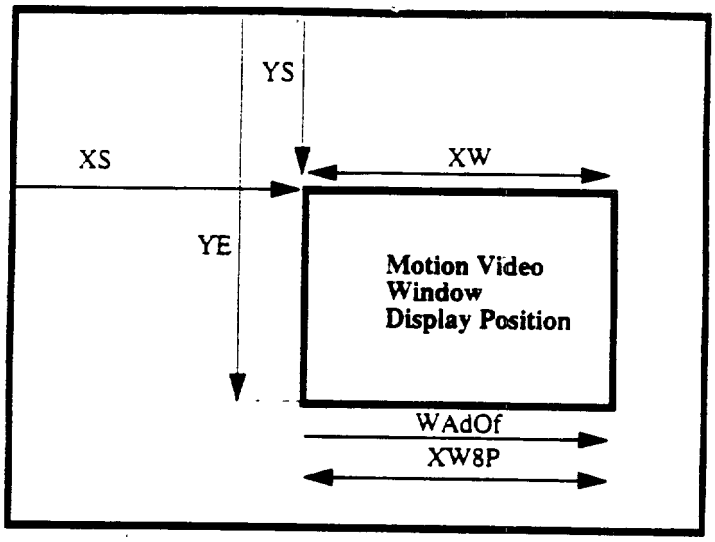
The tags that accompany the motion video data through the CRT-FIFO mark both the data format and the type of data inside the format (U/L for Y or U,V or mask for Y or U,V in Sashapak, Y0, Y1,U or V in 4:2:2).

Double Buffering for MVW Video Memory Data

In order to get a high quality Live Video full frames should be displayed at all times. This assumes that writing the video buffer and displaying it are in sync, which is normally not the case..
To solve this problem and provide a simple interface between MVA h/w and the driver. Nordic will support a double buffer approach.

Addressing with Sashapack:
Sashapack stores data for eight scan-lines in one memory page (works only with synchronous DRAM-s). But due to U,V sub-sampling diferent data types are not read from memory uniformly.
On Y U/L the first four scan-lines read at offset 0 in the page, but the second four scan-lines read at offset 50H in the page.
On U,V U/L we read the same data for each scan-line. So we repeat reading the same data at all times, for eight scan-lines. Page addresses to read are A0:EF. If the scan-line is shorter it will end sooner.
On Y Map the data should be sequential, scan-line oriented: first pixels 0 to 639 on the first scan line, than pixels 0 to 639 on the second scan line and so on till the 8-th scan line. If the lines have less than 640 pixels, Sasha wants them cropped for the first 4 scan lines, and then starting again from the half for the next four scan-lines. This is in sync with Y U/L where the last four scan-lines start from mid.
On U,V Map, because of the vertical subsampling, the same data is read for two scan lines, so there are four scan-lines worth of data but each scan-line is read for two consecutive scan-lines. Even if the scan-line is shorter, there will be a gap every-scan-line: there are fix page addresses for each scan-line up to 640 pixels wide.

Full Screen in a given graphics mode



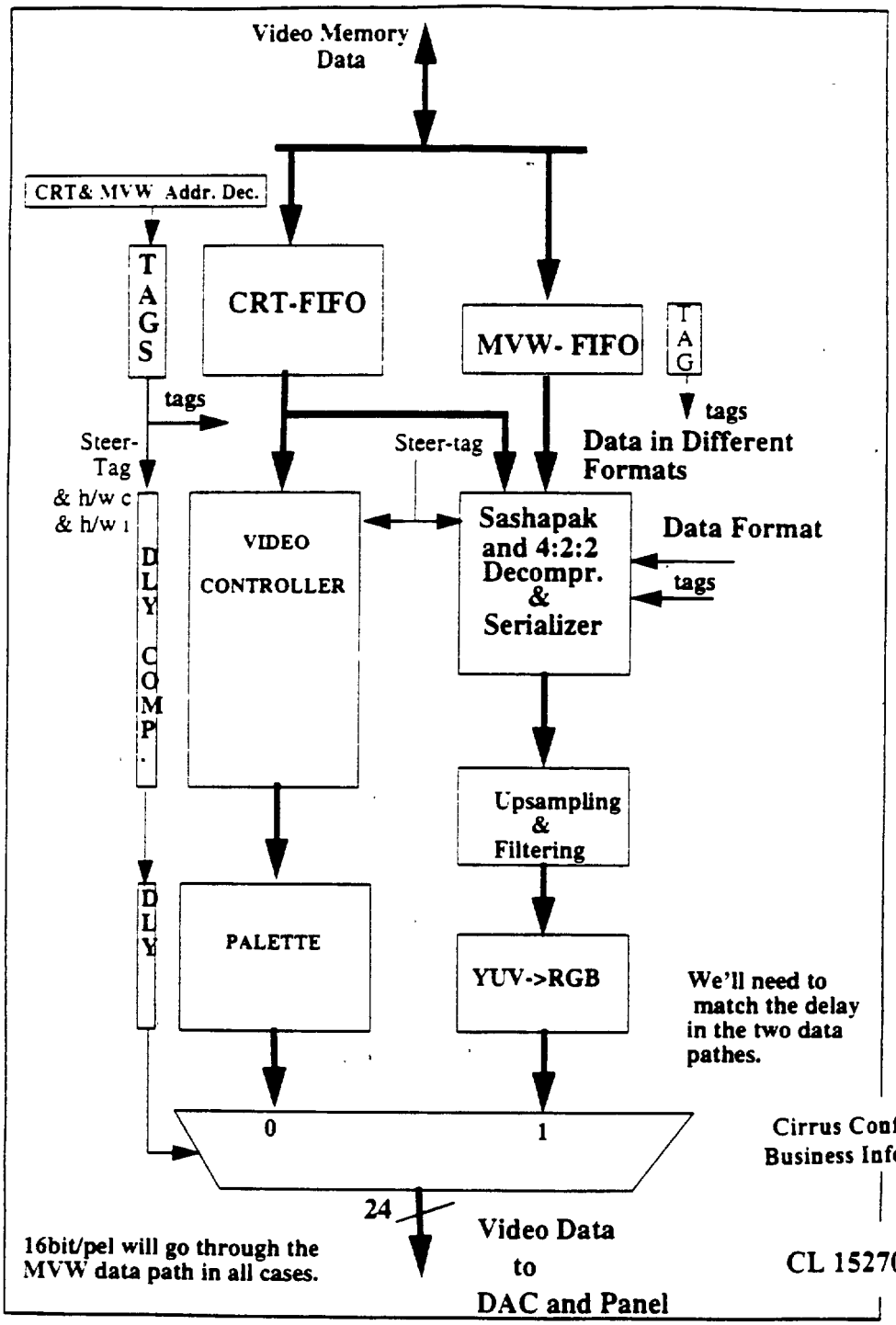
Where:

- **XS** = MVW Horizontal Start Coordinate (in surrounding pel depth memory cycles)
- **XW** = MVW Horizontal Width (MVW pel depth memory cycles)
- **YS** = Vertical MVW Start (in true scan-lines not affected by scan-line doubling or panel vertical expansion)
- **YE** = Vertical MVW End (all bits are programmed, in true scan lines)
- **WAdOf** = MVW Address Offset (a number to be added every line to the CRT Address Counter to allow it to jump over the MVW without counting through it.
- XW8P = MVW horizontal width expressed in 8 pixel units

Please note that MVW horizontal width is defined twice in different units:
XW defines it on the memory side in memory cycles
XW8P defines it on the CRT side in 8 pixel units.

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Video Memory Data
CRT& MVW Addr. Dec.
TAGS
CRT-FIFO
MVW- FIFO
TAG
tags
tags
Steer-Tag
& h/w c
& h/w 1
Steer-tag
Data in Different Formats
DLY COMP.
VIDEO CONTROLLER
Sashapak and 4:2:2 Decompr. & Serializer
Data Format
tags
Upsampling & Filtering
DLY
PALETTE
YUV->RGB
We'll need to match the delay in the two data pathes.
0
1
24
Video Data to DAC and Panel
16bit/pel will go through the MVW data path in all cases.
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4.5 Feature Connector Support

Nordic-1M will support 5428 Feature Connector so that it is compatible to Media Manager
Nordic-1M will support VAFC (Vesa Advanced Feature Connector) in the 8bit VSVPC passthrough compatibility mode.
The main difference beteen 5428 FC and Nordic FC is the fact that 5428 FC has one EDCLKn control pin controlling the direction of the DCLK pin, while Nordic-1M as well as VAFC have a FCDCLK output pin and a FCVCLK input pin.
Dave Keene believes that 5428 FC is VAFC compatible. To ease the design, I kept 5428 FC pin names (not VAFC pin names).
<u>On VAFC compatibility</u> here are some comments:
- GENCLK can be applied on XVCLK if SR22[3]=1.
But, if SR22[3]=1 (select xclk) & SR24[7]=1 (VAFC enabled), then XMCLK should get OSC and MCLK Synthesizer operates normally, except that the reference frequency comes from XMCLK instead of OSC pin. If SR22[3]=1 & SR24[7]=0, then MCLK comes directly from XMCLK pin and the MCLK and VCLK Synthesizers are powered-down !!
- GRDY signal is similar to OVRW.
- VRDY is similar to EVIDEO if EVIDEO is dinamically switched as a valid data in signal.
- EGENn is not needed if we configure Nordic-1M in the right configuration with SR22[3] (XCLKPU) and SR24[7] (VAFCPU).
- As VAFC maximum FCVCLK frequency is 37.5MHz, VAFC supports a mode in which data is sent at 37.5MHz to the DAC and it each pixel will be displayed twice if the chip is running at 75MHz pixel clock. This allows only 8bit/pel data to be displayed. To display 16bit/pel data we should use both phases of the FCVCLK and pack the data into one pixel. I think that this is already done in 5428, if not Man-Shek and Fong-Jim are modifiying the 5429 RAMDAC to support this mode -> we need to support it too.
- VAFC requires FCDCLK to be switchable under s/w control beteen 1x and 1/2x the pixel clock. If we took this out of Nordic-1M data base, we should put it back, but the divide by two should affect only FCDCLK going out of the chip.

Check VESA VAFC Proposal 1.0p rev. 0.31 07/15/93 for VAFC timing info.

<u>**Nordic-1M FC Pins Functional Description**</u>

Most of this is from 542X Data Sheet page 3-26:

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VSYNC and HSYNC	TO	The standard CRT pins tri-stated when FCESYNCn is L. Thes pins have programable polarity.
FCBLANKn	I/O	BLANKn in 5428. If FCESYNCn is H, this is an output and it supplies the actual composite BLANKn CRTC signal. VAFC requires this to be the composite Display Enable (no borders). If this is the case, we'll need a bit for VAFC that puts DE = HDE & VDE inverted on BLANKn.

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If FCESYNCn is L, FCBLANKn is an input and it forces RAMDAC RAM outputs to 0 (black), but it should force them black before they go to the panel.

It seems that by connecting OVRW output to BLANKn as input we can display FC data in a window - this will work though only if OVRW, internally controls the pixel address mux between normal VGA data and the FC data.

FCP[7:0] I/O P[7:0] in 5428.
If FCEVIDEOn is H, these pins are outputs and represent the pixel address of the RAMDAC
IF FCEVIDEOn is L, these pins are inputs and represent the pixel address to the RAMDAC.
CR1A[3:2] control the way the FCP[7:0] are muxed with the normal data.

FCDCLK O (the actual pin is I/O) outputs VCLK or VCLK/2 if selected through s/w

FCESYNCn I ESYNCn in 5428. Controls HSYNC, VSYNC and FCBLANKn (H-> outputs, L-> H/VSYNC are tri-stated, FCBLANKn is tri-stated.).

Nordic does not have EDCLKn input as FCDCLK and FCVCLK are not shared.

OVRW O OVRW in 5428 = Overlay Window. **This active Low** signal, is generated by the BLANKn VT and HT logic (shared) and is supposed to be used to create an Overlay Window in which data from the Feature Connector is displayed. *I don't know why we output this signal. It should be controlling the MUX between the normal pixel address and the FC originated pixel address.*

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4.5.1 On the Video Port for TFT Panels

A Video Overlay live video solution requires a TV Decoder Chip Set, a de-interlacer (at least a line buffer, but usually a full frame buffer), a scalar/filter/color converter chip (like CL-PX0072, CL-PX0070 or the more expensive CL-PX2070). To display live video in a window at 800x600 or 1024x768 a full frame buffer is needed and some frame level synchronization needs to be achieved.

Is there a cheap way to display full screen TV on a 640x480 panel?
Is a video port a cheap system solution to the above problem?

Can we design a system that uses a universal TV Decoder like SAA7151A and feeds data directly to a Video Port that displays live video at 640x480 30fps with no additional components? This is what customers require!

Problems to solve:

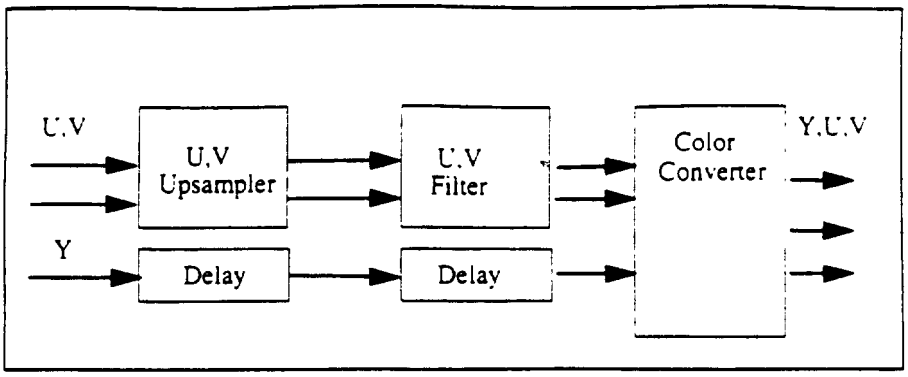
1. Accept 7151 data format: 4:2:2 YUV at 6.75MHz or 4:1:1 YUV at 3.375MHz, interlaced.
2. Synchronize at frame level.
3 De-interlace. Optionally display only odd fields with scan line doubling (according to Sasha this looks better than displaying true de-interlaced picture).
4. Get enough memory bandwidth with a 32bit wide DRAM.
5. Have enough storage space on the Graphics Controller to go over the CRT horizontal non-display memory refresh & prefetch time while Live Video Data comes at normal TV display speed.

4.5.1.1 Data Format

In order to accept YUV data, we need good up-sampling filters on U and V After up-sampling and filtering we need a Color Space Converter with 2-th complement (for 7151) or excess 128 (for other TV decoders). A good 4:1:1 UV up-sampling filter is quite complex and requires many stages of pipe-lining (9 or 11) . A good 4:2:2 UV up-sampling filter requires less than 5 stages of pipe-lining.
As data is stored in TV decoder format, up-sampling, filtering and color conversion are done on the CRT read side at dot-clock rate.
Please note that 4:1:1 data requires 48 bits of storage (two data packs will fill 3 32 bit words).

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4.5.1.2 Synchronize at Frame Level

To avoid moving objects jagging we should display only full frames. In many systems today this requirement is not met. For instance play-back systems display as fast as possible without any regard for frame synchronization. According to Sasha this is not good for TV. How bad it is remains to be seen.
If the CRT/TFT display runs at 27MHz (double TV dot-clock rate) it is possible to use a double buffer scheme in which we display twice each frame while writing one TV frame in the other video buffer and alternate the two buffers. For a 640x480 display at 4:2:2 YUV we'd need 2MB of DRAM, as the buffers are embedded in the Video Memory (614.4KB per buffer needed).
Even with this scheme, external VSYNC from the TV Encoder should be used to synchronize (= reset) Nordic vertical counter, so that TV and Graphics frames start at the same time. SAA7151 outputs VS (TV VSYNC) which can be used as external SYNC by Nordic.
If only odd fields are displayed, half data is stored reducing Video Memory requirements to 307KB per frame (614KB total which fits in 1MB). This is not a bad idea especially if the picture looks better!

4.5.1.3 De-interlace

This is naturally done by writing data in the Video Memory. If only odd fields are displayed, Nordic has to determine the field boundary by counting HS (TV HSYNC) pulses.

4.5.1.4 Memory Bandwidth with 32bit Wide DRAM

There are two cases: 4:2:2 YUV and 4:1:1 YUV.

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A. 4:2:2 YUV Bandwidth Requirements

CRT-dot-clock frequency = 27MHz, TV-clock frequency = 13.5MHz
R=6m, P=2m

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a. TV-FIFO = 16 stages with 8 to write 8 to read .

CRT-FIFO = 16 stages with 8 to write and 8 to read
2xCRT-FIFO-fills + TV-FIFO-empty < 2x16 CRT-dotclks=16 TV-dotclks=1185ns
2x(R+7P) + R+7P + 3m = 3R+21P+3m=18m+42m+3m = 63m < 1185ns
mclk-period < 1185ns/63 = 18.8ns -> 53MHz min mclk frequency

b. TV-FIFO = 32 stages with 16 to write and 16 to read
CRT-FIFO = 16 stages with 8 to write and 8 to read
4xCRT-FIFO-fills + TV-FIFO-empty < 4x16 CRT-dotclks=32 TV-dotclks=2370ns
4x(R+7P) + R+15P + 5m = 5R+43P+5m=30m+86m+5m = 121m < 2370ns
mclk-period < 2370ns/121 = 19.58ns -> 51MHz min mclk frequency

c. CRT-FIFO = 32 stages 16 to write and 16 to read @ 27MHz
TV-FIFO = 16 stages 8 to write and 8 to read @ 13.5MHz

CRT-FIFO-fills + TV-FIFO-empty < 32 CRT-dotclks=16 TV-dotclks=1185ns
(R+15P) + R+7P + 2m = 2R+22P+2m=12m+44m+2m = 58m < 1185ns
mclk-period < 1185ns/58 = 20.43ns -> **48.9MHz min mclk frequency**

Please note that Nordic already has 32 (or 36 stages of CRT FIFO - MVA FIFO) and 24 stages of FB-FIFO (write + read). So if we use all the buffering area available we can meet case c requirements and run direct live video at 48.9MHz mclk.

d. CRT-FIFO = 24 stages (12/12)
TV-FIFO = 12 stages (6/6)
CRT-FIFO-fills + TV-FIFO-empty < 24 CRT-dotclks=12 TV-dotclks=888ns
(R+11P) + R+5P + 2m = 2R+16P+2m=12m+32m+2m = 46m < 888ns
mclk-period < 888ns/46 = 19.3ns -> 51.8MHz min mclk frequency

B. 4:1:1 YUV Bandwidth Requirements

a. CRT-FIFO = 24 stages (12/12)
TV-FIFO = 12 stages (6/6)
CRT-FIFO-fills + TV-FIFO-empty < 32 CRT-dotclks=16 TV-dotclks=1185ns
(R+11P) + R+5P + 2m = 2R+16P+2m=12m+32m+2m = 46m < 1185ns
mclk-period < 1185ns/46 = 25.7ns -> 38.8MHz min mclk frequency

Because 3x32bit house 8 pixel data, it is advisable that the number of stages in the FIFO-s are a multiple of 3 for 4:1:1.

For 4:1:1 YUV, the picture quality is not that good as for 4:2:2, the control requirements are harder to meet, the filter on U and V is expensive, but the bandwidth requirements are easy to meet.

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4.5.1.5 Covering the Memory Refresh and CRT-FIFO Prefetch Time

During each horizontal non-display time, Nordic executes memory refresh (normally 3 with an option of 1 - all random cycles), h/w icon and CRT-FIFO prefetch cycles.

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At that time the TV data comes at normal rate and has to be stored in the TV-FIFO. Let's see how long it takes to execute all these cycles.

a. With reference to case A.c. 4.5.1.4
(4:2:2 YUV the case that meets bandwidth requirements at 48.9MHz mclk)

x. CRT-FIFO = 32 stages, 3 refreshes, h/w icon 64x64x2 (4 h/w icon cycles)
R+31P + 3R + R+3P + 3m = 5R+34P+3m=30m+68m+3m=101m < 1185ns
-> m < 1185ns/100m=11.7ns -> min mclk freq. is 85MHz
(off by about 42mclks to get to 50MHz mclk).

y. CRT-FIFO = 32 stages, 3 refreshes, h/w icon but prefetch 16 CRT-FIFO stages
(no need to fill the FIFO at the beginning of the line).
R+15P + 3R + R+3P + 3m = 5R+18P+3m=30m+36m+3m=69m < 1185ns
-> m < 1185ns/69m=17.17ns -> min mclk freq. is 58.2MHz

z. CRT-FIFO = 32 stages, 1 refresh, h/w icon but prefetch 16 CRT-FIFO stages
(no need to fill the FIFO at the beginning of the line & use extended refresh DRAMs).
R+15P + 1R + R+3P + 3m = 3R+18P+3m=18m+36m+3m=57m < 1185ns
-> m < 1185ns/57m=20.78ns -> **min mclk freq. is 48.1MHz**

This case meets the minimum requirements for non-display time buffering.

b. With reference to case B.a. 4.5.1.4
(4:1:1 YUV the case that meets bandwidth requirements at 38.8MHz mclk)

x. CRT-FIFO = 24 stages, 3 refreshes, h/w icon 64x64x2 (4 h/w icon cycles)
R+23P + 3R + R+3P + 3m = 5R+26P+3m=30m+52m+3m=85m < 1185ns
-> m < 1185ns/85m=13.9ns -> min mclk freq. is 71MHz
(off by about 26mclks to get to 50MHz mclk).

y. CRT-FIFO = 24 stages, 1 refreshes, h/w icon but prefetch 16 CRT-FIFO stages
(no need to fill the FIFO at the beginning of the line & extended refresh DRAMs).

R+11P + 1R + R+3P + 3m = 3R+14P+3m=18m+28m+3m=49m < 1185ns
-> m < 1185ns/49m=24.18ns -> **min mclk freq. is 41.3MHz**

Case b.y will do it for an mclk frequency above 41.3MHz.

Note: If required, we could disable the h/w Icon and h/w Cursor when in full screen live video from Video Port.

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Conclusion on Video Port Cheap System Solution

It is possible to achieve a minimum cost mother-board solution for full screen 640x480 30fps live video by interconnecting directly a digital TV decoder to Nordic Video Port under the following conditions:

1. **Prefetch only half CRT-FIFO instead of the entire FIFO**
2. **Do one refresh per line (eventually use extended refresh DRAMs)**
3. **To display 4:2:2 YUV use 32 CRT-FIFO stages and 16 TV-FIFO stages (between CRT-FIFO and MVA-Buffer we have enough storage now, but it has to be reconfigured). Minimum memory clock frequency is 48.9MHz**
4. **To display 4:1:1 YUV use 24 CRT-FIFO stages and 12 TV-FIFO stages. Minimum memory clock frequency is 41.3MHz.**

Under the same conditions, it is possible to display live video in a window with a 640x480 TFT panel, but the image has to be scaled-down and filtered with PX0070 or PX0072 - a more expensive solution. Also, during the actual live video display time, CPU and BLT will get very few cycles. This is not a factor with full screen live video as the CPU does not need to access the Video Memory at that time.

The question is now: how much cheaper is this solution relative to a full screen TV with overlay ? Sasha is working on a cheap solution with overlay.

Minutes of the Meeting on MM in Nordic in Nov. '93

With D.Keene. Keith. Del and Nordic Team on

- Video Port with 32bit memory is bwth. limitted. It is not a good solution for 32bit bus - better use Overlay or Sashapak.

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4.6 On WavePort Architecture and Audio Driver

Starting from Dave Keene's WavePort Specificauon. Rakesh. Sasha and Vlad came-up with some ideas which could greatly simplify the design work for WavePort. reducuon the complexity and the number of gates of the WavePort.
We'll start with the small issues and move towards more important issues

4.6.1 AUXS1 and AUXS2 Pin

A. Dave proposed to share this pin with PDN (Power Down) WavePort Pin and configure it as AUXS2 when using 4231S.
We nouced that 4231S does have a PDN pin which we'd like to use to save power
We'll put AUXS2 on another pin.

B. Dave proposed to have a fully programmable location for AUXS1 and AUXS2 CPU I/O map with a default at 530H and 388H. This is costly (4 registers and fast comparators) and very difficult to design at required speed: will slow down address range decode for I/O a lot affecting command to command parameters.
We suggest to have a fix address for these ports: 530H and 388H.
Two register bits (one per address) can disable the chip from answering to these I/O addresses.
If we are not sure where to place these ports, we can leave it as a metal option for future modification or have one more alternative for each, but the address should be fix for fast decode.
GR58:GR5B are no longer needed if this option is accepted. We'll need two bits to disable 530H and 388H address decode and eventually two other bits to select other two alternate I/O addresses. We should always decode 16 addresses: 530:53F and 388:397 (not 4 or 16).

4.6.2 WavePort R/W Buffer Location and Size

To simplify the h/w and reduce verification work-load , WavePort R/W Buffer Size should be fix: 32KB for each, enough for at least 180msec of operation -> 90msec for half buffer. Every 90msec the CPU will have to fill and/or empty half Audio Buffer (write or read respectively).
It is also possible to place the WavePort memory buffer in a fix memory location, common for both desktop and portable architectures. We could place it in Memory in the upper part
(in high address area), just before the h/w cursor. If the h/w cursor takes the upper 16KB of the memory, we could use the next 64KB for the WavePort buffer.
Going down in memory, in Nordic we'd place the h/w icon in the next 16KB (only 4KB needed now... but leave some room for expansion) and the Half Frame Buffer for monochrome and color panels in the next 32KB and 96KB respectively.

Total:

96KB for CRT/TFT/SS STN panels,
128KB for monochrome panels and
192KB for dual scan color STN panels.
out of 1MB or 2MB memory available.

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When the memory is expanded, all these fix components should move automatically in the upper side (towards the end of memory).

This places the WavePort buffer at:

- **for 1MB** of memory by 32 (256Kx32 -> 00000:3FFFF) **3B000:3EFFF**
- **for 2MB** of memory by 32 (512Kx32 -> 00000:7FFFF) **7B000:7EFFF**

If we adopt this solution, GR43 is not needed.

4.6.3 On Host Access to WavePort Buffer

In order to ensure independence between the Graphics s/w Driver and the Audio Driver, taking into account AVGA limitation of no CPU accesses during BLT operation, Dave proposed a separate path for WavePort Host Accesses. This involves a separate 4 stage by 32bit write and read buffer and separate arbitration for the Audio cycles. The buffer is shared by WavePort read and write operations and an I/O to an extension register bit is needed in order to switch from a read operation to a write operation or vice-versa.
Dave also proposed that the host address be dependent on GR6 CPU address map bits such that the video and audio address maps don't overlap.
Please note that this approach prevents debug with a Hercules card when in graphics.

In the following an alternate scheme is proposed:
- There is one register bit that enables WavePort memory write accesses and one register bit that enables WavePort memory read accesses. When one of these bits is asserted ,the chip expects only host accesses for the WavePort: the host address will be automatically translated to a memory address inside the WavePort buffer. The access will be fully linear, 32bit only, **graphics mode independent** (like in extended 8bit/pel). The Graphics block will be forced to this mode and all planes will be automatically enabled. On the Host side, the WavePort buffer will be placed always at A000:0000 - A000:FFFF -> 64KB with 32KB for read buffer (the upper side) and 32KB for write buffer (the lower side of this 64KB segment).
- The CPU Data Path is the same as for any other CPU cycle: no special FIFO, no special arbitration are required. The Audio Driver and The Graphics Driver communicate through interrupts: There is an interrupt for BLT completed (Dave's idea when presented with this proposal) and an interrupt for Audio Buffer Full (or Audio Transfer Completed). When the BLT is completed, if Audio is enabled on the chip, the BLT Completed interrupt allows the Audio Driver to check if there is any need to service the Audio and vice-versa. If possible, the Graphics driver should restrict the extent of the BLT operations to less than 160msec or so (leaving at least 20msec to start filling the WavePort buffer).

- There is no on chip CPU WavePort address generation. The CPU address in the range A0000:AFFFF (incremented by 4 every cycle for DW accesses) is translated to physical memory address 3B000:3EFFF. If host side WavePort pointers are used, the host address is latched and translated for comparison with the Codec pointers generated on chip.

Adopting this scheme would greatly simplify the extent of the design and verification work for WavePort: 8 weeks at least will be saved.

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4.6.4 On the Audio Driver

Dave proposed that the Graphics Controller has h/w to compare the WavePort pointers and generate interrupts. The Codec pointers are I/O readable by the host as well as several buffer status bits (Audio-IN buffer Full, Audio-In buffer half-full, Audio-Out buffer half-empty, Audio-Out buffer empty,...).

Nordic-1M will support Dave's proposed interrupt driven interface.
In this case the only important difference for the driver will be that it will have to generate the buffers address and not rely on the h/w to do this (Dave suggests that CPU will write and read always the same address A000:0 or B000:0 and the actual address on the host side is generated on the chip - we sugest to change this and let CPU generate the address)

Because CPU has to wait untill the a BLT operation is complete and the BLT has to wait for Audio buffer to be full or the transfer completed, two more interrupts are needed: BLT operation completed and Audio transfer completed. This way the Audio Driver and the Video driver can communicate with each other.

The Read and Write CPU side pointers will be generated by latching the last read and write WavePort CPU address (lower 16bits only) after translation to physical memory address. Comparators on the host and codec pointers will generate Buffer Full and Buffer Empty signals.

Jeff Ort drew our attention to the fact that the driver transfers a certain size block and needs an interrupt anytime half of what was placed in the Audio buffer was read by the Codec (the play-back buffer is half empty). To make things simple for the h/w, we propose to give Jeff an interrupt when the CODEC side playback buffer read pointer reached a preprogrammed value, value the driver programs everytime it transfers a block of a certain size in the playback buffer. For instance, if the driver put 2KB of data in the playback buffer starting from phisical address 3B000 (host address A000:0) and wants on interrupt when the first 1KB was read by the CODEC, it should program 3B0FF in the playback interrupt register, as 1KB = 256 32bit words. The register will have 16bits and the driver will program B0FF to get an interrupt when the CODEC reads 3B0FF or 7B0FF playback buffer address.

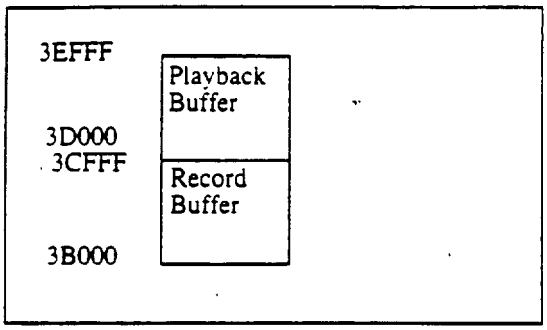
Similarly, on the record side, there will be a programable interrupt on the CODEC side to be used to tell the driver when the Record buffer is half full.
So we'll need two 16bit indexed registers for these programable interrupts. For each WavePort interrupt we also need a status bit to say that the interrupt happened, an enable bit to enable the particular interrupt. As Dave proposed, GR4D is the Interrupt Status register but bits [0] and [2] will be the programable interrupts status bits. The interrupts and the status bits will be cleared after this register is read (automatic clear in h/w).

We could use registers GR58:5B as high and low byte for the programable interrupt

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on Record and Play-back buffers respectively.



The write-buffer (or Audio-Out =the one in which the CPU writes) is empty one WavePort write cycle to memory after

WRBUF-Write-Pointer = WRBUF-Read-Pointer+1

(this condition will activate set an empty flag).

The write-buffer is full one WavePort write cycle to memory after

WRBUF-Read-Pointer = WRBUF-Write-Pointer + 1

The same equations apply to the WavePort read-buffer, only this time the read-pointer is on the host side and the write-pointer on the Codec side.

Shouldn't be a Audio-Out buffer full interrupt and a status bit for it?

Threshold detect mechanism will require to increment host pointers, but the CPU is supposed to read this pointer and generate the proper address when going above the threshold The idea of the threshold detector is that by incrementing the Audio-In read pointer everytime the write pinter is incremented if the Audio data is under the threshold value, the delta between the pointer remains the same and the buffer does not fill in with sub-threshold value. This was true if the half-full detection had been generated based on the delta between pointers. After talking to Dave, there are some clarifications to be made on the threshold detect mechanism for record:

For one record sesion, this is a one time event mechanism: if the threshold was passed once after being enabled, its effect is lost - even if the sound level goes below the threshold the record buffer read pointer works normally. The threshold will help only in the initial stage before the first actual voice pattern is detected, but it does not have any effect after the intitial triggering event - once the sound leved passed once the threshold.

With this driver approach, GR43 and GR58:5B will not be needed.

Five registers are saved. Twenty One register are still needed (plus two reserved = 23).

Another possible approach for the driver uses extensively the Vertical Interrupt:

In this case every Vertical Interrupt, the Audio Driver reads the Codec side pointers, compares them with the Host side pointers, the driver generates based on the CPU address it last wrote to or read from and makes its own decisions. The driver will also check the BLT completed status bit.

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In other words, every 18msec (@60Hz), on the Vertical Interrupt the Audio driver can process data from the Codec pointers, calculate based on the last address if the WavePort buffer is full or empty and decide how many more WavePort accesses to execute. As at least 180msec worth of data is in a full Waveport Buffer, the driver has 6 opportunities to find out that the buffer is empty and start filling it before half WavePort buffer is empty.
On chip h/w is still needed to stop sending data to the Codec after sending all data and to read all data from the WavePort read memory buffer on the host side. Because the CPU decides when the buffers are full, half full or empty there is no need for registers for the pointers on the CPU side, but the CPU address will still be latched to generate the host side pointers.
The "BLT operation completed" and the "Audio transfer completed" interrupts are needed anyway bacuse we share the data-path for BLT and CPU cycles.

By adopting this mechanism in the driver, no special h/w is needed to preserve pointers on the Host side, to compare the Host side pointers (read and write) with the Codec pointers and to generate interrupts and status bits. The only interrupts needed are Standard VGA Vertical Interrupt as a time base, BLT completed Interrupt and Audio Completed interrupt.

We can still implement the threshold detect.

GR44,GR45, GR48 and GR49 won't be needed.
Nine registers are saved. Seventeen register are still needed (19 with two reserved registers).

Conclusion
The above proposal, if OK for the WavePort driver, would reduce significantly the amount of design and verification work on the WavePort. This document was written in order to get feedback and reach an agreement ASAP. Our goal is to have a unique s/w model for the WavePort, but we'd like to cut the amount of work if possible.

Rakesh's notes on the discussion with Jeff Ort and Dave Keene, 11/03/93

1. Since in Nordic, we do only 1R + 1P always, what happens if the bit is disabled for the host read at a time when ODD number of FIFO stages are filled? At Present we assume that while recording some SILENCE is inserted at the end of recording session and thus we can disable the bit as soon as driver disable it.
Jeff and Dave Kenne both agree that even though no SILENCE is inserted at the end, it is still valid to disable the memory transfer immediately after the bit is negated.

2. Threshold Issue.
If threshold mechanism is enabled, we keep putting the samples into the AUDIO BUFFER.
If the data in buffer is more than the programmed value (GR74 and GR75) and input data crosses the threshold value, the interrupt is generated immediately. But if data amount is less than the

value in the registers GR74-GR75 and input data has crossed the threshold value then we wait till it crooses this value(GR74 and GR75) and then interrupt is generated.

Dave's specs talk about two pointers on the RECORD buffer, one for the CPU read and
another for CODEC write. Both of these pointers are accessable by the CPU in his specs So he suggests that before the threshold is met we should fill up the buffer till half full condition. Once the buffer is half full, any more writes to RECORD buffer by the CODEC should increment both of these pointers. In this case whenever the threshold is met we are guaranteed to have some information about the history of audio samples just before the threshold is met. At the time when threshold is met the generated interrupt should tell CPU that CPU can read the data from the location pointed to by CPU read pointer.

But in NORDIC, the CPU read pointer is not accessible by CPU. Thus we keep putting the samples in the RECORD buffer and not generate the interrupt till the threshold is met even though we might pass the programmed value for the interrupt. At the time when the threshold is met, the interrupt is generated if CODEC write pointer is past programmed number. If threshold is met before the CODEC write pointer passes the programmed number, we wait till it does cross the programmed number. So the driver for Nordic should store the CPU address at the time when the threshold mechanism is enabled. So at the time of interrupt CPU can calculate the amount of samples in the BUFFER.

3. Independent control for IN / OUT mono / stereo .

Codec read and write are independently controllable for mono or stereo input / output.

4. Jeff agrees with the usage of OFFSET register GR9 to generate the CPU side adress for audio, instead of NORDIC generating the adress automatically.

Minutes of 11/20/93 Meeting with Keith, Del and Dave Keene

1. We need to check if WavePort accesses work with linear addressing (SR7 - aperture register).
2. Make sure that OverRun Status is there even if OverRun Interupt is disabled.
3. Enable looking for threshold only after you reach the given address.
4. Bit GR6E[6] should move to GR6E[3].
5. Talk about programable address for AUX1 and 2.
6. Check out arbitration for audio throughly.
7. Check overrun interrupt during threshold... always programmed interrupt after crossing threshold. ?? Rakesh may understand this!!

4.6.5 Registers specs for the AUDIO of NORDIC1-M.

GR60 Wave Port Control 1

7 Reserved
6. Reserved
5. Enable audio for host accesses.
4. Select 4215
3. Stereo for reciever (i:e STEREO CODEC)
2. Stereo for transmitter (i:e STEREO NORDIC)
1.0 Data Format select
    00 16 bit
    01 8 bit
    10 4 bit
    11 reserved.

GR61 Waveport control 2

7. Reserved
6. powerdown control ---> 0 will force low on PDN.
5. Enable command mode. 4215 must have been placed in COMMAND mode by forcing
    low on D/C* pin.
4. input level in SDI in command mode.
3. output level on SDO in command mode.
2. output level on SCLK in command mode.
1. output level on FSYNC in command mode.
0 output state of D/C* pin.

GR62 Input Audio Threshold setting.

7:0 Available only for 16bit mode. Only +ve data is compared i:e if msb of left data is 1 no compare is performed.

GR65

7. Enable Threshold detect mode.
6:0 Reserved

GR66 7:0 Audio Input Codec write pointer low byte

GR67 Audio Input Codec write pointer high byte

7. Enable input from codec to audio buffer.
6:0 Audio Input Codec write pointer (low 7 bits of 15 bit pointer)

GR6A 7:0 Audio Output Codec Read pointer low byte

GR6B Audio Output Codec Read pointer high byte

7 Enable output to codec from audio buffer.
6:0 Audio Output Codec read pointer (low 7 bits of 15 bit pointer).

GR6C : Interrupt Control.

7:6 Reserved.
5 Standard VGA Interrupt disable.
    0 --> Allow VGA interrupt
    1 --> Disable VGA interrupt.
4:2 Reserved.

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1 Audio Input interrupt control -----> DURING RECORD SESSION
0 --> disable this interrupt source.
1 --> Enable input buffer full OR programmed full interrupts.

0 Audio Output interrupt control -----> DURING PLAY SESSION
0 --> disable this interrupt source.
1 --> Enable Output buffer empty OR programmed empty interrupts.

GR6D : Interrupt Status.

Indicates any active enabled interrupt. Reading this register will clear the interrupt state and reset the status. No effect on the standard VGA interrupt status or interrupt.

For All of the following 1 in the bit means PENDING INTERRUPT.

7:6 Reserved.
5. Standard VGA Vsync interrupt (state of 3C2(7)).
4. Reserved.
3. Record Buffer FULL (OVERRUN).
2. Record Buffer PROGRAMMED FULL.
1. Play Buffer EMPTY. (UNDERRUN)
0. Play Buffer PROGRAMMED EMPTY.

GR6E : AUX1 and AUX2 control

7. Enable Aux Sel 1 low-true output on adress match 530-53Fh.
6. Enable Aux Sel 2 low-true output on adress match 388-397h.
5:0 Reserved.

GR6F: Code status.

7:4 Reserved
3 Timer status (ADI) time slot 6 bit 7
2. overrange (OVR) time slot 7 bit5
1. PIO1 input status. time slot 7 bit 7
0. PIO0 input status. time slot 7 bit 6

GR70: Codec control DWORD from Nordic to codec. byte D7:0
GR71: Codec control DWORD from Nordic to codec. byte D15:8
GR72: Codec control DWORD from Nordic to codec. byte D23:16
GR73: Codec control DWORD from Nordic to codec. byte D31:24

GR74:75 Interrupt value for audio IN buffer.

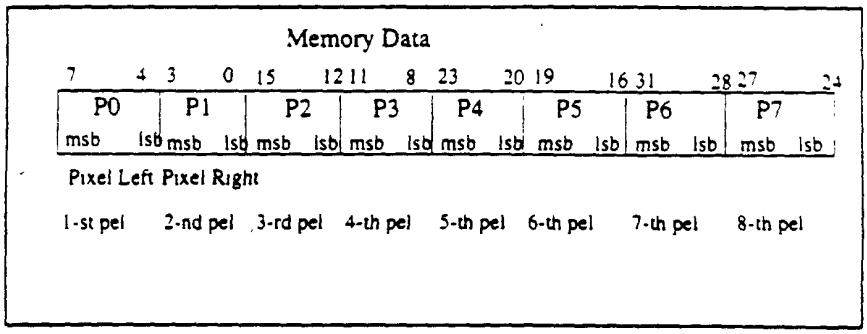
When CODEC reaches the programmed adress -1, an interrupt is generated during the record session.

GR76:77 Interrupt value for audio OUT buffer.

When CODEC read pointer reaches the programmed adress -1, an interrupt is generated during the play session.

4.7 Four Bit per Pel Packed Format

To fully support Windows Chicago, Nodric-1M should support 4bit/pel packed format. CPU will be able to write only 8bits or more at a time. To modify only 4bits the CPU will do read modify write and mask four bits (bring them from CPU latches)
The following picture shows the actual format:



In order to get Nordic-1M to support this mode, we need to place the VGA Video Data Path in 8bit per pixel mode with pixel doubling (mode 13) but disable the mechanism that concatenates adjaisant 4bits to make one 8bit pixel displayed twice (at a divided by two RAMDAC VCLK) and disable as well dividing by two the RAMDAC VCLK.

On the CPU side chain 4 address scrambling should be disabled and data should be shifted right like in extended 256 color modes.
In nordic-regs-rev9.lst we assigned SR26[0] to enable this graphics mode.

4.8 Robin's Ideas on High Resolution Panels for Nordic-1M

Nordic's objective is to be able to center and fill the screen on 800x600 panels and to center an 800x600 picture on 1024x768 panels. The main focus is 800x600 panel support TFT and dual scan STN.
In TEXT there will be three options:
- horizontal and vertical centering with 9x16 fonts (disable 640x480 force to 8dots font)
- auto-expand the font to fill the screen
- special font to fill the screen

In Graphics there will be tree options:
- horizontal and vertical centering
- use a driver to run at maximum resolution
- automatic expand to 800x600 (only if s/w verification shows it being OK).

In all cases horizontal and vertical options will be decoupled (different enable bits).

Here's a list of what needs to be done:
a. Expand horizontal and vertical centering capability from 640x480 to 1024x768.

b. Shadow all H/V CRTC registers except HDE and VDE.
The vertical registers are shadowed now, but the horizontal registers are not
We need to shadow CR0, 2, 3, 4 and 5. These registers will be written by the BIOS at POST. The same mechanism to enable/disable vertical shadow is used to enable/disable horizontal shadow.

c. Support 10dot character-clock and CRT-FIFO-Read / Shift/Load (Video-Serializer Load). Now only 8dot and 9dot character-clocks are supported. For smooth-scrolling the pel-pan has to be expanded to 10 positions (0:9).

d. TEXT auto-expand will be as follows:
- horizontal: replicate the last pixel once for 9 dots wide fonts and twice for 8 dots wide fonts.
- vertical: replicate all odd scan-lines

TABLE 3. Font Expansion for Different Panel Sizes

Font-Size/Panel-Size	480	600	768
8x14	8x19	10x21	10x21 + center
8x8 with scan-ln. doubling	8x19	10x24	10x24 + center
9x16	8x19	10x24	10x24 + center

Please note that in text vertical expansion is done on the scan-line counter as well as the vertical display line counter, but it does not affect the vertical non-display line counter.

e. Graphics modes expansion (to be implemented only after s/w verification)
Graphics expansion is less important as it is assumed that important applications will run at maximum panel resolution with a driver.
We'll need to supply drivers for many applications with high res. panels !!
Vertical expansion:
- 350lines -> replicate all odd scan-lines
- 400lines -> replicate all odd scan-lines
- 480 lines -> replicate every 4-th line

Horizontal:
- center
- duplicate every 4-th pixel
- ~~duplicate every 4-th pixel with diagonal shift~~

~~(scan-line 0 -> 1st pel, scan-line 1 -> 2nd pel, scan-line 2 -> 3rd pel, scan-line 3 -> 4th pel ;~~

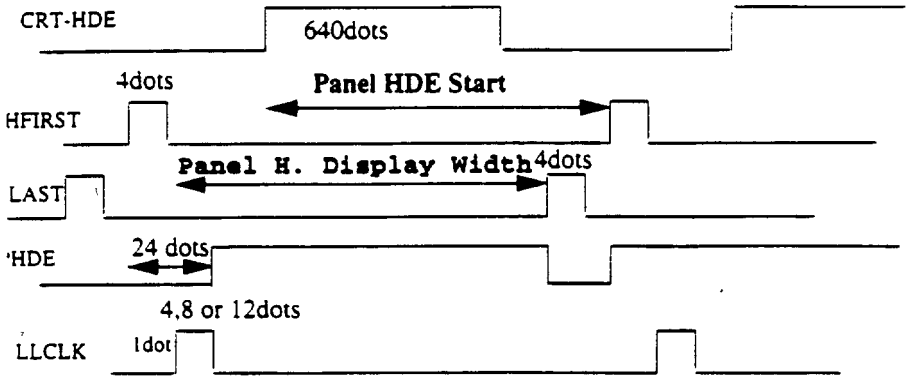
f. Please note that when character clock is expanded to 10 dots, h/w cursor also needs to be positioned at 8 or 9, so it needs one more bit of fine position.
SR2E[0] will be the msb of h/w cursor (default zero) to be used in this case.

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4.8.1 Panel Horizontal Timing Control in Nordic

If in Terminator all panel timing is based on HSYNC and VSYNC programing, in Nordic it will be independent of HSYNC and VSYNC programming.

Horizontal Timing for 800x600 panel with 640x480 picture:



Registers for Panel Horizontal Timing Control

This set of four registers are used to generate horizontal panel timing with 640x480 or 800x600 panels and to center horizontally a 640dots or 720dots picture on an 800x600 panel.

CR40 No Center Panel HDE Start Register

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. This register is used to program Panel Line Clock Start and Panel Display Enable Start with both 640x400 and 800x600 panels any time no horizontal centering is needed.

CR41 Panel HDE Start Register to Center 720 dots

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register

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will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 720 dot mode (text or graphics - RIX mode only) is centered on an 800x600 panel. If horizontal expansion is on CR40 is used.

CR42 Panel HDE Start Register to Center 640 dots

[7:0] Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 640 dot mode (text or graphics) is centered on an 800x600 panel. If horizontal expansion is on CR40 is used.

CR43 Panel HDE Dot-Clock Skew Control Register

[7:6] Panel Line Clock Width:
- 0 = 4 dot-clocks
- 1 = 8 dot-clocks
- 2 = 12 dotclocks
- 3 = reserved

[5:4]CR42 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

[3:2]CR41 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

[1:0]CR40 value fine (dot-clock) skew:
- 0 -> no skew
- 1 -> delay Panel HDE start by one dot-clock
- 2 -> delay Panel HDE start by two dot-clocks
- 3 -> delay Panel HDE start by three dot-clocks

By programming this skew, it is possible to compensate internal delays on Panel HDE for diferent types of panels. If all delays are matched the skew fields should be zero to

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align with character clock.

Automatic switching between these three registers will be done based on CRTC and Sequencer programming and the type of panel used (640x480 or 800x600).

CR 44 Horizontal Panel Display Width Register

The value in this register is expressed in 4 dot-clocks (never divided by two).

[7:0] Panel Display Width in hex expressed in 4 dot-clock chunks. As it is used to compensate for internal delays, this value is close but not exactly 640/4 or 800/4.

4.8.2 Horizontal CRTC Registers Shadowing

In order to run VGA programs on 800x600 panels, Nordic needs to shadow the horizontal timing registers except the display enable end, which is application dependent.
(T1 has shadows only for horizontal total.)
This is because all horizontal timing registers but HDE have to be set-up for 800x600 in order to run an 800x600 panel. Symulscan with 800x600 panels runs even the CRT as an 800x600 display in all graphics modes.
In T1 as well as in Nordic, vertical panel registers are mapped at R2x, R3x.... accesible when CR2D[7] = 1. In nordic these registers remain there.
IN T1 there are two registers: **R0x and R1x** which represent HTot shadows, accessible with **CR2D**[7]. They are no longer used in Nordic, **but there is a replacement for them, independent of CR2D**[7].

In Nordic, H Total, H Retrace Start and End, H Blank Start and End are shadowed. Each entity has two values to chose from: a value for dclk/2 and a value for dclk not divided by two. The effect selection is done automatically based on SR1[3] value, but for access there is a selection bit: CR2C[4] to control which of the two sets of registers gets read or written.

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Here is a summary of the horizontal shadow registers and its controls:

CR2C[5] write protect for horizontal shadow

1 -> write both the shadow registers and the corresponding standard VGA registers fields (some registers are not accessed entierly but only in their timing part)

read back the shadow registers

0 -> write only the standard horiz. timing VGA registers (the shadow registers are write protected). Changing onlt the value of these registers does not have any effect over the CRTC timing.

read back the standard VGA horiz. timing registers

CR2C[4] Select the set of horizontal timing shadow registers to be used (low rez or normal). This bit is reutilsed from T1: it was low power RAMDAC mode - tie now the logic L) .

0 -> select Ry for access

1 -> select Rz for access

To diferentiate from the Rx registers which still exist as in T1, and are vertical panel registers, we'll call the two sets of horizontal shadows mapped in the same address space Ry and Rz (Ry = normal, Rz = dclk/2 case)

The effect of Ty and Rz is controlled by SR1[3] (dclk/2 bit).

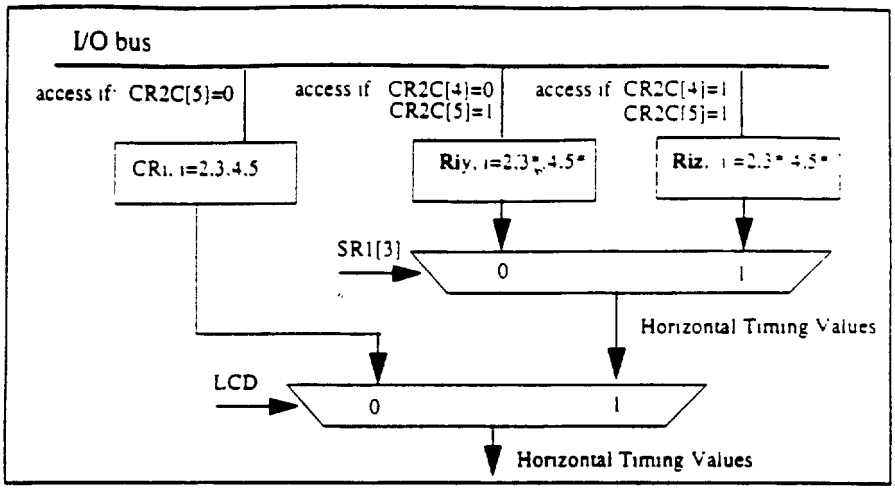
The Horizontal Timing shadow registers are:
R0y,z R02y,z R03y,z (only lower bits) R04y,z R05y,z (only lower bits)

When CR2D[7] =1 we can access only the panel registers: R2x.... RBx. In this case we cannot access either the VGA standard registers or the horizontal timing shadow registers. **Please note that R0x and R1x are reserved in Nordic. Their function is replaced by R0y,z.**

Standard VGA CR0,2,3,4,5 horizontal timing registers (only the timing fields) do not have any effect on the CRTC: only the shadow registers have effect.

Note: Vertical Blank registers CR15 and CR16 are only write protected in T1 - not shadowed. This seems to be an error... so they should be shadowed in Nordic.
When using blank as overlay, DEn becomes blank and the shadow registers create the overlay both horizontally and vertically, but they are no longer write protected by CR2C[3] or [5]... As in 5428, they will not be write protected at all as the overlay is used only under MS Windows which is a controlled environment.

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4.9 TV-Out Support in Nordic-1M

Nordic's objective is to be able output data to an analog TV Encoder chip thus supporting a cheap way of displaying on a TV. The main application is graphics, probably under windows, TV display and tape-recordig are of interest.
Nordic will run in a locked interlaced mode at 13.5MHz for NTSC and it will use the LCD panel supprt shadowing mechanism (the shadow Horizontal and Vertical CRTC registers) to prevent the application from changing the CRTC set-up. Even the dotclock frequency will be locked. Horizontal and vertical display enable will be open to the application. Nordic will provide analog RGB, Composite SYNC, NTSC/PAL and TV-ON to the TV encoder. AD720 and MC1377 analog TV encoders that accept RGB input will be supported directly (with no glue logic).
Nordic will have edge skew h/w on the appropriate signals in order to meet the TV Standards timing requirements .
In this mode Nordic will not be able to run a panel or a CRT monitor... no simulscan supported with TV-OUT. But the same system will display on a panel, a CRT monitor or a TV with minimum glue logic.

Digital TV Encoders are not supported.

All standard VGA modes plus 640x480 8bpp can be supported, though special set-modes are required, as they all run interlaced. I suspect that we'll end up supporting only a few important modes. Should we compress text to 8dot wide fonts?

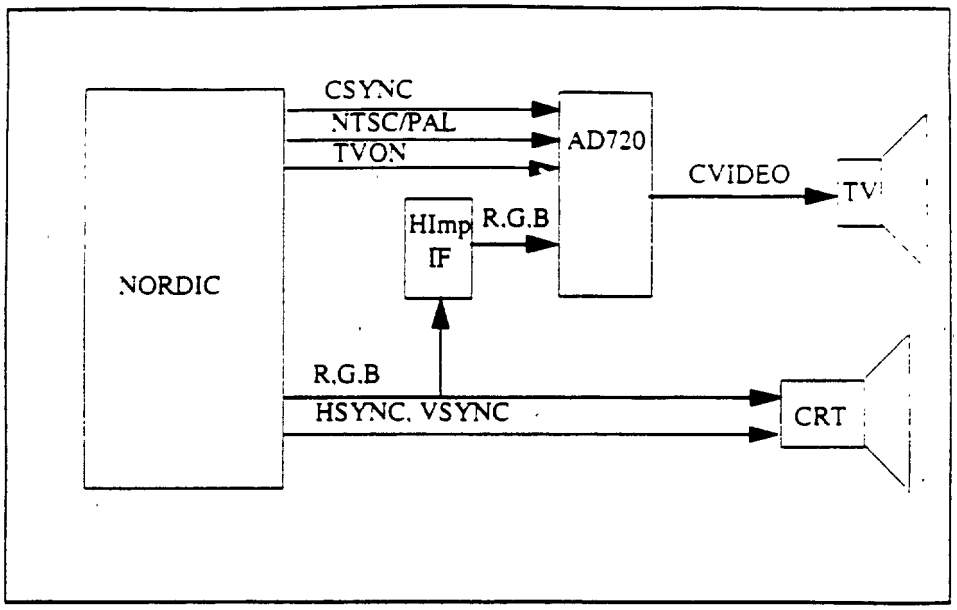


TABLE 4. Data on TV Standards

PIXCLK	Multiples of Line Frequency	Active Pixels per Line	Field Rate
12.2727MHz	780xFH	640	60Hz
14.75MHz	944xFH	768	50Hz
13.5MHz	858xFH	720	60Hz
13.5MHz	864xFH	720	50Hz

Signals to be supplied by Nordic:

- CSYNC = Composite SYNC signal
- NTSC/PAL = a programable output selecting the TV Standard NTSC (1) or PAL (0) The value of CR30[2] comes out on the pin.
- TVON = H for the TV Encoder to be ON, L for it OFF. The value of CR30[3] comes out on the pin. If CR30[3] =0, CSYNC and NTSC/PAL pins are L.

In Nordic-1M all these signals will come out to the panel pins when a certain configuration bit is enabled.

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Vertical Timing

Vertical Blank and the appropriate CRTC registers are programmed to generate Blank which in TV case is the actual Display Enable.

For NTSC program 9 lines of VBlank.

For PAL program 7 lines of VBlank. In h/w Nordic will generate 7.5 lines of VBlank in this case by delaying the trailing edge by 0.5 line

Vertical Sync Registers will be programmed for Field Sync generation

For NTSC program 3 lines.

For PAL program 3 lines and get 2.5 lines by delaying the leading edge by half line.

Horizontal Timing

Two basic pulses are generated:

- HREF1 = Horizontal Reference 1 which is HSYNC start with 64 dotclocks width CR30[1:0] controls the fine skew of this edge by increments of two dot-clocks.
- HREF2 = Horizontal Reference 2 which is a pulse marking the middle of the line between two HSYNC start edges. CR19[7:0] are used to program the start of this pulse.

CR30[1:0] controls the fine skew of this edge by increments of one dot-clock.

Note that HREF1 and HREF2 skews are in sync: HREF2 skew is half HREF1 skew. Horizontal Total is 858 dot-clocks at 13.5MHz for NTSC and 864 dot-clocks at 13.5MHz for PAL.

Composite SYNC Logic Equation is:

CSYNC = [(HREF1 + HREF2) & VS] trigg368dclk-pls + -> Field Sync (serration)
[(HREF1 + HREF2) & VS*&VB] trigg32dclk-pls + -> Equalization
[HREF1 & VB*] trigg64dclk-pls -> standard sync during display time

Where: VS is Vertical Sync programmed time
VB is Vertical Blank programmed time
* is a logic negation
trig32dclk-pls means: on the rising edge of this signal generate a 32 dot-clocks wide pulse.

There are four ways to connect the video encoders and the CRT. We are now in the process of deciding which one is the best:

1. The simplest way to connect the TV decoder is to assume that the CRT Monitor should not be hooked to the notebook computer at the time the TV is. In this case we can put a high resistance voltage divider (2KOhm) to get the required 0.7V or 1.0V full swing to the decoder. The 2KOhm voltage divider will not practically affect the 50 Ohm resistance on the CRT, when the CRT is hooked on. The disadvantage of this method is that it requires a CRT to be disconnected from the note-book computer when connecting a TV. The TV encoders get RGB input through an AC connection (a capacitor) so the DC source may be a high resistance.

The advantage is that it is simple and low cost.

2. There are no buffers or other resistors than usual We control the RSET resistor value on the LM334 current source depending on the presence of the CRT Monitor hook-up or not. If the CRT Monitor is not hooked-up, we adjust IRef so that DAC-s full swing output voltage is 0.7V (or 1.0V) with a 150 Ohm load. If the CRT Monitor is detected to be hooked up, RSet will be left as it is now. The adjustment is done automatically with a transistor. This approach requires a programmable output (from Nordic or Core Logic) to control RSet value. The detection of the CRT Monitor presence is done by s/w the standard VGA way.

3. Put 50 Ohm load on the DAC output and feed it to the TV encoder and to an Analog Voltage Repeater that drives the CRT Monitor RGB lines. This way DAC output is always 0.7V full swing independent if the CRT Monitor is hooked to the notebook or not.

This approach works for AD720 but not for MC1377 which requires 1V full swing. With this approach the presence of the CRT monitor cannot be detected VGA style (incompatibility issue ?).

4. Leave the CRT path unchanged, except for a low resistor shunt added in series.Convert the constant current delivered by the DAC into voltage that is amplified to NTSC/PAL level depending on the type of encoder used. Requires fast operational amplifiers on each gun, but allows operation with or without CRT connected and color compare.

This looks to be the best scheme but it is also the most expensive. The op-amp can be used also as a filter to limit the spectrum and avoid cross talk in color modulators.

Note: According to Fong-Jim Nordic DAC has some oprtational limitations: at 5V DACVDD, if the load is 150 Ohm and the DAC input is all ones (FFH) the output will be indeed 2.1V as expected.

If the load decreases (to more than 150 Ohm) , the output voltage will be increasing up to 2.7 V. At that point it will stop increasing: the DAC will be out of its operational range This is OK for what we are trying to do with TV-OUT.

At 3.3V though, according to Fong-Jim the DAC output will follow the load only up to about 1.1V. This would require a 50 Ohm load at all times. With a 50 Ohm load the maximum DAC voltage at both 5 and 3.3V is 0.7V, within the operation range.

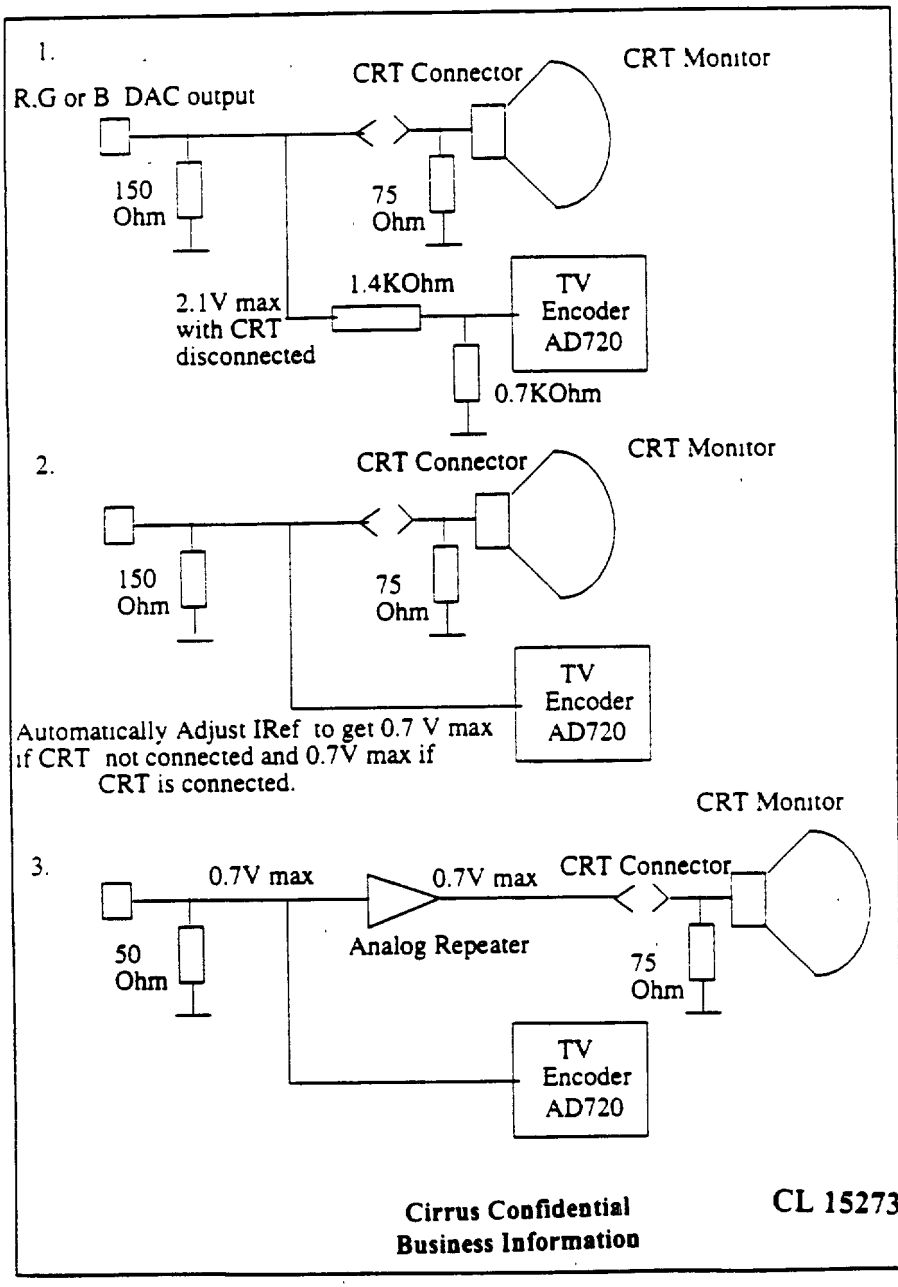
The question is: how to add a 75 Ohm load when there is no CRT in there?

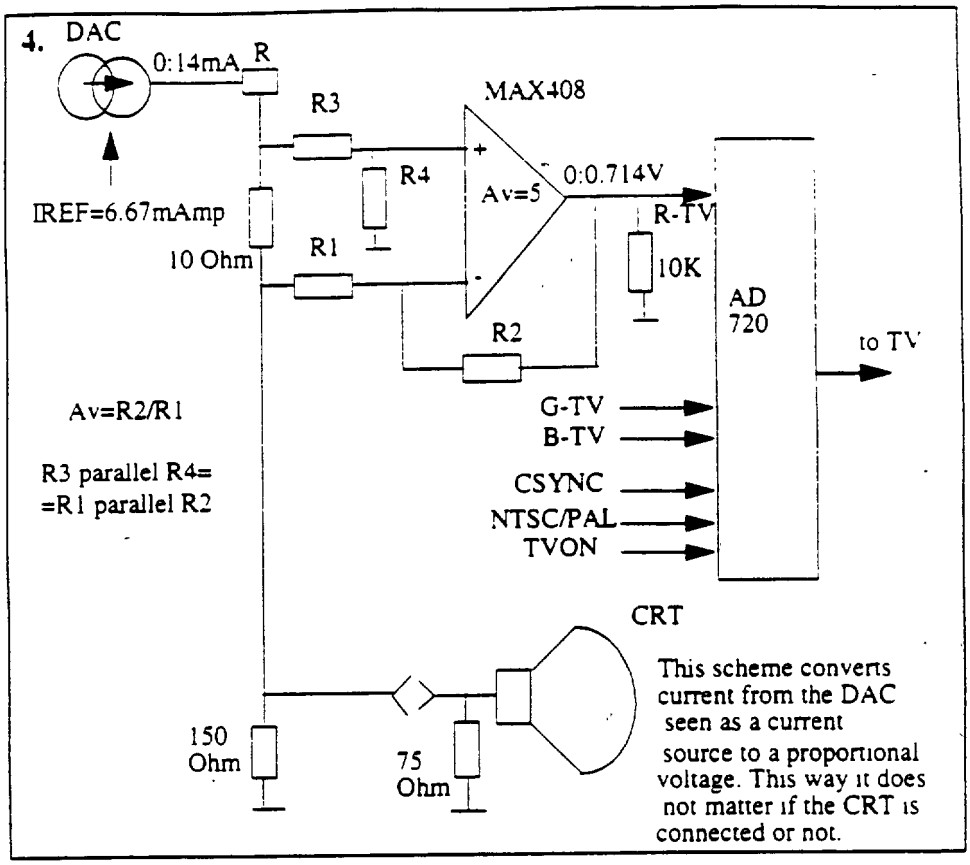
I see two simple solutions: either use TV-OUT at 5V DACVDD (switch CVDD and DACVDD to 5V for TV-OUT) or make an external connector similar to a CRT connector that one plugs into the back of the notebook when the CRT is not in use. This connector should have 75 Ohm resistors to GND on RGB lines.

There may be other solutions too... everyone is invited think.

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Three possible ways to connect an Analog PAL/NTSC TV Encoder to DAC output.





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4.10 H/W ICON Support for Nordic-1M

Nordic-1M will support a h/w icon with the following features
- Up to 4 64x64 Icons displayed at the same time as a vertical bar.
- All Icons move together and they are inedex by 64 scan lines.
  The Icon start reference point is top left corner.
- Horizontal Resolution is one pixel programed coarse as character clocks and fine as pixels exactly as a h/w cursor.
- Vertical Resolution is one scan-line.
- Each Icon has inependent display control for
  - icon number i enable for display (i=0:3)
  - display mode: 3colors + transpency or 4 colors
  - blink enable at text cursor rate (or half of it)
  - horizontal pixel doubling (extendes towards right)
  - vertical scal line doubling (extends down)
  - mamory map selection: two maps available per icon
- H/W Cursor goes on top of H/W Icon
- Icon memory model is and phisical address space are very similar to h/w cursor
  Actually the icon resides in memory in h/w cursor area: Nordic supports half the number of h/w cursor maps 5428 does and uses the remaining space for icon maps. Eight 64x64 icon maps are supported: two for each icon we can display. Icon memory map assignment is fix.

H/W Icon S/W Model

Icon position will change at set mode if it is not compensated. BIOS should service the icon so that it keeps the position stable in all graphics modes: read current position and translate in the same position in the new graphics mode. The BIOS should have a call to set-up the h/w icon position and another call to control which icon is displayed and how

What we need:
a. Horizontal Start Position in character clocks and pixels
  Will be programmed exactly as h/w cursor at SR10,30,50,70,90,B0,D0,F0.
  (or SR "odd" "zero"). The upper 3 bits of index define the fine (vclk) position.
  SR2A[6] is the fine postion msb to be used with 9 and 10dots fonts.See 542X Reference Manual page 9-13, SR10 description.
Note: 1. If character clock or vclk change (8/9/10 dot cclk or vclk/2) the horizontal position should be adjusted.
  2. As with h/w cursor the horizontal and vertical position of the icon are synchronized: s/w writes the horizontal position first, but the new position effect takes place only after vertical position was updated.

b. Vertical Start Position in scan lines.
  Will be programmed exactly as h/w cursor at SR11,31,51,71,91,B1,D1,F1.
  (or SR "odd" "one"). The upper three bits of index define the low order three bits

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of position in scan lines. See 542X Reference Manual page 9-14. SR10 description
How will Nordic know to program icon or cursor?
One bit will tell if icon is programmed instead of cursor. As the icon position is programmed seldom, this mechanism does not affect performance while saving address decode h/w.

c. Enabling icon position modification by CPU is done in the same register h/w cursor is enabled. SR12.

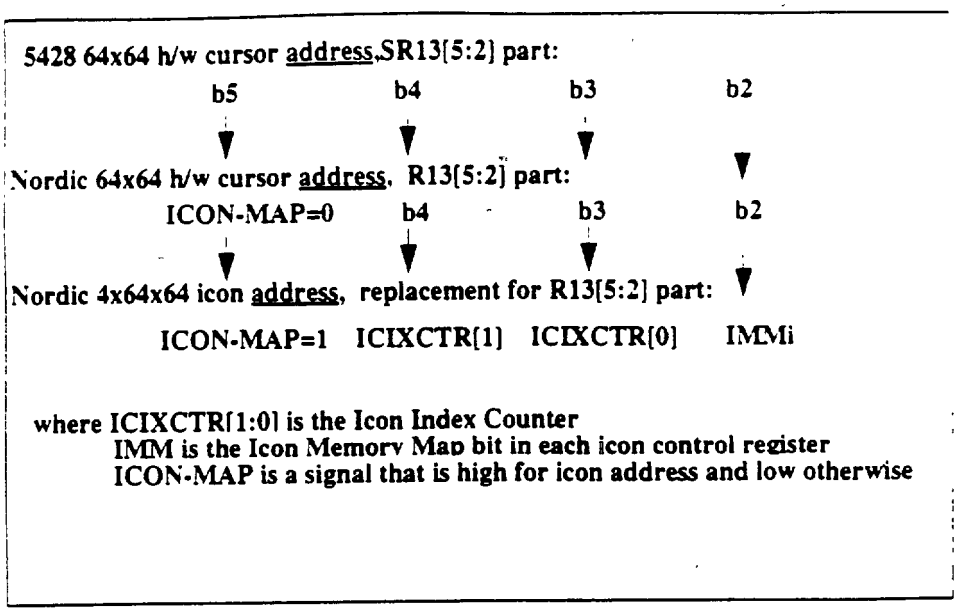
SR12[3] Enable CPU access for Icon Position Modification
(default:0 = disable = use the same I/O address for cursor position modification)
This bit affects both horizontal and vertical position.

d. Icon and h/w cursor memory map selection:
5428 uses SR13[5:0] for 32x32 h/w cursor memory map selection (64 maps) and SR13[5:2] for 64x64 h/w cursor memory map selection (16 maps).

In Nordic, SR13[4:0] still select h/w cursor memory map, but the memory address bit which in 5428 is controlled by SR13[5] is no longer controlled by SR13[5]. It is controlled by an internal signal whose value is always 0 when a h/w cursor is addressed and 1 when icon is addressed. So in Nordic SR13[5] is no longer used to select a h/w cursor map. Only half of the 5428 h/w cursor memory is available for Nordic h/w cursor memory map. In Nordic there are 32 32x32 and 8 64x64 h/w cursor memory maps available.

The icon address is generated exactly as the h/w cursor address, but the source of the address map selection is no longer SR13[5:0] (it cannot be as SR13 is used for h/w cursor). SR13[5] is also noy used. To generate icon mamory map select, a two bit counter counts the first, second, third and fourth set of 64 scan lines on the Vertical Total Line Counter (the one not affected by vertical expansion). This two bit counter output, called the Icon Index Counter (ICIXCTR) will replace SR13[4:3] in Icon Memory Map Address generation.
A signal called ICON-MAP will be generated during Icon addressing. This signal is 1 if an icon data is to be fetched from memory and 0 otherwise (including when h/w cursor data is to be fetched from memory).
ICON-MAP signal will replace SR13[5] in both h/w cursor and icon memory map selection address.
One register bit in each icon control field will select the first or second memory map for each icon to be retrived from memory. This bit called Icon Memory Map (IMM) will

replace SR13[2] in icon memory map generation.



e. Icons Control Registers

Each Icon has a field of bits attached to it

0.- icon i enable for display (i=0:3)
1.- display mode: 3colors + transpency or 4 colors
2.- blink enable at text cursor rate (or half of it)
3.- horizontal pixel doubling (extendes towards right)
4 - vertical scal line doubling (extends down)
5.- mamory map selection: two maps available per icon

Six bits per icon, all defaulting to zero. The icon enable bits select which icon is displayed
Start at SR2A register.
Use **SR2A,2B,2C,2D[5:0]** for Icon 0,1,2,3 control.
If an icon is not enabled, do not generate the memory cycles for its data... if it is not difficult to do, and do not display that icon.

f. SR2A[7] is Icon Test bit. Normally it is zero, only in test mode it will be 1.

g. The colors for the Icon are in the 16 location RAM extension at location 258.
See SR12 description in 5428 Technical Reference Manual.
Locations 256 and 257 are accessible with pixel address 0 and F for h/w cursor access.
Locations 259, 260, 261 and 262 are accessible with pixel address 3,4,5,6 as icon colors 0,1,2 and 3.
When three colors plus transparent attribute is used, the pixel addresses will be 4,5,6, for colors 1,2,3 (so pixel address 3 and color 0 of the 16 location special RAM are not used).

h. **SR2A[6]** is the most significant bit of fine horizontal position for the h/w icon:

SR2A[6] SRX[7] SRX[6] SRX[5] --> bit3 bit2 bit1 bit0

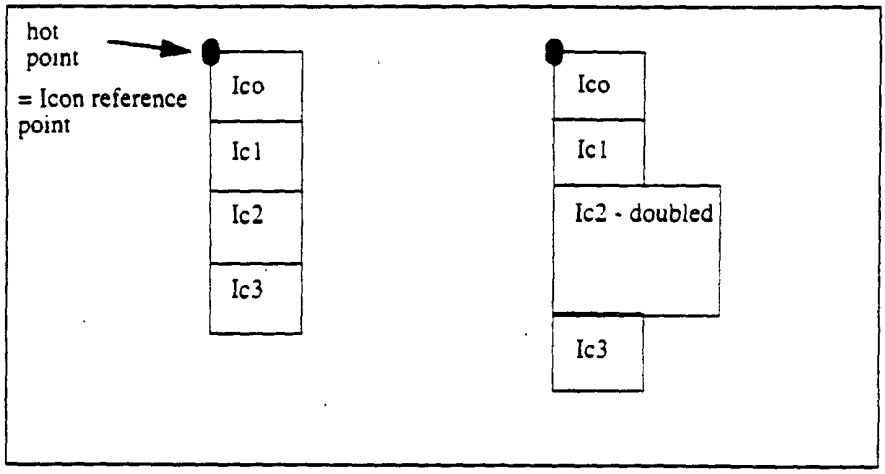
Please note that SR2A[6] will be used only in 9 or 10 dots text when the fine position is 8 or 9.

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1. Please note that when character clock is expanded to 10 dots, h/w cursor also needs to be positioned at 8 or 9, so it needs one more bit of fine position.
SR2E[0] will be the msb of h/w cursor (default zero) to be used in this case.

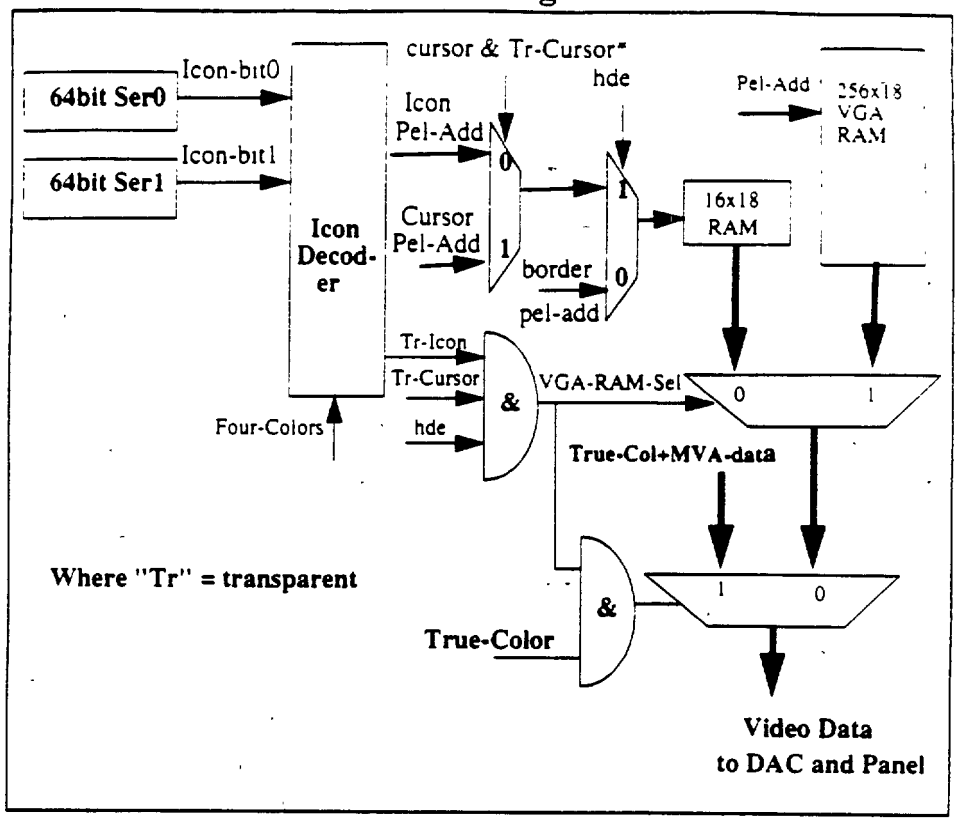
H/W Activity for Icon

1. Horizontal and Vertical Window
2. Address Generation including the independent scan-line counter for Icon
3. Memory cycle generation (at the end of line, after h/w cursor if icon and cursor are on the same line)
4. Icon Latch, Serializer and Data Path including icon blink
5. Horizontal and Vertical Doubling



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Icon Data Path Block Diagram



4.11 Dithering in Nordic

Due to new pixel depth modes and for increased flexibility the dither block in Nordic is diferemt than T1.
In Nordic the dithering is subtractive, (not additive like in T1). This moves the dither error (= double shade) to black where it is less obvious than it was before (when it was white).

CR4C - Input Resolution Override Register for Dithering

Bit	Definition
[7]	Enable Input Resolution Override (default disable) Normally the graphics mode resolution is decoded and fed to the dither block. For all graphics modes that go through the RAMDAC RAM - 6bits/gun is automatically the input resolution. For 5:5:5 RGB or 5:6:5 RGB or 8:8:8 RGB we use

a diferent input resolution: 5 for 5:5:5 and 5:6:5 and 8 for 8 8 8 RGB
In all cases the proper input resolution is automatically selected
If there is a need to overide this value, than we will use this bit to enable the override and write the new value in bits 3:0. For 8 bit per gun we write 8 (1000) for 6 bits per gun -> 6 (0110) and for 5 bits per gun -> 5 (0101)

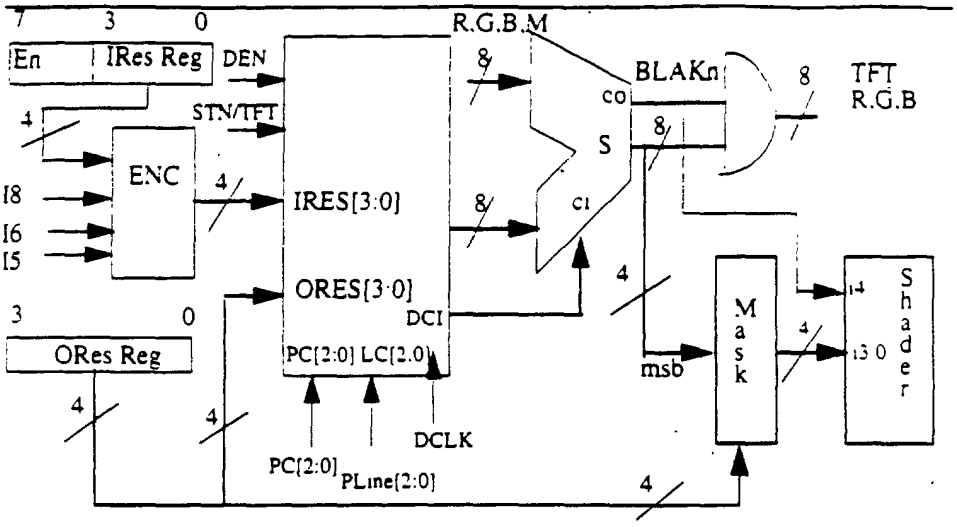
[6:4] Reserved

[3:0] The binary value of the override input resolution
1000 -> 8bit/gun
0110 -> 6bit/gun
0101 -> 5bit/gun

CR4D - Output Resolution Register for Dithering

Bit	Definition
[7:4]	Reserved
[3:0]	The binary value of the output resolution for dithering 1000 -> 8bit/gun (TFT) 0110 -> 6bit/gun (TFT) 0100 -> 4bit/gun (TFT or 16 shades STN) 0011 -> 3bit/gun (TFT or 8 shades STN) 0010 -> 2bit/gun (4 shades STN) 0001 -> 1bit/gun (2 shades STN)

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TFT: 8,6,4,3 bits/gun

STN: 4,3,2,1 bits/shade (16+1,8+1,4+1,2+1 shades, +1 = force black)

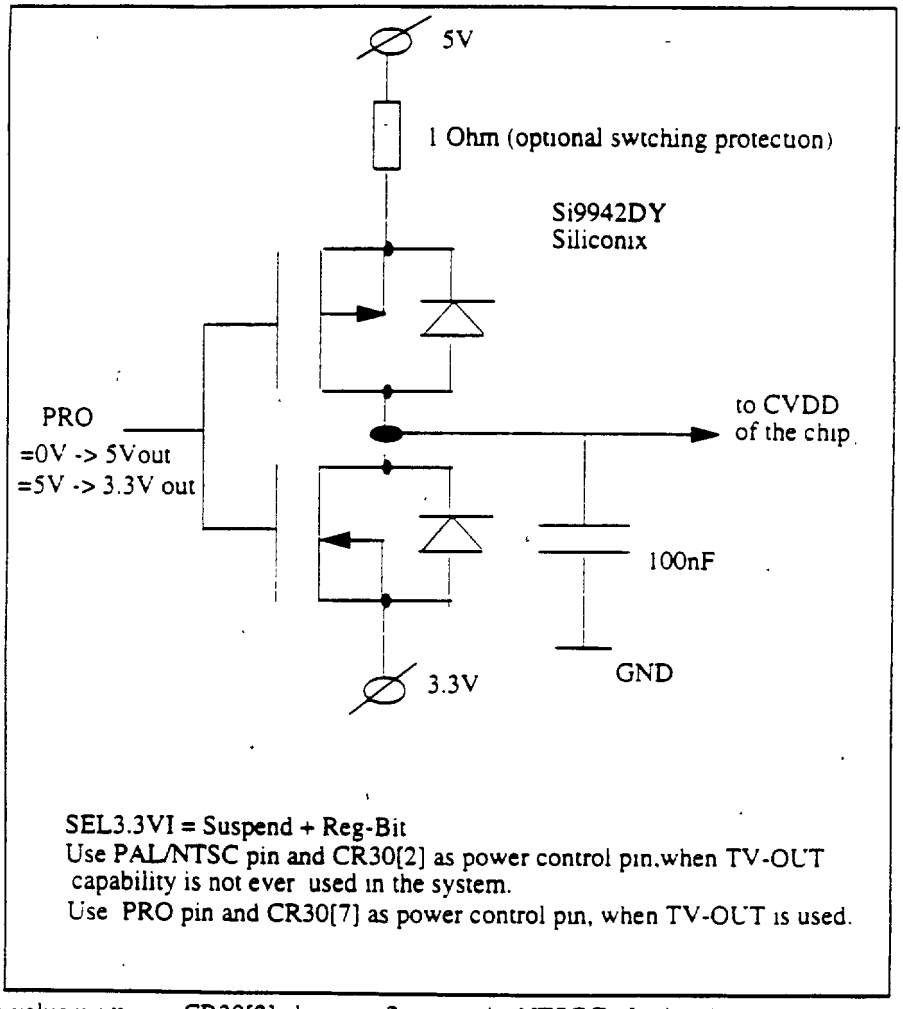
Nordic Dithering

4.12 Core-VDD Control

Because Nordic can run higher frequency memory-clock at higher Core VDD (5V) but it offers maximum power savings at low Core VDD (3.3V), we look for a mechanism to dinamically switch at set-mode or when going into suspend from 5V to 3.3V and vice-versa.

This would allow for instance to run 24bpp 640x480 mode at 5V CVDD while switching back to 3.3V when going into suspend mode or when switching to a 4 or 8bpp mode

All Nordic needs to do in this case is supply a programable output to be used to switch an external circuit



SEL3.3VI = Suspend + Reg-Bit
Use PAL/NTSC pin and CR30[2] as power control pin,when TV-OUT capability is not ever used in the system.
Use PRO pin and CR30[7] as power control pin, when TV-OUT is used.

The value written in CR30[2] always reflects on the NTSC/PAL pin which thus can be usd as a generic programable output.

In a system without TV-OUT capability, NTSC/PAL bit and its output pin can be used to

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control when CVDD is 5V or 3 3V This way, in most modes the chip may be optimesed for power running at a lower mclk frequency, while in certain modes it will be optimised for performance, running at 5V CVDD and a high frequency mclk (higher than what can be run at 3.3V). Because NTSC/PAL pin is tied to CRTVDD which is 5V in most systems, this bit is the first choice for the CVDD switching function.

5.0 Nordic-1M Pinout Specification 208 pin package:

System Interface (reference is VESA VL bus): **74**

(on BVDD)

DAT31:0
HIMEM0/ADR[24] (normally used as ADR[24], but it can be used as any upper address or any logic combination of upper addresses. The valid value of this pin for Nordic address space is programable in VESA VL and PCI bus.
HIMEM1/ADR[25] (normally used as ADR[25], but it can be used as ADR31 and leave 2GB of upper address space reserved for MPEG/JPEG boards). The valid value of this pin for Nordic address space is programable in VESA VL and PCI bus
With these two pins, Nordic can directly decode up to 64MB of CPU address space in VESA VL bus.
ADR[23:2]
BE3n,BE2n,BE1n,BE0n
LADSn,LDEVn,RDYn
M/IOn, W/Rn
RESETn, LCLK
RDYRTNn,
EBROMn/SLEEPIn (Enable BIOS ROM Buffers on all busses or when not in ISA or SLEEP Input active L. If this pin is L, the chip goes in sleep mode as if 3c3[0] is 0 or 46E8[3] is 0. The ISAPU read-back register bit configures the pin for EBROMn. If not in ISA bus, this pin is configured as SLEEPIn and it should be tied H if not used.
INTR, CLK32K, OSC/XVCLK (14.318MHz or External VCLK)
SUSPI/BLI, SBYI/ACTI/FCEVIDEOn
(32KHz clock input,
Supend Input/ Back-Light Input
Stand-by Input/Activity Input/VAFC External Video Control Input - controlls the direction of FCP[7:0]. Pin configuration controlled by VAFCPU. Most systems will
use only one direction for VIDEO, probably video in, so the fact the FCEVIDEO is on BVDD should not require voltage translation).

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Configurations: - VL/PCI/ISA bus, support/not BIOS, 8/16bit BIOS
- Need a register bit to select SUSPEND Input or Back-Light Input Default is SUSPEND Input.
- Need a register bit to select Stand-By Input or Activity Input Default is Stand-By Input.
- SUSPIn, BLIn, SBYIn, ACTIn are level triggered, active L inputs In Nordic there is no Suspend pin polarity bit as in T1 (SR8[4])

Note: a.In PCI bus, Alpine used ADR17:2 as BIOSA15:0. We assume that all portable systems will use a motherboard video BIOS and do not support an adapter BIOS in PCI. We do support an adapter BIOS in VESA VL bus and ISA to facilitate demo board design.

b. EBROMn is active on all bus types: in ISA is generated on Address Decode and MEMRn, while in VL and PCI is unlatched address decode. In PCI bus the BIOS should be relocatable, an option we do not support. That is why we say that we do not support BIOS in PCI. We do support IOCHRDYn and RDYn/TRDYn for BIOS accesses too. All this logic should already be in 5428 (ISA and VL) and Alpine (PCI).

c. The 5428 Feature Connector pins are available in all buses. A register bit enables them early in the logic to save power when not in use.

d. In ISA RESETn has to be inverted outside the chip.

System/Bus Interface Signal Mapping

(See 54xx Reference Manual for Feature Connector Pins Description: FCyyyy)

TABLE 5. VESA-VL <-> PCI bus <-> ISA bus Pin Mapping

VESA-VL	Intel-PCI	ISA
HIMEM	--	--
ADR23 16	--	LA23 16
ADR15:9	--	SA15:9
ADR8	PAR	SA8
ADR7	STOPn	SA7
ADR6.2	--	SA6:2
BE3n	C/BEn3	SA1
BE2n	C/BEn2	SA0
BE1n	C/BEn1	SBHEn
BE0n	C/BEn0	RFRSHn
DAT31.22	AD31:22	--
DAT21 19	AD21 19	--
DAT18	AD18	MWRn
DAT17	AD17	IOCS16n
DAT16	AD16	IRQ
DAT15.0	AD15:0	SD15:0

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TABLE 5. VESA-VL <-> PCI bus <-> ISA bus Pin Mapping

VESA-VL	Intel-PCI	ISA
RESET	RESET	RESETDRV
LADSn	FRAMEn	BALE
LDEVn	DEVSELn	MCS16n
RDYRTNn	IRDYn	AEN
W/Rn	IDSELn	IORn
M/IOn	--	MRDn
LCLK	CLK	IOWn
RDYn	TRDYn	IOCHRDY
EBROMn/VADRn	VADRn	EROMn/VADRn
INTR	INTR	ZEROn

Notes: 1. SW2, SW0/MCLK/XMCLK and SW1 pins are normally used by the BIOS as panel type switches readable on SR24[2:0].

2. XMCLK and XVCLK (on OSC/XVCLK) are needed for manufacturing test of the chip. When they are used, SR24[1:0] will wiggle at clock rate and they should be masked on the tester.

3. MCLK and VCLK are needed for manufacturing test of the clock synthesizer and for chip debug.

DRAM Interface (for assymetric, dual WEn 256Kx16 DRAM-s): **50**
(on DVDD)

MA9:0
MD31:0
RAS0n,RAS1n,CASn/WEn, OEn
WE0n/CAS0n,WE1n/CAS1n,WE2n/CAS2n,WE3n/CAS3n

Configurations: symetric/assymetric DRAM, dual WEn/CASn

Note: a) For dual CASn DRAMs, the WE0n:WE3n pins become CAS0n:CAS3n, while CASn becomes WEn.
b) Two RAS-es are used for two banks.
c) OEn is not actually needed as we use early write.

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Clock Synthesizers: **6**
(MAVDD, MAVSS feed mclk clock synthesizer, VAVDD, VAVSS feed dclk clock synthesizer)

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MAVSS, VAVSS, MAVDD, VAVDD,
MFILTER, VFILTER
(Can we design a clock synthesizer without an external filter?)

CRT & TV-OUT Interface and RAMDAC related pins: 13
(DAVDD, DAVSS feed all RAMDAC custom layout)

R,G,B (analog)
IRef, DCVDD1, DCVDD2, DCVSS1, DCVSS2

On CRTVDD:
HSYNC , VSYNC TO (these two pins are on CRTVDD)
CSYNC O (Composit Sync to be used with any analog TV Encoders like AD720.
CSYNC is activated by SR25[4]=1, otherwise is forced 0.)

NTSC/PAL O
(A programable output that can be used to control a TV Encoder input that selects the TV standard. This pin is a generic programable output. Its value is not affected by SR25[4].)

On FPVDD:
TVON/RES O (Generic Programable Output controlled by CR30[3] .
It can be used to control AD720 TV Encoder Power Control Pin.)
TVON is on FPVDD (not on CRTVDD like the other TV-OUT pins)
This pin is also reserved for future use (DRAM-s).

Note: If TV-OUT feature is disabled CSYNC, NTSC/PAL and TVON are forced L (to avoid powering up the TV Encoder in case it is powered off when not in use).

FLAT PANEL and Power Management Interface (on FPVDD): 31

R7/SUD3, R6/SUD2, R5/SUD1, R4/SUD0, R3/SUD7, R2/SUD6, R1/FCP[3], R0/FCP[2],

G7/SLD7/sud3/UD3/TD7, G6/SLD6/sud2/UD2/TD6, G5/SLD5/sud1/UD1/TD5, G4/SLD4/sud0/UD0/TD4, G3/SUD5, G2/SUD4, G1/SUSPSTn/FCP[1], G0/SBYSTn/FCP[0]

B7/SLD3/sld3/LD3/TD3, B6/SLD2/sld2/LD2/TD2, B5/SLD1/sld1/LD1/TD1, B4/SLD0/sld0/LD0/TD0, B3/MOD, B2, B1/OVRW, B0/FCVLK

(use slow edge pads and stagger them modulo 4)

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FPVDCLK, LLCLK, LFS, FPDE, (use slow edge output pads)
FPVCC, FPBL, FPVEE

Notes.

b. R1:0, G71:0, B1:0 (24 bit TFT panel extra video data out pins)

c. We need also bits for SUSPST and STANDBYST, PANEL-ON/OFF, PANEL-IN-POWER-UP-or-DOWN. Dwarka, do we have this now ?

d. We assume that only STN panels need external MOD

e. No NPD pin.

f. FCP[3:0] pins are I/O-s whose direction is controlled by FCEVIDEOn in VAFC configuration. FCVCLK is the clock that clocks them in and which should be used to clock them while they are displayed or at least to resynchronize them before being latched on the internal clock. FCVCLK is always an input when in VAFC configuration.

Nordic TFT Panel Data Pin Name versus the actual TFT Panel Data Signal for diferent types of TFT Panels

Nordic Pin Name-> /Panel Type	RGB7	RGB6	RGB5	RGB4	RGB3	RGB2	RGB1	RGB0
8bit/gun	RGB7	RGB6	RGB5	RGB3	RGB2	RGB1	RGB0	RGB0
6bit/gun	RGB5	RGB4	RGB3	RGB2	RGB1	RGB0	N.U.	N.U.
4bit/gun	RGB3	RGB2	RGB1	RGB0	N.U.	N.U.	N.U.	N.U.
3bit/gun	RGB2	RGB1	RGB0	N.U.	N.U.	N.U.	N.U.	N.U.

Where N.U. = Not Used for Panel Data with this type of panel.

~~Audio Port (on ADVDD):~~ ~~6~~ **Removed on 12/24/93**

~~SDO (SErial Data Output to CODEC pin SDIN)~~
~~SDI (Serial Data input from Codec pin SDOUT)~~
~~FSYNC (Frame Sync Output)~~
~~SDCLK (Serial Data Clock I/O)~~
~~D/Cn/AUXS1 (Data/Control Select Output or CS4231S Chip Select for the ISA bus)~~
~~PDN (Power Down Output)~~
~~Note: These pins can be used as extensions for 24 bit TFT panels, in which case the chip does not support the audio port.~~ ~~**Note also that CS4215 has Resetn pin.**~~

Miscellaneous Pins: **12**

Following pins on MVDD:

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SW2/RES4CS I (Switch #2 or reserved for SDRAM support in the future)
SW1/RES4CKE I (Switch #1 or reserved for SDRAM support in the future)

SW0/MCLK/XMCLK I/O with PD controlled by XReset
(Switch #1 or mclk driver buffered output for tesing and debug or external mclk for testing; a special register bit disables this output in normal operation*for power savings
Default: Input on which either SW2 or XMCLK comes in
Only if the special register bit is set, this input becomes output and outputs MCLK from the clock synthesizer for testing.
The special register bit defaults 0 = the pin is configured as Input. Please note that a h/w configuration PU/PD controlls if the actual internal mclk comes from an internal or external source, but this PU/PD does not control if SW2/MCLK/XMCLK is an input or an output.)

RES4PMS Free Pin with no buffer on it.

Following Pins on PVDD:

TRWn I (Test Latch Load Enable, active L - for pinscan & test mode)
VCLK/FCDCLK I/O (Switch #0 Input or vclk driver buffered output for testing and debug, or VAFC Dot-Clock Out ; Default for this pin is Input on which SW#0 is applied; VCLK and FCDCLK is the same signal, the name is diferent to ease reference to VAFC spec)
FCP[7:4] I/O Feature Connector Data Pins bits 7 to 4. The other Feature Connector pins are shared with some panel or host bus pins.
FCESYNCn/RES4SDCLK I 5428 Feature Connector ESYNCn pin - controlls the direction of FCBLANKn and its effect and tri-states HSYNC and VSYNC.
FCBLANKn I/O Feature Connector active low bidirectional Blank signal. Its direction is controlled by FCESYNCn.

Digital, Mixed Voltage Power Pins: 22

BVDD1, BVDD2, FPVDD1, FPVDD2, MVDD1, MVDD2, CRTVDD, CVDD1:4, VSS1:11

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Total Pins Used: 208 (with two Reserved pins and three other pins that could be freed.)

Pinout Modifications in rev. 3.8 relative to rev. 3.7 09/11/93

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1 Took-out Whisper Support Pins WWRn, WRdn, WAD[3:0], FPCn

2. Reduced the number of CPU Address Pins. ADR[24:27] went-away Use HIMEM to place the chip outside 16MB of memory for linear addresing

3 Killed CRTVDD and placed CRT Interface on Host Bus VDD.

4. Introduced VAFC pins in a unique pinout configuration in both VESA VL and PCI
Added VAFCPU a pull-up to enable VAFC (VESA Advanced Feature Connector)
ADR[27:24] VAFC pins, and R[7:4], G[7:6], EROMn/VADRn, SUSPI/BLI, SBYI/ACTI get a configuration for VAFC -> total 14 pins.
SW0/VCLK will be used as VAFC VCLK, losing SW0 pin as panel type when VAFCPU is used.
In PCI bus, no ADR pin will be shared with VAFC.
ASW0PU (Alternate Switch 0) will be added on MD pins to replace SW0 pin when VAFC is enabled by VAFCPU. ASW0PU will read-back in the same register bit as SW0, so the BIOS will not feel any modification in the reporting scheme. The chip will draw more power in suspend with VAFC.

5. Moved SW2, SW1/MCLK/XMCLK the two reserved pins (one obtained by killing CRTVDD)and TRWn on MVDD to prepare for SDRAM pin compatible option in the next Nordic that supports SDRAMs. Marked them as "reserved for SDRAM pin name" It looks that TRWn will not be needed, but it was moved on MVDD so that in case it is needed, it is available (in this case we'll need an extra switch for SDRAM support or at least to disable TRWn test mode effect).

6. Rearanged VAFC pins as pins R4 and R5 were used by VAFC - an error.

Pinout Modifications done on 01/06/94 rev. 3.0

1 Update Panel Data Pins based on Robin's Table.
2 Move MOD pin on a Panel Data Pin used in 18bit TFT
3 Move OVRW on a 24bit Panel Data Pin.
4 Removed pin configuration for TV-OUT support with digital encoders. All pins marked TV were removed. As a result, some pins like LLCLK, LFS, FPDE, FPVDCLK have one function now
5 Removed WavePort pins, including AUDVDD: total 7 pins freed.
AUX2 and TVG muxed on EBROMn are no longer needed either.
6. Added one more CPU address pin: instead of HIMEM, Nordic has now HIMEM0 and HIMEM1, corresponding to CPU Address 24 and 25 or any other external decode of the high order CPU address bits. In the proccess of adding this pin, most CPU Interface pins on the right side were moved to the right by one pin.
7 Added CRTVDD supplying HSYNC, VSYNC, CSYNC, NTSC/PAL CRT and TV Interfaces output buffers.
8. EBROMn is shared with TVON, the power-on signal for AD720. So, in ISA bus with on chip BIOS support, AD720 power on cannot be directly controlled by Nordic.
9 Added pins for Analog TV Encoder support - AD720 and MC1377 .
a. CSYNC = Composit Sync signal
b. NTSC/PAL = 0 -> NTSC, 1-> PAL

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c EBROMn/TVON (see #8)

10 ASW0PU "Alternate Switch 0 Pull-Up" pull-up on pin 155 MD[26] was removed as SW0 is now not multiplexed

11 Demiltiplexed some of the pins previously multiplexed.

a. Pin 168 TWRn/RES4PMS is now RES4PMS. a pin reserved for synchronous DRAM support.

b SUSPI/BLI/FCBLANKn is now SUSPI/BLI. not affected by the Feature Connector Enable Configuration

c. As a consequence of b. pin 97 is FCBLANKn (not muxed with anything) Please note that FCEVIDEOn is still muxed with SBYI/ACTI as before. as Standby Input and Keyborard Activity are less important functions in a system

d. SW0 is no longer muxed on VCLK/FCDCLK. So VLK/FCDCLK is a pin but it moved to pin 103 in the PVDD area, to be consistent with FC power supply

12. SW1, muxed on MCLK/XMCLK (pin197) became SW0. This is just a name change to have the switches placed in a more consistent manner.

13 SW1 is now muxed with a reserved pin: RES4CKE, pin 148, which before was totally reserved. The idea here is to go for pu/pd with SDRAM-s for SW2 and SW1, while keeping SW0 on MCLK even with SDRAM-s.

14 Pin 147 is Reserved. It is actually one of the WavePort pins, but placed in-between Memory and Panel VDD busses (on MVDD) for maximum flexibility. To acheive this, the pins on its right were moved to the right by one

FPVEE <BIAS> moved down to pin 98 (it was 105)

15 TRWn is now by itself on pin 96, on FPVDD.

16 The names of all flat panel data pins reflect the panel type table attached to this document.

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Configuring Nordic-1M

If Terminator used specially assigned pins to configure the chip, **Nordic-1M will use some of the MD31:0 pins sampled on the Reset trailing edge,** similar to Mustang. The pad cells will have an active pull-down controlled by an **extended Reset** signal. The pull-down resistence will be about 75KOhm. An external pull-up less than 60KOhm is needed only if the option is used. In Suspend, the MD pads are inputs and the DRAM OEn is H so no DC current is drawn by the configuration h/w. An external resistor is needed only if the configuration pin has to be H at Reset. H/W configuration can be read via s/w too.

All h/w configuration latches are read accessible via I/O. The h/w configuration is latched on Reset trainling edge. (these latches were r/w, with s/w PU read, having

only read is enough).
We'll define the configuration pins to minimize the number of external resistors:

CPU Bus Configuration:

On MD18:16 & -> no external PU = 32bits VESA VL bus at 33MHz or less bus clock
& MD23 -> MD16 PU = 32bits PCI bus with Burst PU called "PCIPU"
-> MD17 PU = 16bits ISA bus PU called "ISAPU"
ISAPU controls also the pin EBROMn/SLEEPIn
In ISA bus this pin is EBROMn output; otherwise it is SLEEPIn input to be tied H if not needed
-> MD18PU = 32BIT VESA VL BUS AT 50MHZ BUS CLOCK
PU called "FVLPU"
-> MD23 PU = 32bits PCI bus no Burst PU called "PCINBPU"
This is a reserved configuration in case burst does not work on a PCI bus.

Reads-back in SR22:

PCIPU on MD16 -> SR22[0]
ISAPU on MD17 -> SR22[1]
FVLPU on MD18 -> SR22[2]
PCINBPU on MD23 -> SR22[7]

Clock Configuration:

On MD19 (reads back on SR22[3])
-> no external PU = internal MCLK and VCLK clocks, from the internal clock synthesizer
-> MD19 PU = use external clocks from SW1/MCLK/XMCLK and OSC/XVCLK
PU called"XCLKPU"

This PU is used for manufacturing test.

One reg. bit is needed if internal clock is selected to control outputing mclk on the MCLK/XMCLK pin = 1 if use internal clock then output it on SW0/MCLK/XMCLK pin. -> SR23[0] is this bit.

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Memory Configuration: SRF[0]
No Pins, Use Two Register Bits -> 2CAS/2WE bit=H 2WE, bit=L 2CAS (default =L)
-> Symetric/Asymetric bit=H Asym., bit=L Sym. (default=L)

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BIOS Support: (reads-back on SR22[6] for BIOS8PU)

Nordic-1M supports 16bit or 8bit BIOS and only in ISA bus configurations
The BIOS is always supported when in ISA

On MD22 -> no external PU = 16bit BIOS
-> external PU = 8bit BIOS (no MEMCS16n decode on C000)
This option is mostly for debug in case 16 bit BIOS range decode is not fast enough
If the BIOS support is disabled, this configuration is don't care. Called "BIOS8PU"
Please note that Nordic-1M supports C000 BIOS only in ISA.

In a normal note-book the BIOS is at E000:0 or C000:0 but it is not supported by Nordic, so no external component is needed.

Sleep Address Selection:

On MD21: Sleep Address Selection (reads-back on SR22[5]).
-> No external PU = sleep at 3C3[0] - to be used when Nordic is on the Mother-board (most cases)
-> External PU = sleep at 46E8[3] - to be used when Nordic is an adapter (like a PCMCIA card and/or an adapter to turn desktop into an environment friendly PC) Called: S46PU
Note that Nordic-1M comes-up awake.

Feature Connector Configuration: (reads-back on SR24[7])
On MD25:
-> No external PU = no Feature Connector Support: outputs used only for FC are forced L, I/O are forced inputs, I/O and inputs are forced on the chip so that they do not take power if not connected externally.
-> External PU = All pins needed for FC including OVRW are active.
Called: VAFCPU

~~On MD26: Alternate SW0 Selection (Reads-back on SR24[0] when SR24[7] is 1)~~

Total: 9 H/W PU configuration options.
In normal operation with FC enabled up to three external PU-s may be needed (bus type if not VL and FC).
In normal operation with FC disabled up to one external PU-s may be needed (bus type if not VL and FC)

Summary of PU/PD Configuration Pins and Register Bits where they can be read-back:

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SR22 [7:0] **H/W Configuration Read Register #1**

Read only register, written on reset trailing edge by activating PU/PD on MDi pins. The PD-s are inside the pads active only during XReset (extended reset).

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[7] 32bits PCI bus no Burst h/w PU configuration on MD23. It is called "PCINBPU (read only bit).
This is a reserved configuration in case burst does not work on a PCI bus.

[6] Select 8 bit BIOS support (if 1). Otherwise 16 bit BIOS support if the BIOS support is at all enabled. PU on MD22.

[5] Resereved for Sleep Address Select: reads back S46PU (MD21).
1 = I/O address 46E8[3] as sleep address (needs external PU).
0 = I/O address 03C3[0] as sleep address (no external PU is needed).

[4] Reserved

[3] Select external clocks: MCLK and VCLK on SW0MCLK/XMCLK and OSC/XVCLK. (default: internal clock synthesizer, SW0 and OSC).
PU on XCLKPU on MD19.

0 = internal clocks with the pins used as inputs for panel type switch #1 and OSC. If SR23[4] and SR23[0] are 1, VCLK and SW0/MCLK/XMCLK, respectively become VCLK and MCLK outputs respectively, for test purposes (only if SR22[3]=0 MCLK can be seen, but VCLK can be seen even if SR22[3]=1 as long as SR23[4]=1)

1= SW0/MCLK/XMCLK and OSC/XVCLK become XMCLK and XVCLK inputs generating directly chip MCLK and VCLK without clock synthesizer. The clock synthesizers are powered down if SR22[3]=1.

[2] Select VESA VL Bus at 50MHz
1 = VESA VL bus at 50MHz selected (needs external PU on MD18)
0 = VESA VL bus at 50MHz not selected

[1] Select ISA Bus with PU on MD17.
1 = ISA bus selected (PU on MD17)
0 = ISA bus not selected (no PU on MD17)

[0] Select 32bit PCI Bus with PU on MD16.
1 = 32bit PCI bus selected (PU on MD16)
0 = 32 bit PCI bus not selected (no PU on MD16)

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If [1:0] = 00 (i.e. no external PU on MD17:MD16) 32bit VESA VL bus is selected.
No more than one PU on MD17:MD16 should be used.

Note: In AVGA3, CF14 is "Enable Local BUs Address Latching Interface". Alpine does

not have this configuration bit We need to do what was done in Alpine to get rid of this Configuration Pull-up/Pull-Down option. *CAN we? WAs this done, Dwarka?*

SR24 Panel Type Switches Register

[7] VAFCPU (VESA Advanced Feature Connector External Pull-up) Read-back. If external pull-up (the bit read-back 1) then all VAFC pins are configured for Video Port Otherwise they have other functions or are disabled if no other function. (Disabled= the inputs are forced = the TTL and CMOST threshold controls are off & the outputs are tri-stated. It actually reads back what is latched on Reset on VAFCPU. VAFCPU is on MD25.

[2:0] SW2:0 pins read back (read only bits) ~~Please note that bit [0] reads back SW0 if VAFCPU (SR25[2]) is 0 and ASW0PU if VAFCPU is 1.ASW0PU is on MD26~~

Configuration Register Bits needed:

Symetric/Asymetric DRAM -> SR8[7] in T1, CF13 in AVGA3
=> SRF[1] 0 = Symetric DRAM Default: 0
1 = Assymetric DRAM

This bit is read only in AVGA3 (reads back CF9), but it is writable in T1. It controlls MCLK frequency as an alternate to SR1F. We will use only SR1F to program MCLK frequency in Nordic. The default MCLK frequency will be 39.374MHz, corresponding to SR1F[5:0] = 18H=22D. This frequency fully meets the spec for -80 256Kx16 DRAM-s.

Two CAS or two WE DRAM -> pin 72 in T1, CF12 in AVGA3
=> SRF[0] 0 = 2 WE DRAM (Default:0)
1 = 2 CAS DRAM

16 or 32bit wide Video Memory (One or Two 256Kx16 DRAM-s or SDRAM-s)
-> not in T1, SRF[4:3] in AVGA3 (01=16bit, 10=32bit)
=> SRF[7,4:3] will be used in Nordic with the same encoding as in AVGA3 (11 is reserved for 64bit wide). Default: 10 (32bit). See Table next page. Please note that we have room to add other types of DRAM-s (SDRAM-s for instance).

In AVGA3 SR8[0] is "CS OUt to EEPROM" a feature Nordic does not Support. Nordic will not change the meaning of AVGA3 bits unless they are read only (like the pins or external PU read back).

SR8[2:0] are in T1 the read-back bits for SW2:0 input pins, but AVGA3 uses them for EEROM programming so we moved SW2:0 read back to SR24[2:0].

In T1 SR8[7] is symmetric/assymetric addressing... in Nordic this is SRF[1].

Two or one Bank 32bit wide DRAM

-> not in T1, SRF[7,4:3] in AVGA3 (00=8bit, 01=16bit, 10=32bit, 11=64bit. SRF[7] controls if 2MB of Video memory are available with 4x512kx8 -0- or with 4 256Kx16 DRAM-s, two banks -1-). *It seems that in AVGA3 to support 1MB with two 256Kx16 dram-s and 32bit wide bus, we select 32bit wide and SRF[7]... but I do not exactly know how this configuration is selected.*

=> SRF[7,4:3] in Nordic, will select the Video Memory Configuration slightly differently than in AVGA3 and Alpine. See the following table.

	SRF[7]	SRF[4]	SRF[3]	Memory Configuration
new	0	0	0	32bit, 2MB=4x512Kx8
	0	0	1	16bit, 512KB=1x256Kx16
	0	1	0	32bit, 1MB=2x256Kx16 (default)
	0	1	1	Reserved (64bit in Alpine)
new ?	1	0	0	32bit, 2MB=4x256Kx16, Two Banks
	1	0	1	Reserved
	1	1	0	Reserved
	1	1	1	Reserved

DRAM Timing select (short RAS or long RAS)

-> SRF[2] in T1 and AVGA3

=> SRF[2] in Nordic, default 1 = short RAS (3.5 L, 2.5H)

BIOS 48KB or 32KB -> not in T1; CF8 in AVGA3. In T1 SR8[4] is Suspend pin polarity. In Nordic Suspend pin is always active L (0 on pin puts the chip in Suspend).

=> SR23[2] in Nordic =0 32KB BIOS (default=0) C0000:C7FFF

=1 48KB BIOS : C0000:CCFFF

The initial BIOS code should be placed in the first 32KB starting at address C0000.

BIOS ROM ZERO* wait select in ISA and fast timing in VL bus

-> not in T1; CF1 in AVGA3

=> SR23[1] in Nordic =0 no ZERO wait state for BIOS in ISA

=1 ZERO wait state for BIOS in ISA, 8MHz bus

Output internal VCLK on VCLK/FCDCLK pin -> not in T1 or AVGA3

=> SR23[4] in Nordic =0

VCLK/FCDCLK is an output pin forced L

=1 either VCLK or

FCDCLK is outputed on this pin,

depending on VAFCPU (read back in SR24[7] value).

If SR24[7]=1 (Feature Connector pins enabled) than FCDCLK is outputed, otherwise, if

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SR23[4]=1 than VCLK is outputed. VCLK out is needed only for manufacturing test

Output internal MCLK on SW0/MCLK/XMCLK pin -> not in T1 or AVGA3
=> SR23[0] =0 this pin is an input namely XMCLK if SR22[3]=1 (enable external clocks) and SW0 otherwise
=1 output mclk

This pin will normally be used as SW0, except for manufaturing test where mclk and xmclk functions are needed.

SuspendI/BLI bit -> not in T1 or AVGA3.
=> SR23[5] in Nordic, 0= Suspend pin in Suspend/BLI pin (default)
1= BLI pin on Suspend/BLI pin

SBY/ACTI/FCEVIDEOn bit. -> not in T1 or AVGA3
=> SR23[6] in Nordic, 0= SBY on SBY/ACTI pin (default)
1= ACTI on SBY/ACTI pin
If SR24[7] = 1 (VAFC pins enabled) this pin is FCEVIDEOn independent of SR23[6].

VAFC Enable bit -> not in T1 or AVGA3.
(read only bit, actually reflecting the status of an external configuration PU: VAFCPU on MD25 latched at RESET or under S/W Control)
=> SR24[7] 0= VAFC Disabled at pins.
All VAFC dedicated pins are disabled to save power: inputs are disabled, outputs are L. **I/O-s are disabled inputs (forced H)** internally.
The shared pins are not in Feature Connector configuration.
1= VAFC Enabled at pins.
If any shared pins, they are now in Feature Connector Configuration.
All dedicated pins are active in this configuration.

Compressed Live Video (SashaPack) Enable bit -> not in T1 or AVGA3.
=> SR24[6] 0= disable (default)
1= enable

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~~Audio In (from CS4215 to Nordic) Enable bit -> not in T1 or AVGA3.~~
~~=> SR24[5] 0= disable (force inputs inactive and outputs L~~

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~~disable AI-FIFO and cycle~~
~~1= enable~~

~~Audio Out (from Nordic to CS4215) Enable bit -> not in T1 or AVGA3~~
~~=> SR24[6] 0= disable (as above but AO-FIFO)~~
~~1= enable~~

Panel Type Switch Read-back -> SR8[2:0] in T1 or SR7[6:4], not in AVGA3
=> SR24[2:0] in Nordic, read only, writable on Reset or under S/W Control (SR24[3])
When SR24[3] whose default is 0, transits from 1 to 0 SW2:0 pin value is latched into SR24[2:0 which cannot be written by I/O.

Please **note** that **R9x[1:0]** TFT Panel type field of T1 was expanded to support 24bit TFT panels:

00 -> 9bit (333) (as in T1)
10 -> 12bit (444) (as in T1)
01 -> 18bit (666) [was x1 in T1 covering both 01 and 10 !!]
11 -> 24bit (888) -> new in Nordic

Notes:

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0.1 a. If 24bit TFT panel is selected, all related pins will be configured for it and it has priority over panel pins configuration settings for cross talk reduction enabled
b. MOD is selected only with STN panels.
c. If 24bit TFT is not selected and VAFC is not selected, then SUSPST is selected on
G1/SUSPSTn/FCP[1] and SBYST is selected on G0/SBYSTn/FCP[0]
d. Panel Data unused output pins are forced 0 when not in use (depending on panel type)

SR25 Timers S/W Reset, H/W Config. #2 & Packed Modes Register

[7] The 8514A RAMDAC address is decoded as valid RAMDAC address in addition to the standard VGA RAMDAC address.
[6] Allows use of EBROMn as external 8514A RAMDAC
In this case it bahaves like 5428.
[5] Enable 1bit/pel packed mode
[4] Reserved for 2bit/pel packed mode
[3] Enable 4bit/pel packed mode
[2] Configure PCI bus Nordic module for Faster PCI write
[1] Reset Stand-by Timer
[0] Reset Backlight Timer

Other Register Related Topics
(See nordic-regs-rev#.lst where # is the latest one)

BIOS SCratch Registers #5 and #6 (2 extra required) (r/w)

SR28:SR29[7:0] are scratch registers.
Note that SR9, SRA, SR14 and SR15 are AVGA3 scratch registers which we keep in Nordic. Also there are 13 18 bit scratch registers in the RAMDAC is SR12[1]=1.

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R9x - TFT Panel Data Format

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[7] Reserved

[6:4 Select a 0 to 7 shift-clock delay from the internal character clock counter
(8 VCLK/Character Clock) to TFT panel HSYNC (LLCLK) signal -> as in T1

[3:2] Panel size select:
00 -> 640x480
01 ->

[1:0] TFT Panel Type:

00 -> 9bit (333) (as in T1)
10 -> 12bit (444) (as in T1)
01 -> 18bit (666) [was x1 in T1 covering both 01 and 10 !!]
11 -> 24bit (888) -> new in Nordic

Registers that are Moved Relative to T1

CR1B[7,4,3,2] (R1B in schematics):

[7] Disable Text Cursor Blink in T1. Do we use this feature in T1?
Enable Blank End Extensions in AVGA3
[4] PCLKO (Panel Clock) no divide by two control in T1.
I am not sure this bit is actually needed in Nordic.
[3] IRQ Every Frame or Every Other Frame ? Is this bit used inT1?
[2] Not Used at All in T1.

I think that all these bits are not actually used. Are they needed ? -> Robin.

CR1C[7:0] & CR1D[7:0]

Are important LCD and Power Management Registers in T1 and Overlay Registers in Alpine. These registers are not in AVGA3, but because they are used in Alpine we may move them to **CR2C[7:0] and CR2D[7:0]**, which requires one more CRTC Index Register Bit. So:

CR1C -> CR2C & CR1D -> CR2D in Nordic relative to T1.

SRF[7]

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In T1 is CRT Refresh Disable. This bit gates /FB/RWC[5] in FB sheet 6. In AVGA3 is DRAM Two Bank Configuration select bit.
I don't think that this bit is used in T1 ? -> Robin.

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SR16

In T1 is used to control the pads for power and threshold. In AVGA3 is not used. In Alpine is CRT FIFO demand threshold and other things ([4:0] are used)

Move SR16 bits of T1 to SR20 to avoid contention with Alpine. Increase SRX Sequencer Register Index to 6 bits.

SR1A

In T1 is used as Test register. In AVGA3 and Alpine is Signature Generator Result Hi
Move T1 SR1A bits to SR21 if it is not replaced by a similar register in AVGA3

Nordic Revision and Mask Codes

Nordic Microsoft ID CR2F: CD
Nordic Revision CR27 (4bits chip code, 7z , where z is BIOS rev. counting down): 2F
Nordic Mask Code CR25: 00
Nordic PCI ID: 1200H

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